400Gb/s Logic Ad hoc report

IEEE 400 Gb/s Ethernet Study Group

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Introduction

- The 400 Gb/s Ethernet Study Group Logic Ad hoc has:
  - Held 2 meetings on June 7th and June 26th
- Reviewed 5 presentations:
  - 400GbE PCS Architectural Options gustlin_01_0613_logic
  - Forward Error Correction for 400G: Initial Thoughts bates_01_0613_logic
  - BER objective format for 400GbE anslow_01_0613_logic
  - 400GE lane configurations vs. FEC options wangz_01_0613_logic
  - Multi-rate support of 400GbE wangt_01_0613_logic

- **Meeting minutes and presentations can be found at:**
  - http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

400GbE Logic Ad hoc Priorities

- The stated charter is: Evaluate 400GbE architecture implementations to make recommendations regarding possible objectives
- Depending on what happens in this meeting with respect to the objectives, we will prioritize presentations that address gaps in the logic objectives going forward vs. discussing PCS options
- Dates of future Logic Ad hocs will be announced via the reflector

Possible 400GbE Logic Related Objectives

- Support a MAC data rate of 400 Gb/s
- Support full-duplex operation only
- Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
- Preserve minimum and maximum FrameSize of current 802.3 standard
- Provide appropriate support for OTN
- To define optional Energy-Efficient Ethernet operation for xxx PMD or interface
  - PMD type likely to define what mode(s) are supported, deep sleep vs. fast wake

- Support a (BER or frame loss ratio, pick one) better than or equal to x
  - Likely to be a lot of discussion around this objective
  - With at least some PHYs using FEC it might be better to specify frame loss ratio instead of BER

Thanks!