400Gb/s Logic Ad Hoc Report

IEEE 400 Gb/s Ethernet Study Group

November 2013 Dallas

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400GbE Logic Ad Hoc Priorities

- The stated charter is: Evaluate 400GbE architecture implementations to make recommendations regarding possible objectives

- The study group has adopted many of the logic related objectives in previous study group meetings, but we have yet to adopt an objective on BER (or FLR). Depending on what happens in this meeting with respect to the objectives, we will prioritize presentations that address gaps in the logic objectives going forward vs. discussing PCS options

- Dates of future Logic Ad hocs will be announced via the reflector

Meeting Details

- The 400 Gb/s Ethernet Study Group Logic Ad hoc:
  - Held 1 meeting on October 23rd
  - Previously opportunity on October 1st was cancelled due to lack of presentation requests
- Reviewed 3 presentations:
  - A 400GbE PCS Option – Mark Gustlin
  - 400GbE PCS Direct Coding Analysis - Haoyu Song
  - Error performance objective for 400GbE – Pete Anslow
- Meeting minutes and presentations can be found at:
  - http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

Thanks!