MMF Objective for 400GbE

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400GbE Study Group

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- Gary Bernstein, Leviton
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Purpose and Approach

- Define, provide rationale for a 400GbE MMF objective
- Use relevant selection of IEEE 802 five criteria (5C)
  - Compatibility
  - Distinct Identity

  } Straightforward

  - Broad Market Potential
  - Technical Feasibility
  - Economic Feasibility

  } Focus of presentation

- Discuss simplest example: 400G-SR16 = 4×100G-SR4
  - Objective does not exclude other embodiments

Compatibility

- Compatible with IEEE 802.3 standard, 802.3 MAC, …

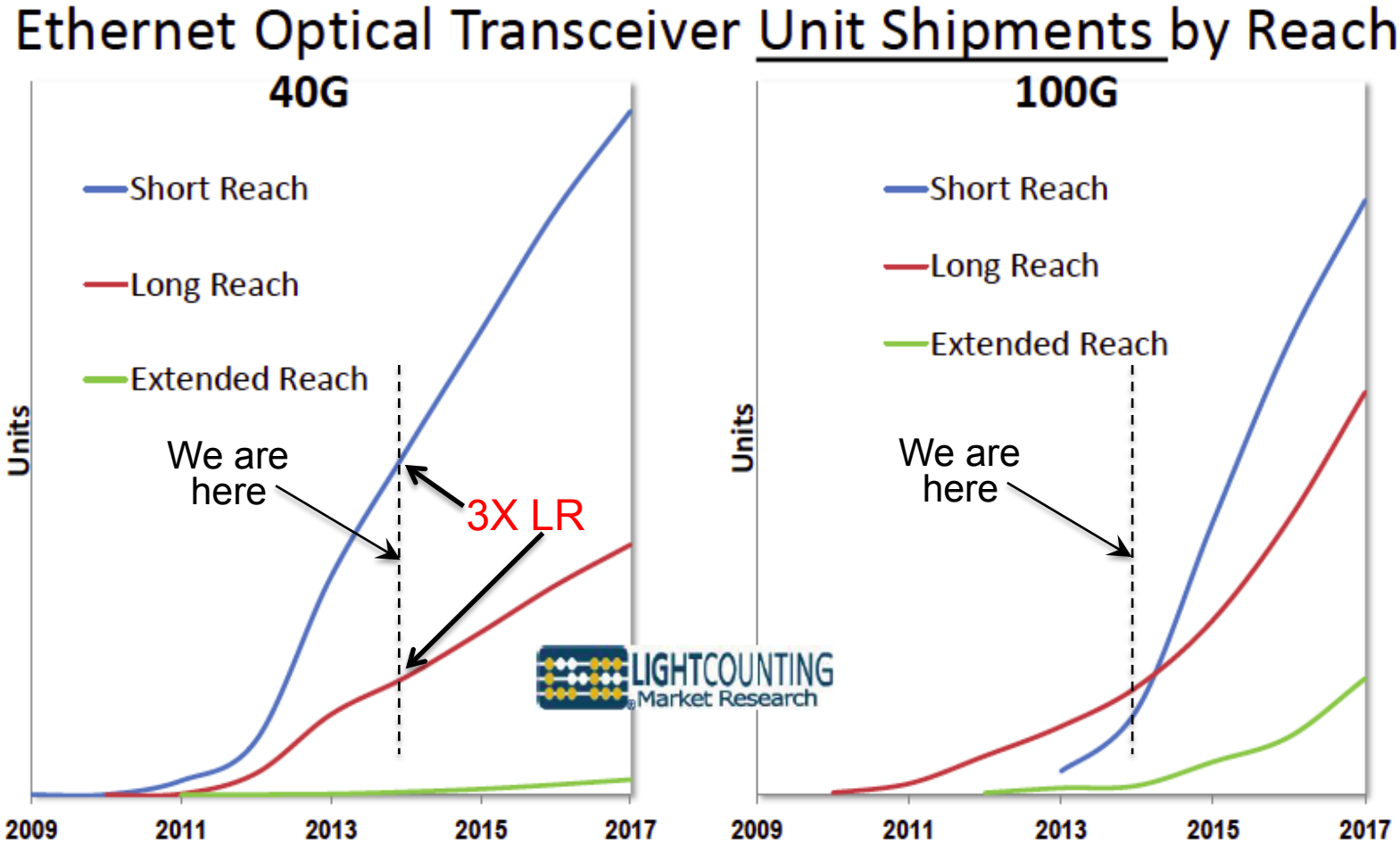
Distinct Identity

- Unique 16-lane x25G 400Gb/s PHY for operation over MMF

Broad Market Potential

At 40G and 100G, the highest volume of ethernet optical transceiver shipments continues to be for Short Reach

from murray_400G_appadhoc_01_1013, rearrangements, additions

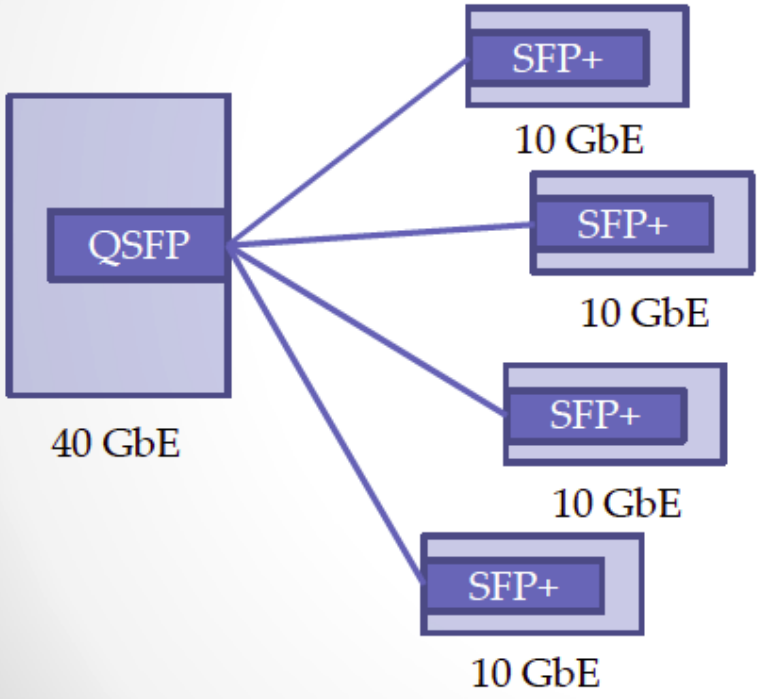


Broad Market Potential

from dambrosia_app_01_1013, with added comment

40 GbE Port Usage (2 of 2)

40 GbE Port Configuration Example #2



"Breakout functionality" is very successful for 40G ➔ 4x10G;
can be similar for 400G ➔ 4x100G

Today's Media*

- Multi-conductor twin-ax**
- Multi-fibre MMF**
- ~~Full Duplex SMF~~
- Multi-fibre SMF

** Being used in data center applications for all above.

* Includes standard & non-standard technologies

Applications Ad Hoc, IEEE 802.3 400 Gb/s Ethernet Study Group
Oct 9, 2013 Teleconference

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Broad Market Potential

"Breakout functionality" is very successful for 40G ➔ 4x10G
can be similar for 400G ➔ 4x100G

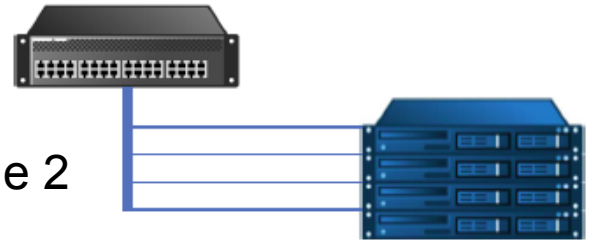
from booth_400_01_0513, with modifications

40G Observations

Four lanes of 10G was extremely useful

- Not everything required a 40G pipe
- Ability to use break-out cables provided a level of "backwards compatibility"

Switch with QSFP+ 4x10G ports

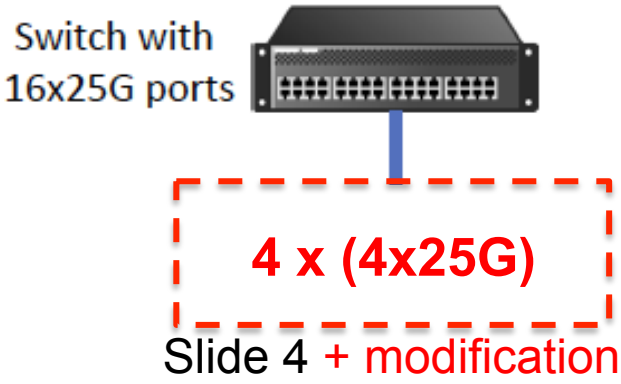


Slide 2

400G Considerations #1

Sixteen lanes at 25G technically possible today

- Build off the upcoming 100G architecture



Slide 4 + modification

Slide 6

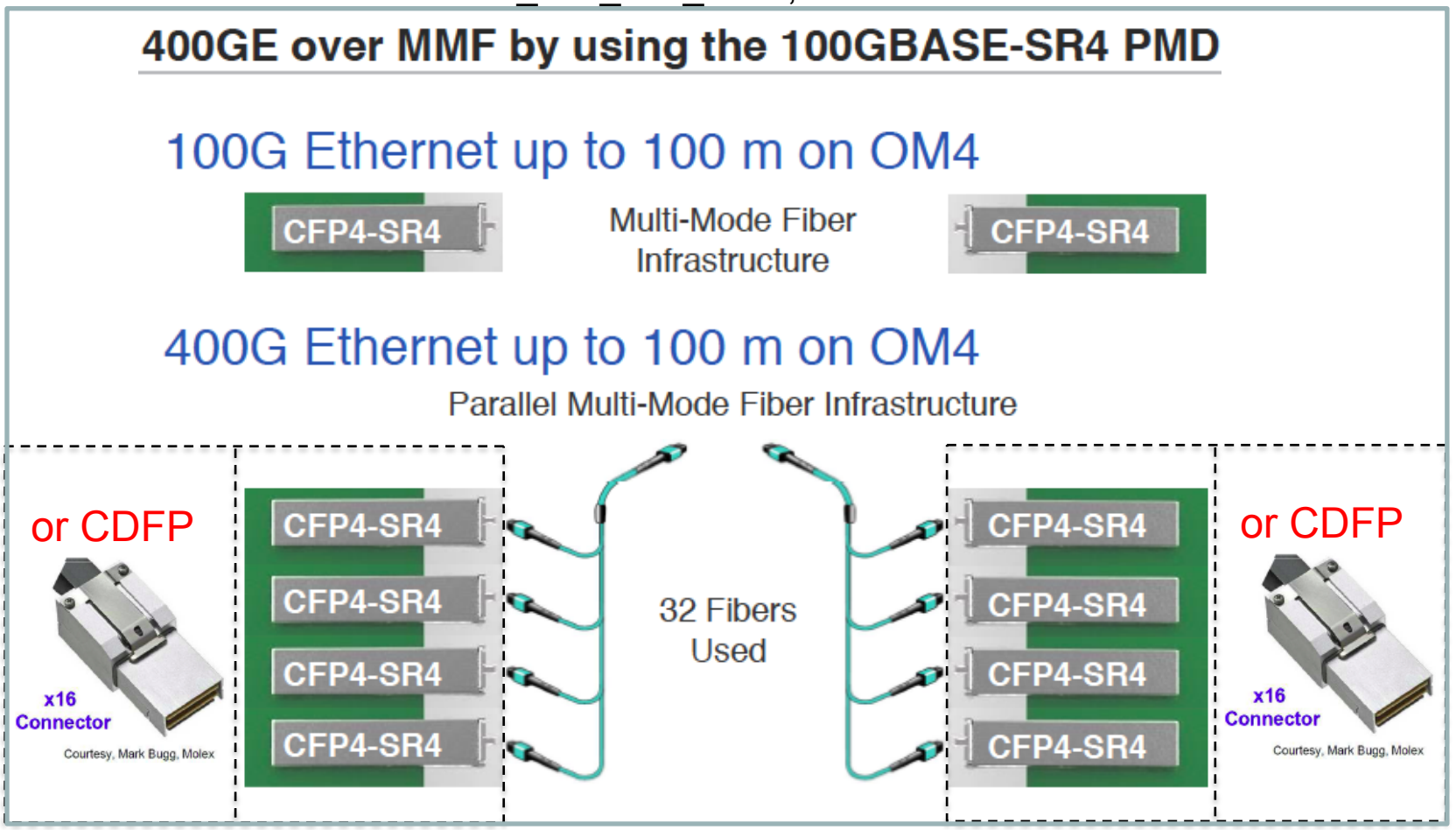
- While 4x10G was not specified, it was a natural outcome
- This is likely to occur again in future generations due to server speeds and switch port density requirements

Broad Market Potential

"Breakout functionality to 100G" makes sense

100G modules likely QSFP28 in volume

from maki_400_01a_0513, with modifications



Broad Market Potential
(more breakout functionality)

from dambrosia_app_01_1013

- Multiple scenarios can be envisioned where 400GbE ports could support higher density / lower rate 40GbE and or 100 GbE PMDs. Some include:
  - 400 GbE based on 16 x 25 Gb/s
    - Could be divided into 4 ports of 100G @ 4 x25Gb/s

- The market is adopting this "breakout functionality" for 10GbE / 40GbE
  - Breakout functionality – the ability to use a port in a lower rate / higher density mode of operation
- "Breakout functionality" will enhance broad market potential of 400GbE by enabling adoption to support higher density / lower rate (40GbE and / or 100GbE) to enable lower 400GbE cost.

Broad Market Potential Summary

- History ➔ SR = highest-volume optical ethernet
  - Already so in 40GbE; imminent in 100GbE
- Breakout functionality e.g. 400G-SR16 = 4×100G-SR4
  - Higher density 100GbE with lower cost
  - Enables earlier and broader market for 400GbE
  - Accelerated volumes accelerate cost reduction
  - Mimics successful use of 40G-SR4 = 4×10G-SR
    - doubled LightCounting's current 40GbE volume
- Applications served
  - Router to transport (e.g. moorwood_app_01_1013)
  - Switch-router, router-router within DC core in 400G mode
  - Switch-switch in leaf-spine architecture, initially at 4×100G
  - Switch-switch in hierarchical star architecture, initially at 4×100G
  - Aggregation of 10G server traffic in 4×100G mode
  - Aggregation of 40G server traffic in 400G mode

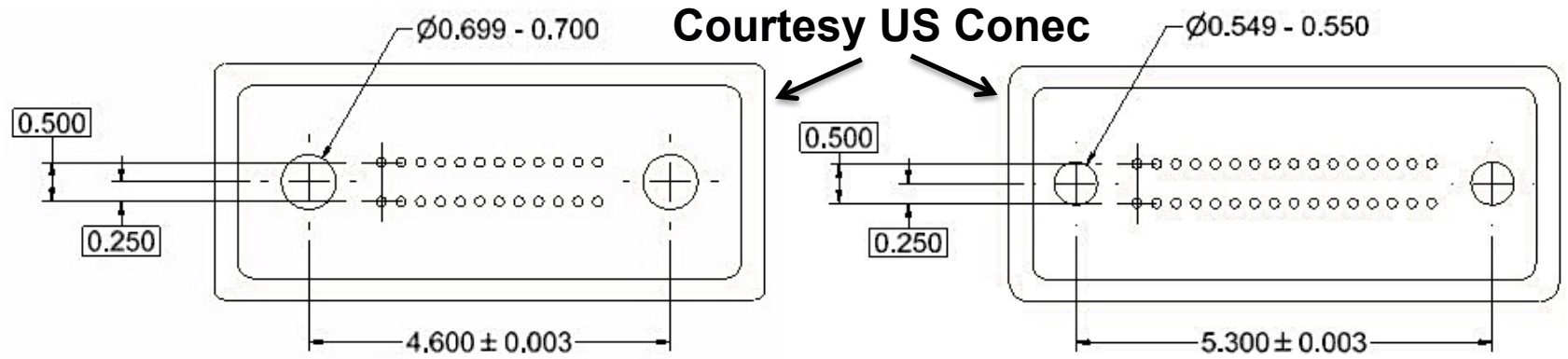
Technical Feasibility

- Simplest example: 400G-SR16 = 4×100G-SR4
- 1st-gen either:
  - Replicated form (e.g. four QSFPs or CFP4s), or
  - Integrated form (e.g. one CDFP)
- Replicated form: 802.3bm deems technically feasible
- Integrated form: Move from 1x4 and 1x12 arrays to 1x16 arrays is not a technological leap
  - VCSEL, PIN, driver, receiver, microlens, fiber:
    - elements and spacings are unchanged
  - 4-element arrays already being standardized at 25/28Gb/s
  - 12-element yields are high ➔ expect 16-element yields similarly high (applies to all types of elements, e.g. VCSELs, PINs, ICs,…)
  - Reliability impact minimal going from 12-element to 16-element
    - Wearout: negligible impact due to array uniformity
    - FIT Rate: incremental increase due to number of elements mitigated by continually-improving materials/processing

Technical Feasibility

2x16-fiber MT connector (MPO-16)

- Existing 2x12 MT defined by TIA-604-5-D and IEC 61754-7
- Proposed features for 2x16 format:
  - Smaller guide pin holes
  - Longer pitch between guide pin holes
  - Same 250um x-pitch and 500um y-pitch as for existing 2x12
- TR-42.13 (TIA) unanimously approved MPO-16 project start
- Discussions initiated at IEC 86B; draft due next meeting



Existing 2x12 MT **Proposed 2x16 MT**

Technical Feasibility

- "CDFP" MSA efforts underway for a highly-compact 400G module based on 16x25G lanes (per direction)

from maki_400_01a_0513

New CDFP MSA

- High-density form factor supporting 16 x 25G
- Likely supporting only copper cabling, AOC, and VCSEL optics
- From slide 26 of http://www.ieee802.org/3/cfi/0313_1/CFI_01_0313.pdf

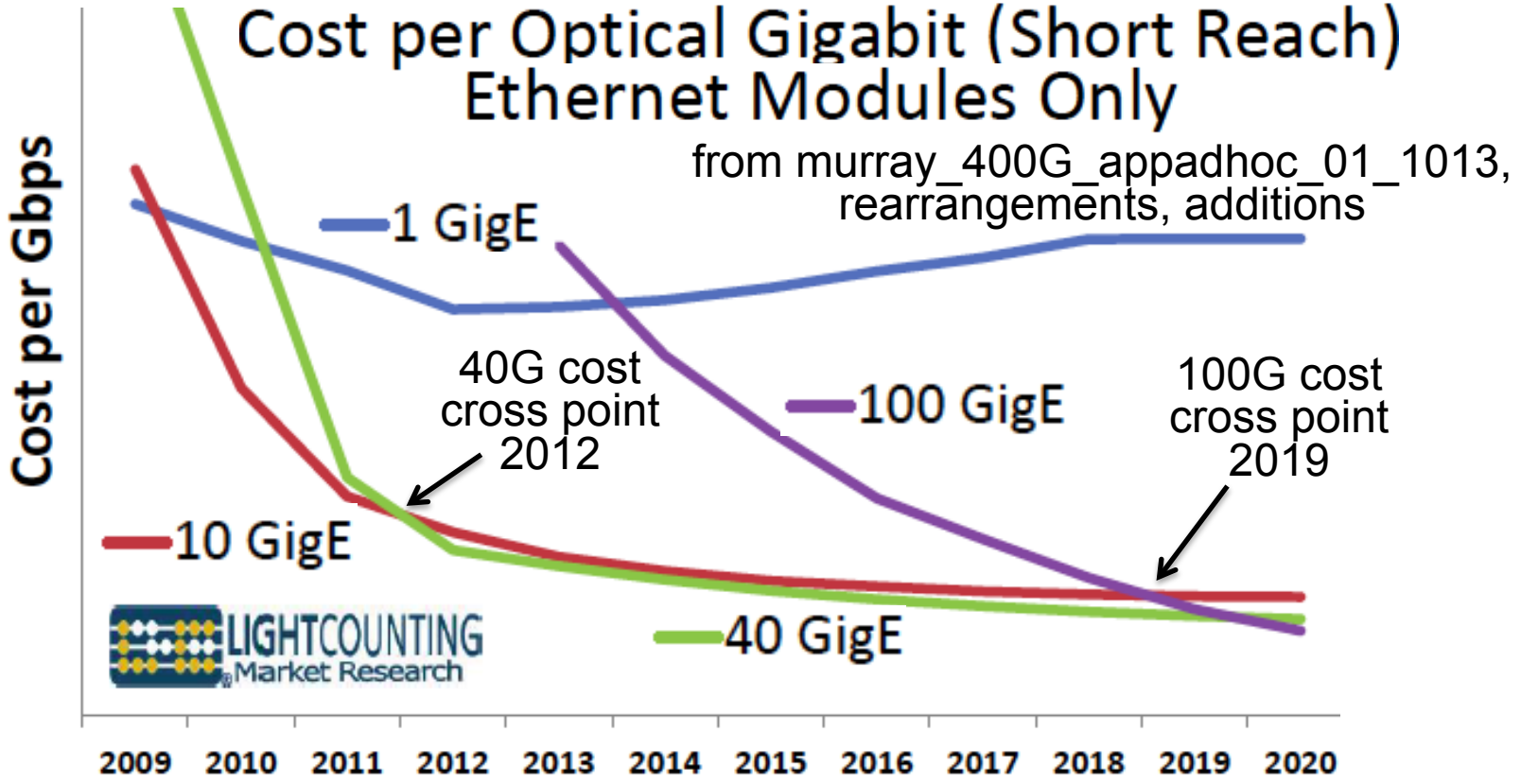
Courtesy, Mark Bugg, Molex

Economic Feasibility

- 100GBASE-SR4 is lowest-total-cost optical 100GbE
  - Lowest power consumption
    - Lowers OpEx
  - Easiest to package in smallest available form, saving switch real estate
    - Compounds CapEx savings: transceivers plus switch chassis
- Multiplying -SR4 cost by 4 is worst case for Gen 1
  - Applies to simply using 4×100G-SR4 (e.g. 4 QSFPs)
- Integration into new form factor will lower cost substantially
  - Number of housings, ICs, PCBs reduced 75%
  - Handling and alignment steps reduced 75%

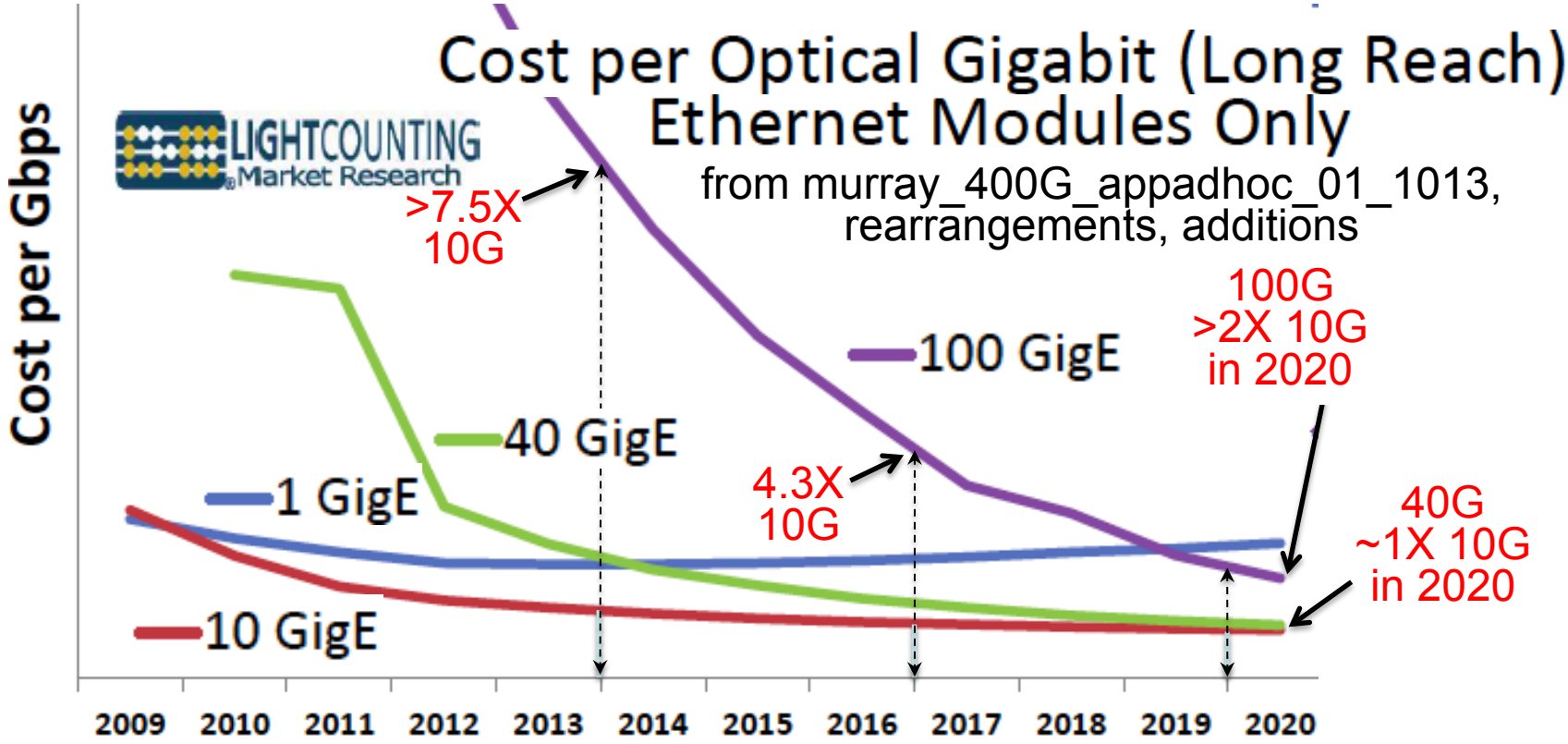
Economic Feasibility (SR)

- **SR** - Cost/Gbps already lower for 40GbE than 10GbE
- **SR** – Cost/Gbps decreasing for 100GbE as volume ramps
  - Upcoming Fibre-Channel 128GFC = 4 x 32GFC may accelerate cost reduction
- Cost/Gbps driven by volume and product simplicity
- 40G cost reduction accelerated by breakout function



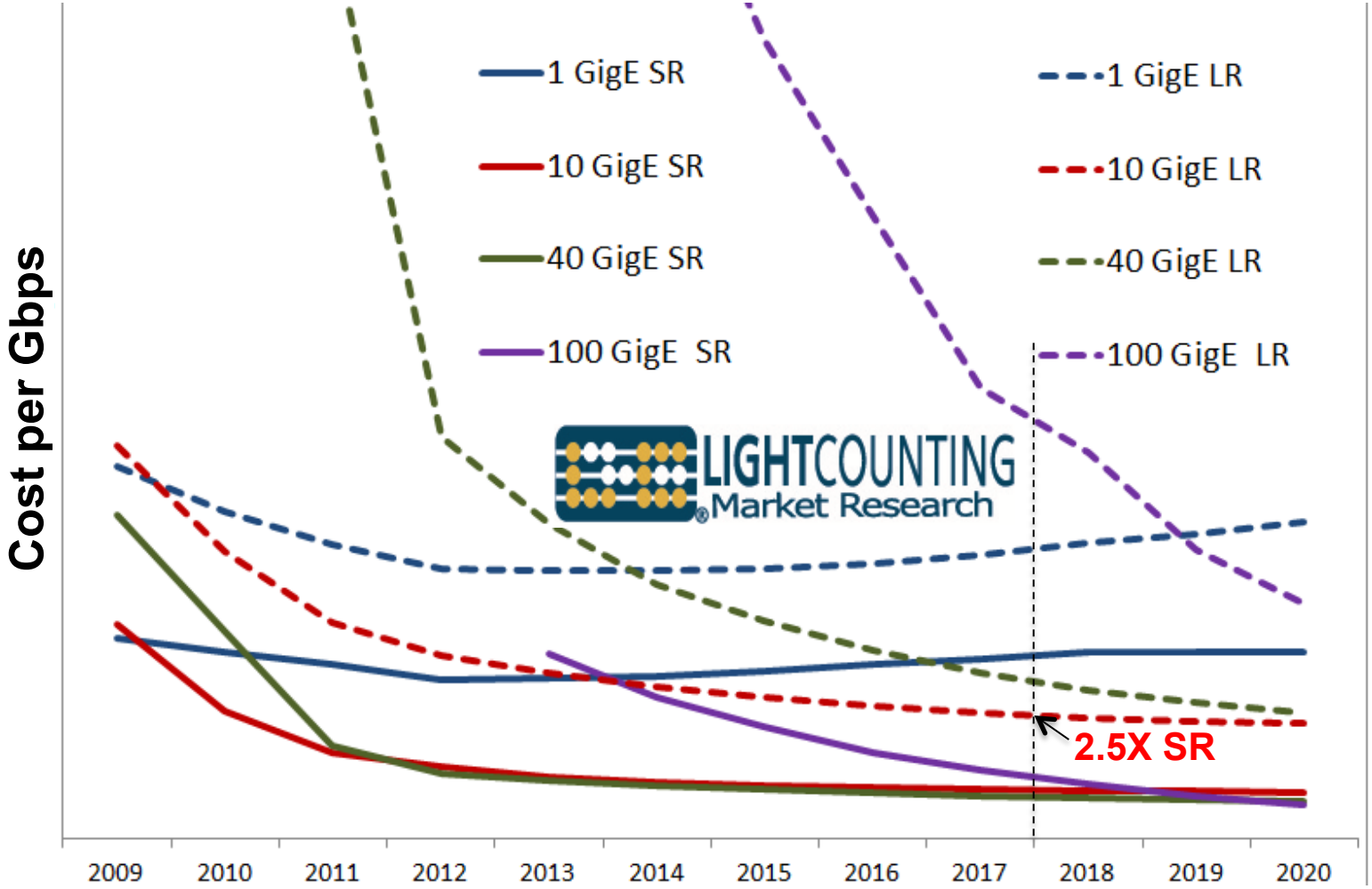
Economic Feasibility (LR Comparison)

- **LR** - Cost/Gbps HIGHER for 40/100GbE than 10GbE thru 2020
- Underscores long-term need for lower-cost SR modules (addresses economic feasibility and broad market potential)



Economic Feasibility (LR/SR Combined)

- SR provides short-reach interconnections at <u>much</u> lower cost
  - ~2.5X asymptotic ratio of 10G LR/SR module Gbps module costs
  - chart courtesy Dale Murray, LightCounting Market Research, rearrangements



5 Criteria Summary

- Compatibility
  - Compatible with IEEE 802.3 standard, 802.3 MAC, …
- Distinct Identity
  - Unique 16-lane x25G 400Gb/s PHY for operation over MMF
- Broad Market Potential
  - SR = highest-volume optical ethernet product – past and future
  - Straightforward breakout functionality to 4x100GbE (4x100G-SR4)
- Technical Feasibility
  - 400G-SR16 would ~replicate 100G-SR4 technology/specs
  - All technical aspects in place or undergoing standard/MSA process
- Economic Feasibility
  - SR = lowest-cost optical ethernet product – past and future
  - Simple increased channel count follows successful economic trend

Timeliness and Effort

- 100G-SR4 in late stages of definition in 802.3bm
  - 400G-SR16 would ~replicate 100G-SR4 specs
  - Details of 100G-SR4 still “fresh” in our minds
- Defining 400G-SR16 most efficient now, as opposed to “dredging up” 100G-SR4 specs later, and dealing with “spec-methodology evolution”
  - Defining 40GbE and 100GbE simultaneously (same spec methodology) over the same reaches made the job easier: Tables 86-6 and 86-8 (802.3ba) show common specs for 40/100 GbE
- MPO-16 TIA standard expected ~Nov 2015 (well before 400GbE)
- CDFP MSA completion expected before 400GbE

Timeliness and Effort

802.3ba-2010 - # channels makes negligible difference in specs for same reach

Reasonably expect [100G-SR4 specs = 400G-SR16 specs]

DO IT NOW

86.7.1 Transmitter optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical transmitter shall meet the specifications of Table 86–6 per the definitions in 86.8.

Table 86–6—40GBASE–SR4 or 100GBASE–SR10 optical transmit characteristics

Description	Type	Value	Unit
Center wavelength	Range	840 to 860	nm
RMS spectral width[a]	Max	0.65	nm
Average launch power, each lane	Max	2.4	dBm
Average launch power, each lane	Min	–7.6	dBm
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Optical Modulation Amplitude (OMA), each lane	Min	–5.6[b]	dBm
Difference in launch power between any two lanes (OMA)	Max	4	dB
Peak power, each lane	Max	4	dBm
Launch power in OMA minus TDP, each lane	Min	–6.5	dBm
Transmitter and dispersion penalty (TDP), each lane	Max	3.5	dB
Extinction ratio	Min	3	dB
Optical return loss tolerance	Max	12	dB
Encircled flux[c]		≥ 86% at 19 μm, ≤ 30% at 4.5 μm	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5×10^{-5} hits per sample	Spec values	0.23, 0.34, 0.43, 0.27, 0.35, 0.4	
Average launch power of OFF transmitter, each lane	Max	–30	dBm

[a] RMS spectral width is the standard deviation of the spectrum.
[b] Even if the TDP < 0.9 dB, the OMA (min) must exceed this value.
[c] If measured into type A1a.2 50 μm fiber in accordance with IEC 61280-1-4.

86.7.3 40GBASE–SR4 or 100GBASE–SR10 receiver optical specifications

Each lane of a 40GBASE–SR4 or 100GBASE–SR10 optical receiver shall meet the specifications defined in Table 86–8 per the definitions in 86.8.

Table 86–8—40GBASE–SR4 or 100GBASE–SR10 optical receiver characteristics

Description	Type	Value	Unit
Center wavelength, each lane	Range	840 to 860	nm
Damage threshold[a]	Min	+3.4	dBm
Average power at receiver input, each lane	Max	+2.4	dBm
	Min	–9.5	dBm
Receiver reflectance	Max	–12	dB
Optical Modulation Amplitude (OMA), each lane	Max	3	dBm
Stressed receiver sensitivity in OMA, each lane[b]	Max	–5.4	dBm
Peak power, each lane	Max	4	dBm
Conditions of stressed receiver sensitivity test:			
Vertical eye closure penalty (VECP)[c], each lane	—	1.9	dB
Stressed eye J2 Jitter[c], each lane	—	0.3	UI
Stressed eye J9 Jitter[c], each lane	—	0.47	UI
OMA of each aggressor lane	—	–0.4	dBm
Receiver jitter tolerance in OMA, each lane[d]	Max	–5.4	dBm
Conditions of receiver jitter tolerance test:			
Jitter frequency and peak-to-peak amplitude	—	(75, 5)	(kHz, UI)
Jitter frequency and peak-to-peak amplitude	—	(375, 1)	(kHz, UI)
OMA of each aggressor lane	—	–0.4	dBm

[a] The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
[b] Measured with conformance test signal at TP3 (see 86.8.4.7).
[c] Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver. The apparent discrepancy between VECP and TDP is because VECP is defined at eye center while TDP is defined with ±0.15 UI offsets of the sampling instant.
[d] This is a test of the optical receiver's ability to track low-frequency jitter and is inappropriate for any subsystem that does not include a CRU.

MMF Objective

“Define a 400 Gb/s PHY for operation up to at least 100m of MMF”

Closing Perspectives

- A 400GbE MMF Objective:
  - Continues Ethernet's highest-volume lowest-cost lowest-power highest-density optical technology: Short Reach MMF
    - –Large majority of optical Ethernet ports ever sold
  - Solidly satisfies the 5 Criteria
  - Is timely for this SG's anticipated Task Force project
  - Accommodates potential other SG objective(s)/desires regarding breakout functionality
- A specification based on 4×100G-SR4:
  - Is straightforward, requiring minimal resources
  - Would reference/borrow PMD specs from clause 95, 802.3bm
  - Would "Leverage 100GbE building blocks" per slide 38, 400G CFI

Thanks.
Q & A