Approved minutes
400Gb/s Ethernet Study Group Logic Ad hoc
Teleconference August 7th, 2013
Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:02 am Pacific chaired by Mark Gustlin, the attendee list was taken from the Webex attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

Mark reminded everyone of the IEEE meeting guidelines (https://development.standards.ieee.org/myproject/Public/mytools/mob/preparslides.pdf) and asked if anyone was unfamiliar with them. No one responded.

Meeting minutes from June 26 2013 were approved.

Presentation #1
Title: Error performance objective for 400GbE
By: Pete Anslow, Ciena
See: anslow_01_0813_logic.pdf

A question was asked about the times on slide 6 and if they were in reference to the interface rate or a lane rate, it was clarified that it was the 400G interface rate.

Some discussion around the fact that FLR is an unfamiliar term at least when used for objectives, might be useful to have a tutorial if we do end up with FLR in the objectives.

Some discussion around PHY vs. PMD for the BER/FLR objectives, it was clarified that PHY has a specific meaning in the protocol stack (it encompasses the PCS down to the PMD/AN sublayers).

The terminology of Frames vs. Packets was discussed, for the way Pete is using Frame it is correct.

It was asked why not use FLR for both FEC and non FEC PHYs, Pete responded that he preferred to use the more common BER terminology when possible (non FEC PHY).

A lot of discussion on what an appropriate BER target is and why based on different applications, it was suggested that if someone has a strong opinion on a particular BER/FLR target they should create a contribution stating the reasons.

Presentation #2
Title: 400GbE BER Objective From Perspective of MTTFPA
By: Wenbin Yang, Tongtong Wang, Haoyu Song, Huawei
See: song_01_0813_logic.pdf

It was asked if burst errors were included in the analysis, yes they were.

Attendees (taken from webex):

Mark Gustlin, Xilinx
Ghani Abbas, Ericsson
Xinyuan Wang, Huawei
Wenbin Yang, Huawei
Tongtong Wang, Huawei
Paul Mooney, Spirent
Xinyuan Wang, Huawei
Andy Moorwood, Infinera
Rick Rabinovich, Alcatel-Lucent
Tongtong Wang, Huawei
Andre Szczepanek, Inphi
Haoyu Song, Huawei
Pete Anslow, Ciena
Keisuke Kojima, Mitsubishi Electric
Herbert Endres, Molex
Steve Trowbridge, Alcatel-Lucent
Hugh Barrass, Cisco
David Ofelt, Juniper
Bert Klaps, Altera
Rich Mellitz, Intel
Mark Pilip, EZchip
Rick Rabinovich, Alcatel-Lucent
Mike Dudek, Qlogic
Steve Trowbridge, Alcatel-Lucent
John D'Ambrosia, Dell
David Law, HP
Randy Rannow, APIC
Brian Teipen, Adva
David Chalupsky, Intel
Rick Rabinovich, Alcatel-Lucent
Ali Ghiasi, Broadcom
Derek Cassidy, BT
Takeshi Nishimura, Yamaichi
CK Wong, FCI
Mark Gravel, HP
Li Zeng, Huawei
Mukund Kshirsagar, JDSU
Chris Cole, Finisar
Divya Vijayaraghavan, Altera
Pat Zabinski, Mayo Clinic
Stephen Bates, PMC-Sierra
Zhongfeng Wang, Broadcom