Approved minutes
400Gb/s Ethernet Study Group Logic Ad hoc
Teleconference August 20th, 2013
Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:02 am Pacific chaired by Mark Gustlin, the attendee list was taken from the Webex attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

Mark reminded everyone of the IEEE meeting guidelines (https://development.standards.ieee.org/myproject/Public/mytools/mob/preparslides.pdf) and asked if anyone was unfamiliar with them. No one responded.

Meeting minutes from August 07 2013 were approved.

Presentation #1
Title: 16 v 80 PCS Lanes for 400GbE, an implementer's perspective

By: Cedrik Begin, Gary Nicholl, Cisco

See: begin_01_0813_logic.pdf

On slide 7, show the PMA layer muxing also.

Another option on slide 9 is to just extend the length of the AMs to fill the available space.

It was pointed out that management of 80 PCS lanes is relatively complicated.

Presentation #2
Title: 400GbE PCS Architectural Requirements

By: Mark Gustlin – Xilinx, Chris Cole – Finisar, Pete Anslow – Ciena, John D'Ambrosia - Dell

See: gustlin_01_0813_logic.pdf

On slide 4 it was noted that a new PMD might require a new PCS.
Hugh had presented some slides on similar issues in the 40GBASE-T Task Force with the 802.3ba architecture.

FEC was brought up during the discussion on slide 5, in general FEC is not discussed in this slide set.

It was discussed that the chip-to-module interface on slide 6 might need FEC, for now could change the FEC to TBD at this point.

It was pointed out the designing a module to support both 10x40G and 8x50G lanes would make the module much more complicated. We need to see if technology hits a brick wall between 40G and 50 for VCSELs for instance. Some feel that this won't be the case.

On slide 8, this might be the where we define backplane, once we can do a 4 lane electrical interface.

For slide 9, change LR16 to 4LR4 for now to avoid confusion.

On slide 12, change to PAMn

Slide 18, collapse into a slide set that shows 10GE and 40GE in one.

On the summary slide, some discussion to drop CDAUI-10 unless a compelling use case is presented. There are options to also run 50G lanes slower for 40GbE applications for instance.

Presentation #3
Title: FEC/Architecture/Extender Sublayer

By: John D'Ambrosia - Dell

Some discussion on why 10GbE ended up with the extender sublayer.

Some discussion on slide 5 that RS-FEC is really a PCS layer in disguise.

On slide 7, should add the possibility of having multiple AUIs such as in the 802.3ba arch.
Draw diagrams with both ends of the link shown. Some discussion on if you can split the PCS functionality into multiple blocks.

D'Ambrosia to work on presentation for Sept. Invited those interested to contact him.

Attendees (taken from webex):
Tongtong Wang, Huawei
Jeff Slavick, Avago Technologies
Tongtong Wang, Huawei
Daniel Yang, Huawei
Masashi Kono, Hitachi
Tom McDermott, Fujitsu
Rick Rabinovich, Alcatel-Lucent
Patrick Zabinski, Mayo
Xinyuan Wang, Huawei
Keisuke Kojima, Mitsubishi Electric
Mark Gustlin, Xilinx
Andre Szczepanek, Inphi
Mark Pilip, EZchip

Piers Dawe, Mellanox
Herbet Endres, Molex
Paul Mooney, Spirent
Dale Murray, LightCounting
Cedrik Begin, Cisco
Pete Anslow, Ciena
Gary Nicholl, Cisco
Will Bliss, Broadcom
Mark Gravel, HP
Andy Moorwood, Infinera
Scott Irwin, MoSys Inc
Tom Palkert, Xilinx, Luxtera, Molex
Robert Wang, Intel
Andrew Zambell, FCI
Mike Dudek, Qlogic
John D'Ambrosia, Dell
Dave Brown, Semtech
Sam Sambasivan, AT&T
Michael Ressl, Hitachi Cable
Hugh Barrass, Cisco
Rich Mellitz, Intel
Jay Bhagat, Cisco
Vineet Salunke , Cisco
Ali Ghiasi, Broadcom
Michael Anstey,
Thananya Baldwin, Ixia
Dan Dove, Applied Micro
Tim Webster, Cisco
Chris Cole, Finisar
Jerry Pepper, Ixia
Thananya Baldwin, Ixia
Mike Li, Altera
Li Zeng, Huawei
Zhongfeng Wang, Broadcom
Ky Piper, Cisco
Mukund Kshirsagar, JDSU
Brian Teipen, Adva
Wheling Cheng, Juniper