Unapproved minutes
400Gb/s Ethernet Study Group Logic Ad hoc
Teleconference June 7th, 2013
Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:03 am Pacific chaired by Mark Gustlin, the attendee list was taken from the Webex attendee list.
Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml
Mark reminded everyone of the IEEE meeting guidelines (**https://development.standards.ieee.org/myproject/Public/mytools/mob/preparslides.pdf**) and asked if anyone was unfamiliar with them. No one responded.
Presentation #1
Title: 400GbE PCS Architectural Options
By: Mark Gustlin - Xilinx, Dave Ofelt – Juniper, Gary Nicholl – Cisco
See gustlin_adhoc_01_0613_400g.pdf
Some discussion on how necessary it is to start with 256b/257b encoding, vs. starting with 64b/66b and transcoding when needed.

Simple muxing is a misnomer in slide 5, it is not as simple as the original 802.3ba architecture since you have to find RS boundaries first.

A question about EEE impacts on the architecture options, could we do EEE in 100, 200, 300, 400G increments? Some discussion that this has been looked into in the past and you can save more power by shutting the whole interface down as needed.

A note that we do need to consider support for OTN and EEE in all of the architectural options.

It was noted that FEC options can impact any OTN interoperability.

John D'Ambrosia would like to see a liaison to the ITU out of the Ad hoc, Mark to work with Pete Anslow on this.

There was a lot of discussion about the merits of re-use from 100G to 400G. Some discussion around the fact that 80 pcs lanes is not a big burden, at least for devices that also support 4x100G.

Some questions about how to do Alignment Marker mapping, this needs to be figured out for many of the options.

Some questions were brought up about if we need lower than 25G rates, say 10G or 12.5G? We could add a slide about lower rates not being directly supported in the current proposals. Some were also not clear that 50G is easily supported with the proposed architectures, so make that more clear?

Agreed to add a slide that shows 80 PCS lane options also.

How to address 10x40GE, how does it relate to 400GbE?
And how does MLG fit into this architecture? Both of these can be categorized as inter-generational compatibility, these needs to be looked into in more detail.

Presentation #2
Title: Forward Error Correction for 400G: Initial Thoughts
By: Stephen Bates
See bates_adhoc_01_0613_400g.pdf
A lot of discussion on what FEC gain will be needed, what would a 50G electrical interface require, what will various PMDs require etc.
It was noted that there needs to be a lane muxing function on the receive before the RS-FEC if we want to support any logical lane on any physical lane.

It was noted that some of the PMDs shown are not correct, they should be 4:4 below a 802.3bj FEC for instance.

A big question, as noted in the slides is what latency target is acceptable.

It was noted that it would be good to get information on 50G optics error characteristics in order to understand how FEC might be used for such a PMD.

A lot of discussion on the possible straw polls listed on slide 14, any suggestions for rewording them should be sent to Stephen.

The meeting closed at 9:55 am Pacific.

Paul Mooney
Tomoo Takahara
Masashi Kono
Michael Ressl
Suping Zhai
WenbinYang
Martin Wendt
Tongtong Wang
Mark Gustlin
Ajay Dubey
John D'Ambrosia
Arlon Martin
Herbert Endres
Bert Klaps
Pete Anslow
Andrew Bown

Mike Manstay
Raman Venkat
Toshiki Tanaka
Galen Fromm
Ali Ghiasi
Brian Teipen
Raghu Rao
David Ofelt
Robert Wang
Scott Kipp
Tomoo Takahara
Wissen Zhang
Stephen Bates
Andy Moorwood
Xiaolu Song
Adam Healey
Hugh Barrass
Carl Paquet
Dave Brown
Rich Melitz
Jerry Pepper
Rick Rabinovich
Kyle Piper
Zeng Li
Martin Langhammer
Vineet Salunke
Dan Sparacin
Scott Humber
Jonathan King
Mike Dudek
Scott Irwin
Zhongfeng Wang
Terry Bowen
Jeff Slavick
Keisuke Kojima
Dmitri Varsanofiev
Katsuhisa Tawa
Ted Sprague
Vasu Parthasarathy
John Petrilla
David Chalupsky (Intel)
Wheling Cheng
Derek Cassidy

Andre Szczepanek