Unapproved minutes
400Gb/s Ethernet Study Group Logic Ad hoc
Teleconference October 23rd, 2013
Minutes taken by Mark Gustlin, Xilinx
The meeting started at 8:03 am Pacific chaired by Mark Gustlin, the attendee list was taken from the Webex attendee list.

Documentation for the call can be found at the Ad Hoc web page:
http://www.ieee802.org/3/400GSG/public/adhoc/logic/index.shtml

Mark reminded everyone of the IEEE meeting guidelines (https://development.standards.ieee.org/myproject/Public/mytools/mob/preparslides.pdf) and asked if anyone was unfamiliar with them. No one responded.

Meeting minutes from August 20 2013 were approved.

Presentation #1
Title: A 400GbE PCS Option

By: Mark Gustlin – Xilinx, Gary Nicholl – Cisco, Dave Ofelt – Juniper, Jerry Pepper – Ixia, Andre Szczepanek – Inphi, Tongtong Wang - Huawei

See: gustlin_01_1013_logic.pdf

There was a question on slide 5, do we need to descramble before transcoding, the answer was no, 802.3bj moved to not descrambling, instead removing the redundancy in the block type on tx and recovering it by running a shadow scrambler on the receiver to recover the redundant portion of the block type fields, this proposes the same thing.

On slide 10 the point was made that the 400G AMs are not really markers since we have everything we need to identify the 16 FEC lanes, but those 64b can be used for something else.

On slide 12, the PCS lanes should be FEC lanes.

On slide 13 there was a lot of discussion about why we would want to support 10 lanes…task force will need to decide this. Also it was suggested to clarify exactly what has to happen on the rx side of such an interface (block align, deskew and reorder before changing lane widths again).

Presentation #2
400GbE PCS Direct Coding Analysis - Haoyu Song

See: song_01_1013_logic.pdf

Slide ?, it was asked if the symbol rate is the same with and without FEC, yes, 4 extra stuff bits are added to make it so.

On slide 5 it was asked why go through the effort of supporting this extra mode, answer was lower latency and to support cases where FEC is not needed.

On slide 9 it was pointed out that if you used a 544,520 code at 400G, then the size will go up for any designs that need to support both 4x100G and 1x400G.

On slide 10 it was questioned if 256/260 can cope with burst errors, answer is likely no.

On slide 11 a question was asked about the distribution of the blocks to lanes, it is noted earlier in the presentation that it is proposed to still be 10b blocks, follow up question is if there will be MTTFPA issues given scrambler interactions?

Presentation #3
Title: Error performance objective for 400GbE

By: Pete Anslow – Ciena

See: anslow_01_1013_logic.pdf

A lot of discussion on slide 9: it was asked why specify only a single BER related objective, answer is to simplify and not cause confusion or controversy in the working group (by prejudging a solution), while giving the task force the needed flexibility.
Some discussion around what this higher BER means to re-use of existing PMDs, Pete does not believe it will be a challenge, with applying FEC as one possible solution.
Much discussion about a BER vs. FLR specification and the fact that the FLR statement was not explicit in the objective, Pete has added the details to the proposed objective now.

Attendees (taken from webex, please let me know if you have a correction):
Mark Gustlin, Xilinx
Rick Rabinovich, Alcatel-Lucent
Paul Mooney, Spirent
Xinyuan Wang, Huawei
Ghani Abbas, Ericsson
Dan Sparacin, Aurrion
Tongtong Wang, Huawei
Xinyuan Wang, Huawei
Shamim Akhtar, Comcast
Mark Pilip, EZchip
Tom McDermott, Fujitsu
Masashi Kono, Hitachi
Steve Trowbridge, Alcatel-Lucent
Haoyu Song, Huawei
Andy Moorwood, Infinera
Piers Dawe, Mellanox

Bert Klaps, Altera
Pi Boson, ?
Ali Ghiasi, Independent
Xinyuan Wang, Huawei
Scott Irwin, MoSys Inc
Pete Anslow, Ciena
Michael Anstey,
Larry Tarof, Optelian
Stephen Bates, PMC-Sierra
CK Wong, FCI
Nathan Tracy, TE Connectivity
Alex Umnov, Fujitsu
Jim Theodoras, Adva
Jeff Slavick, Avago Technologies
R. Wood, Altera
Robert Wang, Intel
Matt Brown, Applied Micro
Hugh Barrass, Cisco
Mike Dudek, Qlogic
Velu Pillai, Broadcom
David Law, HP
Mike Li, Altera
Daniel Yang, Huawei
Satoshi Tsutsumi, Hitachi
Vineet Salunke , Cisco
Dan Dove, Applied Micro
Daniel Kucharski, Semtech
David Chalupsky, Intel
Rich Mellitz, Intel
Mark Gravel, HP
Xinyuan Wang, Huawei
Jerry Pepper, Ixia
Gary Nicholl, Cisco
Rich Mellitz, Intel
Jonathan King, Finisar
Zhongfeng Wang, Broadcom
Norm Swenson, ClariPhy
Jeffery Maki, Juniper
Ky Piper, Cisco
Cedrik Begin, Cisco
Adam Healey, LSI Corporation
Martin Langhammer, Altera
Keisuke Kojima, Mitsubishi Electric