Power Matters

IEEE802.3 4P Task Force

PSE PI pair to pair voltage difference

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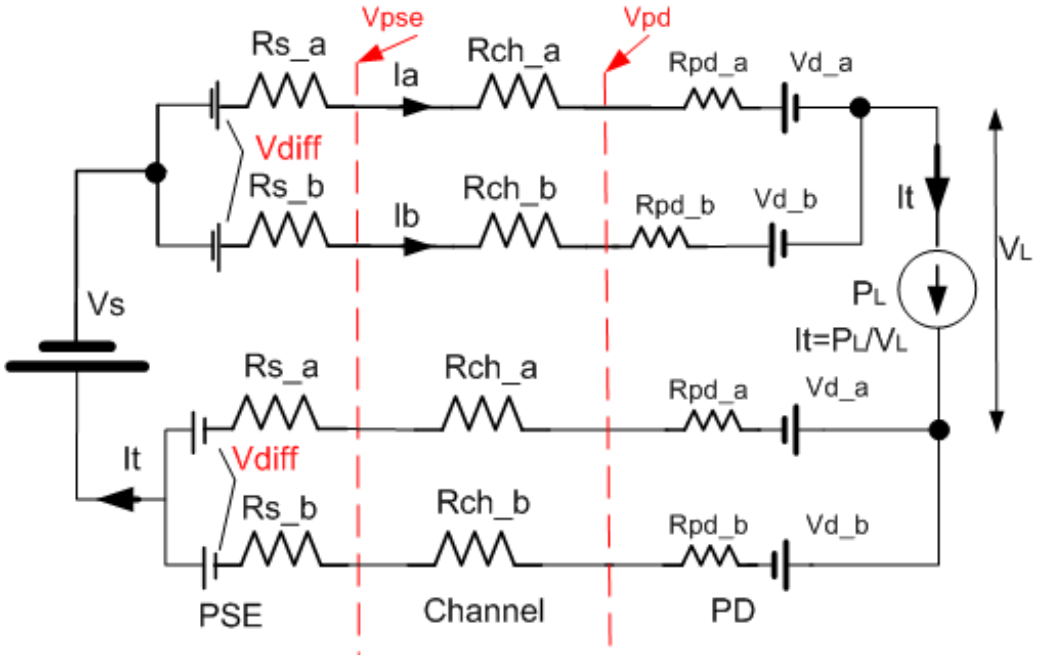
Terms

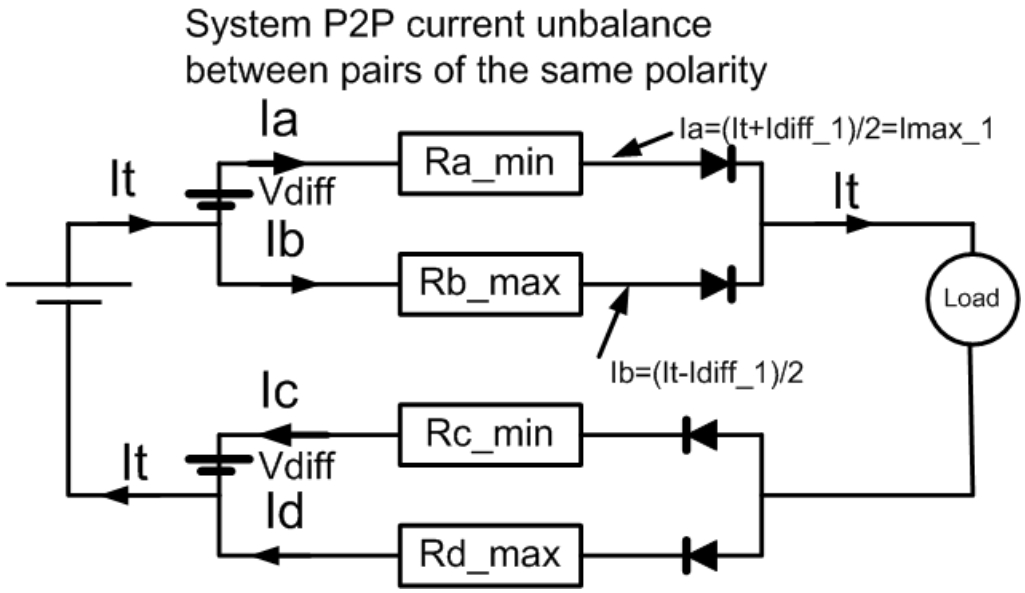
- PSE PI pair to pair voltage difference. The voltage difference between pairs of the same polarity.
  - Pair to pair voltage difference is a major contributor for overall system unbalance especially at short channel length.



- PD diode voltage differences Vd_a, Vd_b.
- PSE P2P voltage differences is described by Vdiff.

Objectives

- To propose base line text for Type 3 and 4 for the maximum pair to pair voltage difference.
  - It will allow us to:
    - Reduce and control worst case system unbalance
    - Help moving design margins to PD were it needed most



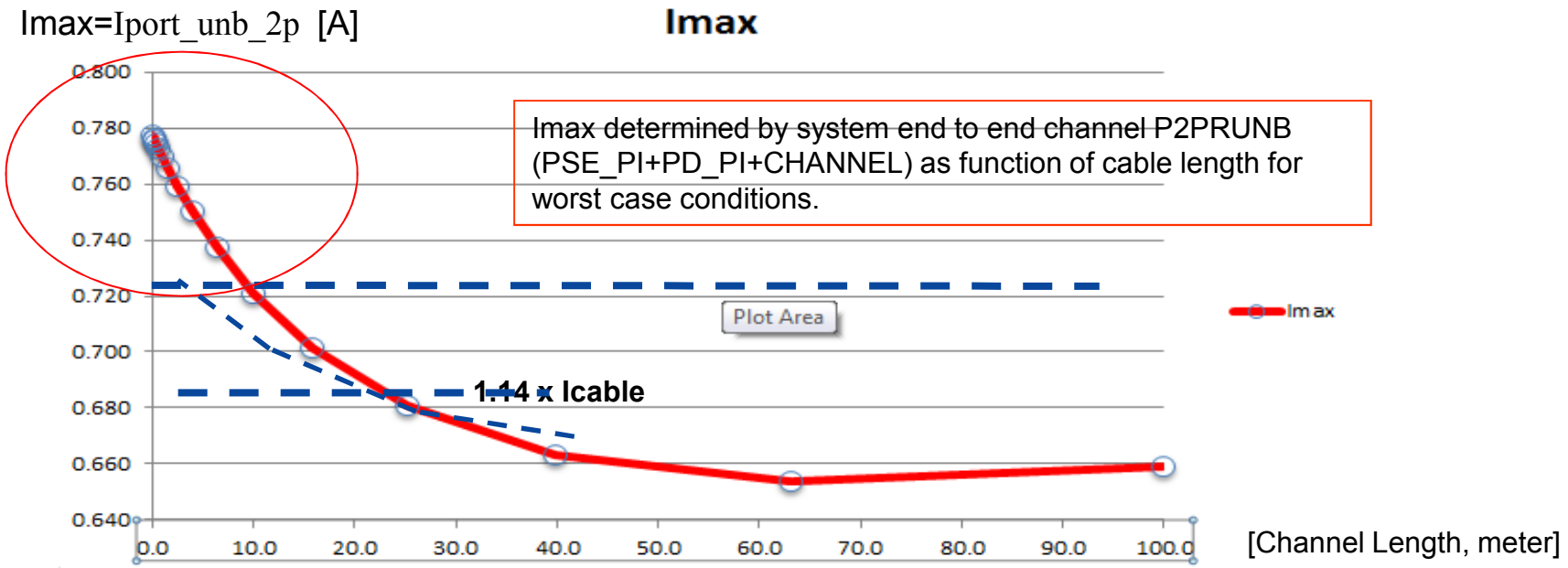
Further simplifying.
Each diode: 2xVd

History

- It was show in many presentations (see Ref1 and others) that voltage difference between pairs of the same polarity, affects system current unbalance.
- We had recommendations at the E2ECP2PRUNB adhoc group and in the room to specify the pair to pair voltage difference as one of the other unbalance parameters.
- The following curve shows worst case pair maximum current as function of channel length as a result of P2P voltage difference at PSE PI (0.1V) and PD PI (0.1V).

Proposed Imax vs. Worst case system End to End CP2PRUNB

- Pair to Pair Voltage Difference: **PSE Vdiff=0.1V. Pd Vdiff =0.1V**
- The 0.78A current value is a result of PSE PI and PD PI Vdiff.
- Maximum Current will drop to <720mA if PSE Vdiff will be <<0.1V e.g. few mV.
- Below (red curve) is the maximum pair current in the presence of end to end channel P2PRUNB of with worst case Rmax/Rmin AND Vdiff per table G1 from September 2014 adhoc report.
- The red circle area is controlled by specifying PSE PI and PD PI unbalance parameters, mainly Vdiff at short channel length.



Proposal

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1.1	Output voltage pair to pair difference of pairs with the same polarity in the POWER_ON state	VPort_PSE_diff	mV		TBD	3,4	Open load voltage. Test setup: TBD.

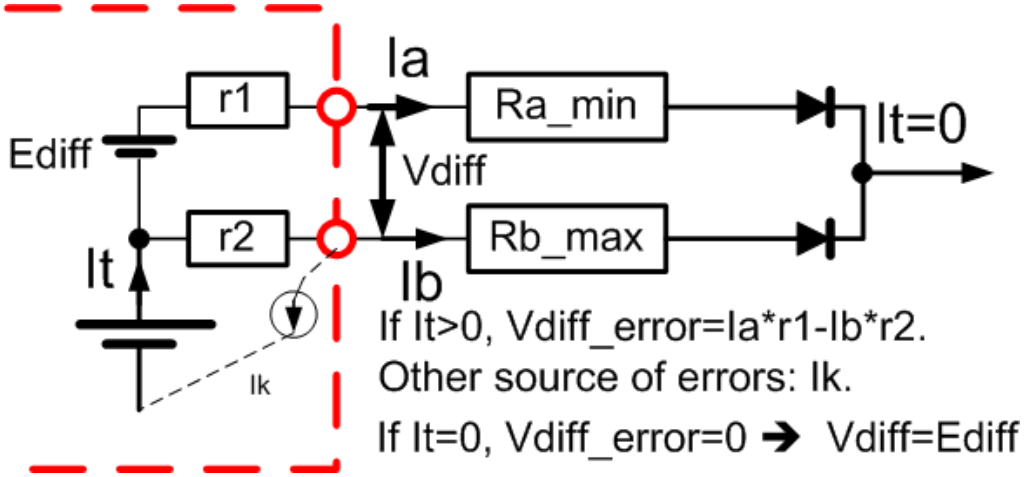
- Why mV range? (See FAQ-3).
  - Easy to get with exiting PSE PI components accuracies and difference.
  - Guarantee avoiding undesired PSE configurations that it is hard to ensure proper current balance for not affecting transformers performance.
  - *It may be too tight for AC disconnect implementation. Group to decide. Therefore TBD.*
    - *My recommendation is, very low Vdiff in PSE as much as possible has high priority. I twill not prevent implementing AC Disconnect , it will require tight diode matching*
- Why testing at NO LOAD or very low load current?
  - See next FAQ slides.

FAQ - 1

- Why specifying Vdiff in positive pairs and negative pairs and not only on the pairs where current is measured?
  - Vdiff affects unbalance at low current at short and long cables.
  - Vdiff affects unbalance at high current at short cables.
  - Transformers are affected by Unbalance
  - Transformers are located in all pairs.
  - Therefor Vdiff need to be specified for all pair sof the same polarity.

FAQ - 2

- Why Vdiff is best to be specified at No load?
  - To eliminate the error that Vdiff is increased in PSE PI due to current flow through PSE PI output resistance that are unbalanced and creates Vdiff which will not affect system current unbalance.
  - We need the Thevenin Vdiff equivalent.
  - Since the PSE chip may have internal circuitry that draws current across the port, Vdiff can not be zero and when measured for compliance, hence a minimum value need to be specified + design margin that will generate the maximum value.



FAQ – 3 What is the expected PSE Vdiff

- It need to be much less from what we allow for the PD Vdiff.
- It shouldn’t be >10mV
- 2mV is considered
- We are waiting for PSE Vendors to send their Vdiff measured at PSE PI at positive pairs and negative pairs at no load conditions or at 10mA load so we can make sure that the standard will support know 4P implementations

Reference Material

ANNEX C: Example for Existing PSE PD PI P2PRUNB Source: (*). PSE PI Vdiff=0.

- Reqv=The resistance equivalent caused by P2P voltage difference on the E2E_C_P2PRUNB
- Rd_eqv=The resistance equivalent caused by PD diode voltage difference and Diode dynamic resistance difference
- The following example is with PSE PI Vdiff=0.

	PSE PI POS								
	Traces	Rt	Rc			Reqv	Sum	Rdiff	P2PRUNB
Rmin [ohm]	0.01	0.12	0.03			0	0.16	0.031	8.83%
Rmax [ohm]	0.011	0.13	0.05			0	0.191		
	PSE PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Reqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0.098	0.05/0.099	0	0.308/0.357	0.083/0.034	11.87%/4.55%
Rmax	0.011	0.13	0.05	0.1	0.1/0.1	0	0.391/0.391		
	PD PI POS								
	Traces	Rt	Rc			Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03			0.25	0.41	0.281	25.52%
Rmax	0.011	0.13	0.05			0.5	0.691		
	PD PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0	0	0.25	0.41	0.281	25.52%
Rmax[ohm]	0.011	0.13	0.05	0	0	0.5	0.691		

(*) http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf

Annex D: Example for Existing PSE PD PI P2PRUNB
Source: (*). PSE PI Vdiff>0.

- Reqv=The resistance equivalent caused by P2P voltage difference on the E2E_C_P2PRUNB
- Rd_eqv=The resistance equivalent caused by PD diode voltage difference and Diode dynamic resistance difference
- The following example is with PSE PI Vdiff>0. P2PRUNB=(Rmax-Rmin)/(Rmax+Rmin)

	PSE PI POS								
	Traces	Rt	Rc			Reqv	Sum	Rdiff	P2PRUNB
Rmin [ohm]	0.01	0.12	0.03			0	0.16	0.131	29.05%
Rmax [ohm]	0.011	0.13	0.05			0.1	0.291		
	PSE PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Reqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0.098	0.05	0	0.308	0.183	22.90%
Rmax	0.011	0.13	0.05	0.1	0.1	0.1	0.491		
	PD PI POS								
	Traces	Rt	Rc			Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03			0.25	0.41	0.281	25.52%
Rmax	0.011	0.13	0.05			0.5	0.691		
	PD PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0	0	0.25	0.41	0.281	25.52%
Rmax[ohm]	0.011	0.13	0.05	0	0	0.5	0.691		

(*) http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf

Annex E: Example for Existing PSE PD PI P2PRUNB Source: (*). PSE PI Vdiff=0, PD Match diodes.

- Reqv=The resistance equivalent caused by P2P voltage difference on the E2E_C_P2PRUNB
- Rd_eqv=The resistance equivalent caused by PD diode voltage difference and Diode dynamic resistance difference
- The following example is with PSE PI Vdiff=0 and PD using matched diodes. With ideal diode bridge PDE PI P2PRUNB may be a bit higher due to lower resistance and process.

	PSE PI POS								
	Traces	Rt	Rc			Reqv	Sum	Rdiff	P2PRUNB
Rmin [ohm]	0.01	0.12	0.03			0	0.16	0.031	8.83%
Rmax [ohm]	0.011	0.13	0.05			0	0.191		
	PSE PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Reqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0.098	0.05/0.099	0	0.308/0.357	0.083/0.034	11.87%/4.55%
Rmax	0.011	0.13	0.05	0.1	0.1/0.1	0	0.391/0.391		
	PD PI POS								
	Traces	Rt	Rc			Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03			0.225	0.385	0.056	6.78%
Rmax	0.011	0.13	0.05			0.25	0.441		
	PD PI NEG								
	Traces	Rt	Rc	Rsense	RDSon	Rd_eqv	Sum	Rdiff	P2PRUNB
Rmin[ohm]	0.01	0.12	0.03	0	0	0.225	0.385	0.056	6.78%
Rmax[ohm]	0.011	0.13	0.05	0	0	0.25	0.441		

(*) http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf

Annex G1:Worst Case Data Base. See Ref 1.

#	Parameter	Data set 1	Data set 2
1	Cordage resistivity[1]	0.14Ω/m	
		0.09262Ω/m for AWG#24 for worst case analysis	
2	Horizontal cable resistivity option 1[2]	11.7Ω/100m=(12.5Ω - 4*0.2Ω) / 100m which is the maximum resistance resulting with maximum Iport.	7.4Ω/100m to 7.92Ω/100m (CAT6A, AWG23) This is to give us maximum P2PRunb
3	option 2[3]	0.098Ω/m.	
4	Unbalance parameters	• Cable Pair resistance unbalance: 2%. Channel pair resistance unbalance: 3% • Cable P2P Resistance Unbalance: 5%. Channel P2P Resistance Unbalance: 0.2Ω/6% max TBD.	
5	Channel use cases to check. See figure 1 for what is a channel.	A. 6 inch (0.15 m) of cordage, no connectors. B. 4 m channel with 1 m of cordage, 3 m of cable, 2 connectors C. 23 m channel with 8 m of cordage, 15 m of cable, 4 connectors D. 100m channel with 10 m of cordage, 90 m of cable, 4 connectors	
6	End to End Channel[6]	The Channel per figure 1 + the PSE and PD PIs.	
7	Transformer winding resistance	120mOhm min, 130mOhm max	
8	Connector resistance[8]	40mOhm min, 60mOhm max	30mOhm min, 50mOhm max
9	Diode bridge[9]	Discreet Diodes: 0.39V+0.25Ω*Id min; 0.53V+0.25Ω*id max. (TBD)	
10	PSE output resistance [10]	0.25+0.1 Ohm min, 0.25+0.2 Ohm max	0.1+0.05 Ohm min, 0.1+0.1 Ohm max

Ad-hoc response, June 24, 2014. Adhoc accept this table

Source: Yair Darshan, Christian Beia, Wayne Larsen

#	Reference	Notes
1	http://www.ieee802.org/3/bt/public/sep14/darshan_01_0914.pdf	Adhoc
2	http://www.ieee802.org/3/bt/public/unbaladhoc/Channel%20Pair%20To%20Pair%20Resistance%20Unbalance%20Specification-What%20is%20the%20preferred%20concept.pdf	comparision
3	http://www.ieee802.org/3/bt/public/unbaladhoc/PI%20Balance%20Specifications%20rev%202.pdf	PSE PI spec.
4	http://www.ieee802.org/3/bt/public/unbaladhoc/Analzing_Channel_Pair_To_Pair_Resistance_Unbalance_use_cases_rev_6.1.pdf	Channel spec
5	http://www.ieee802.org/3/4PPOE/public/nov13/darshan_02_1113.pdf	Thermal
6	http://www.ieee802.org/3/bt/public/sep14/darshan_02_0914_rev%20002.pdf	PSE PI spec.