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HUAWEI ENTERPRISE A BETTER WAY

Backfeed in a 4-pair context

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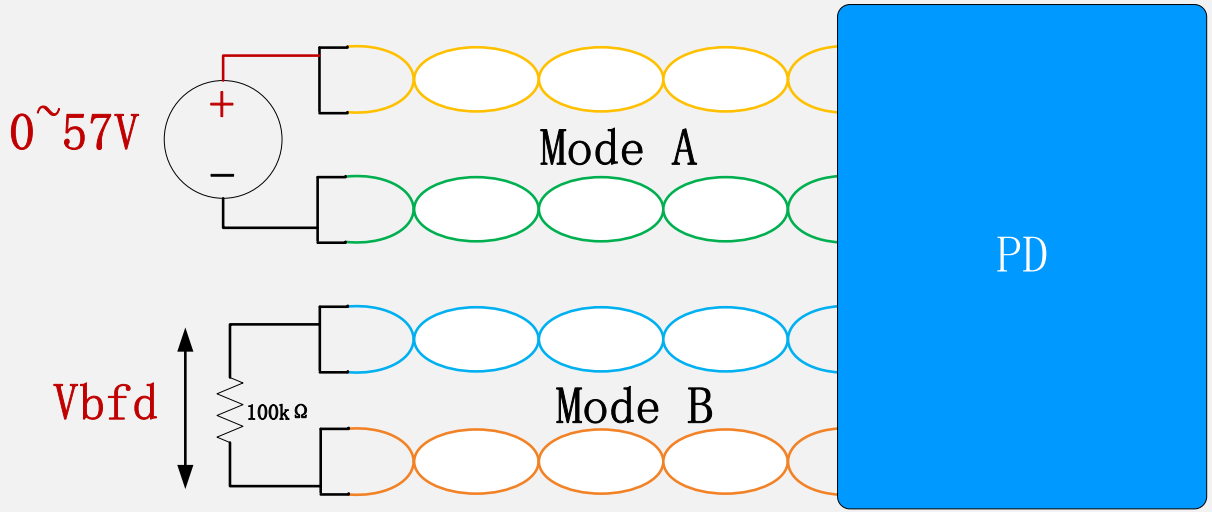
Overview of Backfeed

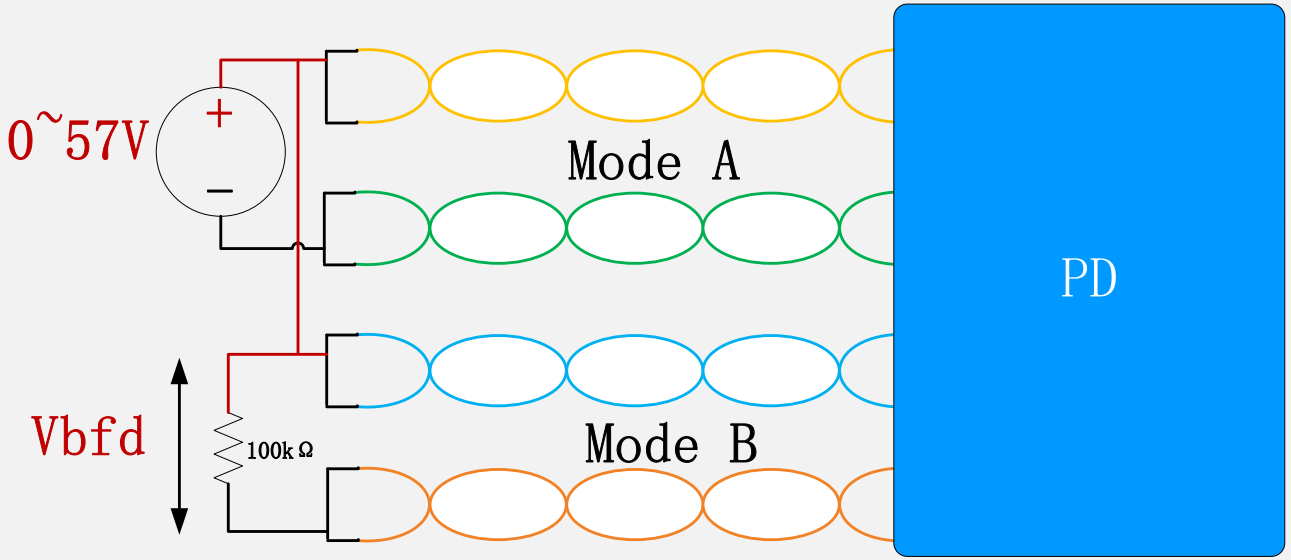
IEEE_P8023bt_DRAFT_3p4 145.3.8.8 Backfeed voltage

“When any voltage in the range of 0 V to VPort_PD-2P max is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 145–20, the voltage measured across the PI for the other Mode with a 100 kΩ load resistor connected across that other Mode shall not exceed Vbfd as defined in Table 145–29.”



4-pair backfeed

A 4-pair capable PSE typically ties the positive lines together at the PSE end. Even in “2-pair” mode, there are two pairs connected to the positive VPSE.



Text change for voltage

Change 145.3.8.8 (backfeed_d3baselinep4.pdf , version v230)as follows:

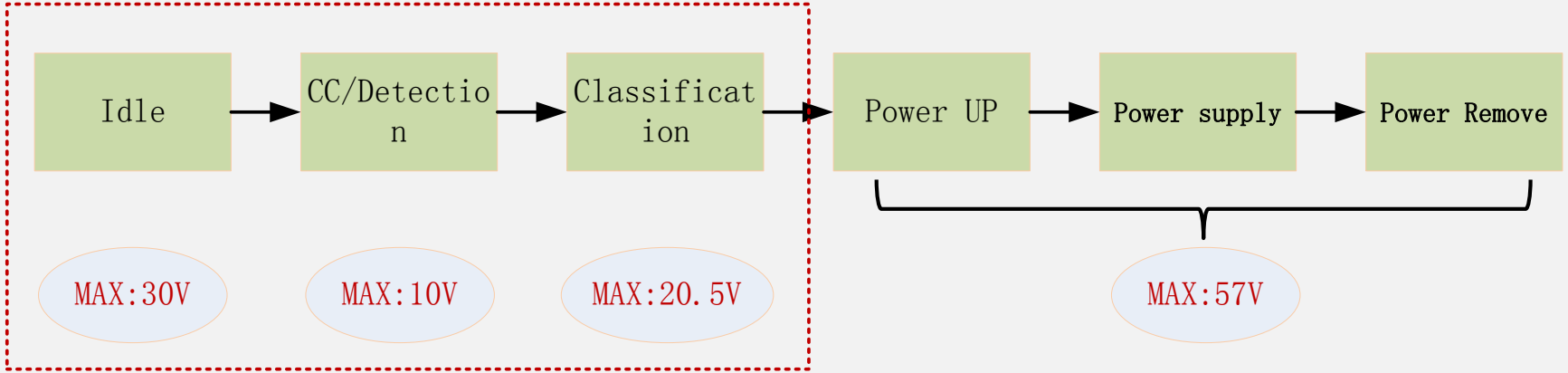
For a single-signature PD, when any voltage in the range of 0V to VPort PD-2P max is applied per any of the valid 2-pair configurations, defined in Table 145–20, that have only a single pair connected to positive VPSE, the voltage on the Mode not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed Vrefl as defined in Table 145–29.

For a single-signature PD, when any voltage in the range of 0V to ~~10.1V~~ 21Vis applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive VPSE, the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed Vrefl as defined in Table 145–29.

For a dual-signature PD, when any voltage in the range of 0V to VPort PD-2P max is applied per any of the valid 2-pair configurations, defined in Table 145–20, including those with two pairs connected to positive VPSE, the voltage on the Mode with at least one pair not connected to the voltage source, with a 100 kΩ resistor connected across that Mode, shall not exceed Vrefl as defined in Table 145–29.

The reason to change to 21V

Vrefl should not affect processes before power up



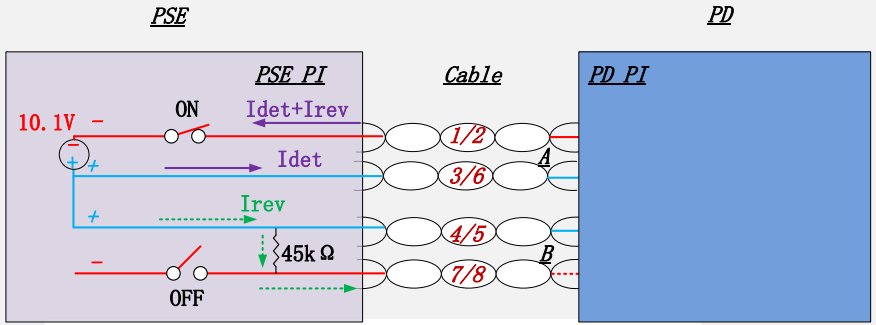
Vrefl's effect on detection

Vrefl will lead to Zsource parallel to Rsig.

Rsig=19kΩ is Accept signature resistance. Rsig in parallel to Zsource is Reject signature resistance

19KΩ*45KΩ/(19kΩ+45KΩ)=**13.359kΩ → Reject signature resistance**

Solution: The voltage for single-signature PD should be **at least 10.1V**



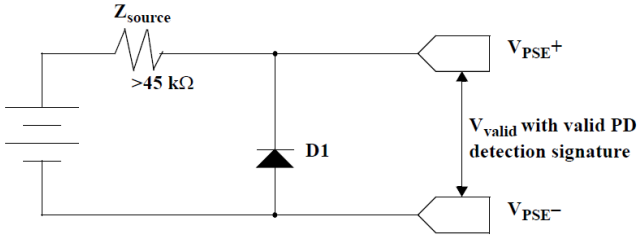


Figure 145–19—PSE detection source

Table 145–8—Valid PD detection signature electrical characteristics, as measured at the PSE PI

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19	26.5	—

Table 145–9—Invalid PD detection signature electrical characteristics, as measured at the PSE PI

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15	33	—

Vrefl's effect on classification

Classification current may be changed by 20.5V/45kΩ=0.456mA (or Irev), which requires higher accuracy measurement.

The margin between class 0 to class 1 and class 1 to class 2 will be reduced to 2.544mA(3mA-0.5mA=2.5mA)

Solution: The voltage for single-signature PD should be **at least 21V**. (preferred 30V, to be discussed)

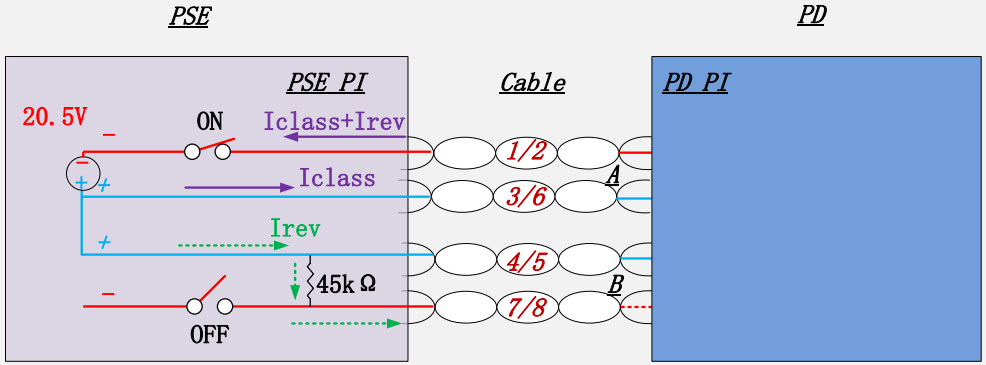


Table 145–13—Class signatures evaluated at the PSE PI

Measured I_{Class}	Class signature
0 mA to 5 mA	Class signature 0
> 5 mA and < 8 mA	Either class signature 0 or 1
8 mA to 13 mA	Class signature 1
> 13 mA and < 16 mA	Either class signature 1 or 2
16 mA to 21 mA	Class signature 2
> 21 mA and < 25 mA	Either class signature 2 or 3
25 mA to 31 mA	Class signature 3
> 31 mA and < 35 mA	Either class signature 3 or 4
35 mA to 45 mA	Class signature 4
> 45 mA and < 51 mA	Either class signature 4 or invalid class signature

Thank you!