

1 Comment (clause 33.3.3.12 #251 page 130 line 24)

2 The following changes are required in the dual-signature PD variable list in clause
3 33.3.3.12 and in the dual-signature Type 3 and 4 PD state machines Figure 33-33
4 and Figure 33-34:

- 5 1. The exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138
6 should be update according to the exits in Figure 33-32 page 129 with the
7 prefix `_modeA` and `modeB`.
- 8 2. There is no need for `DLL_ENABLE_modeA/B` due to the fact that if DLL is
9 enabled, it is done for all powered pairs.
- 10 3. There is also no need for `pd_dll_enable_modeA` and `pd_dll_enable_modeB`
11 due to the fact that if DLL is enabled, it is done for all powered pairs.
- 12 4. In figure 33-33, `DO_CLASS_EVENT5` and `DO_MARK_EVENT4` is missing the
13 suffix "`_modeA`".
- 14 5. In figure 33-34, `DO_CLASS_EVENT5` and `DO_MARK_EVENT4` is missing the
15 suffix "`_modeB`".
- 16 6. To verify that all changes will be in sync with Figure 33-50.

17
18 **See "OPTION A" suggested remedy for reference in the next pages.**

- 19
20 7. Consider to further simplifying the whole dual-signature state machine and
21 its constant, variable, timers and functions starting at page 129 up to page
22 138 by doing the following actions:

23 All constants, variables, timers and functions that ends with the suffix `_modeA` i.e.
24 `parameter_name_modeA` (e.g. `pd_req_class_modeA`) will be change to
25 `parameter_nameY` where the suffix "`Y`" will be "`A`" or "`B`".

- 26 a) All constants, variables, timers and functions that ends with the suffix
27 `_modeB` will be deleted.
- 28 b) Figure 33-33 will be updated with the new suffix "`Y`".
- 29 c) Figure 33-34 will be deleted.

30
31 **See "OPTION B" suggested remedy for reference in the next pages.**

32
33
34 **Baseline starts at next page:**

1 Suggested Remedy –Option A

2 Make the following changes:

3 33.3.3.11 Type 3 and Type 4 dual-signature constants

4 **This is not part of the base line**

Work need to be done to verify that single signature and dual-signature state machine and their variable list are sync with DLL state machines Figure 33-49 and Figure 33-50.

5
6 *Editor Note: DLL PSE and PD power control state diagram (Figure 33-49 and Figure 33-50) need to be evaluated and sync with the single signature and dual-signature PD state machine.*

7
8
9 The PD state diagram uses the following constants:

10 VReset

11 Reset voltage per pairset (see Table 33–26)

12 VReset_th

13 Reset voltage threshold per pairset (see Table 33–26)

14 VMark_th

15 Mark event voltage threshold per pairset (see Table 33–26)

16
17 pd_req_class_modeA

18 A constant indicating the requested Class of the PD over mode A.

19 Values:

- 20 1: The PD requests Class 1.
- 21 2: The PD requests Class 2.
- 22 3: The PD requests Class 3.
- 23 4: The PD requests Class 4.
- 24 5: The PD requests Class 5.

25
26 pd_req_class_modeB

27 A constant indicating the requested Class of the PD over mode B.

28 Values:

- 29 1: The PD requests Class 1.
- 30 2: The PD requests Class 2.
- 31 3: The PD requests Class 3.
- 32 4: The PD requests Class 4.
- 33 5: The PD requests Class 5.

34 35 33.3.3.12 Type 3 and Type 4 dual-signature variables

36 The PD state diagram uses the following variables:

37
38 mdi_power_required_modeA

39 A control variable indicating that over mode A, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:

- 40 FALSE:PD functionality is disabled.
- 41 TRUE:PD functionality is enabled.

1 mdi_power_required_modeB
2 A control variable indicating that over mode B, the PD is enabled and should request power from the PSE by
3 applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the
4 PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:
5 FALSE:PD functionality is disabled.
6 TRUE:PD functionality is enabled.
7

This is not part of the base line

When dual-signature DLL is enabled, it is enabled for both pairset. As a result pd_dll_enabled variable is the same for both modeA and modeB.

8
9
10 pd_dll_enabled_modeA
11 A variable indicating whether the Data Link Layer classification mechanism is enabled, ~~over mode A.~~
12 Values:
13 FALSE:Data Link Layer classification is not enabled.
14 TRUE:Data Link Layer classification is enabled.
15

16 ~~pd_dll_enabled_modeB~~
17 ~~—A variable indicating whether the Data Link Layer classification mechanism is enabled over mode B.~~
18 ~~Values:~~
19 ~~FALSE:Data Link Layer classification is not enabled.~~
20 ~~TRUE:Data Link Layer classification is enabled~~
21

22 pd_max_power_modeA
23 A control variable indicating the max power that the PD may draw from the PSE over mode A. See power
24 classifications in Table 33–28.
25 Values:
26 1: PD may draw Class 1 power
27 2: PD may draw Class 2 power
28 3: PD may draw Class 3 power
29 4: PD may draw Class 4 power
30 5: PD may draw Class 5 power
31

32 pd_max_power_modeB
33 A control variable indicating the max power that the PD may draw from the PSE over mode B. See power
34 classifications in Table 33–28.
35 Values:
36 1: PD may draw Class 1 power
37 2: PD may draw Class 2 power
38 3: PD may draw Class 3 power
39 4: PD may draw Class 4 power
40 5: PD may draw Class 5 power
41

42 pd_reset_modeA
43 An implementation-specific control variable that unconditionally resets the PD state diagram over mode A to the
44 OFFLINE_modeA state.
45 Values:
46 FALSE:The device has not been reset (default).
47 TRUE:The device has been reset.
48

49 pd_reset_modeB
50 An implementation-specific control variable that unconditionally resets the PD state diagram over mode B to the
51 OFFLINE_modeB state.
52 Values:

1 FALSE:The device has not been reset (default).
2 TRUE:The device has been reset.

3 `pd_undefined_modeA`
4 A control variable that indicates that the PD is in an undefined condition over mode A. The PD may or may not show
5 a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may
6 or may not show MPS and may change the `pse_power_level_modeA` variable.
7 Values:
8 FALSE:The PD is in a defined condition (default).
9 TRUE:The PD is an undefined condition.

10
11 `pd_undefined_modeB`
12 A control variable that indicates that the PD is in an undefined condition over mode B. The PD may or may not show
13 a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may
14 or may not show MPS and may change the `pse_power_level_modeB` variable.
15 Values:
16 FALSE:The PD is in a defined condition (default).
17 TRUE:The PD is an undefined condition.

18
19
20 `power_received_modeA`
21 An indication from the circuitry that power is present on the PD's PI over mode A.
22 Values:
23 FALSE:The input voltage does not meet the requirements of `VPort_PD` in Table 33–28.
24 TRUE:The input voltage meets the requirements of `VPort_PD`.

25
26 `power_received_modeB`
27 An indication from the circuitry that power is present on the PD's PI over mode B.
28 Values:
29 FALSE:The input voltage does not meet the requirements of `VPort_PD` in Table 33–28.
30 TRUE:The input voltage meets the requirements of `VPort_PD`.

31
32
33 `present_class_sig_A_modeA`
34 Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over
35 mode A.
36 Values:
37 FALSE:The PD classification signature is not to be applied to the link.
38 TRUE:The PD classification signature is to be applied to the link.

39
40
41 `present_class_sig_A_modeB`
42 Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over
43 mode B.
44 Values:
45 FALSE:The PD classification signature is not to be applied to the link.
46 TRUE:The PD classification signature is to be applied to the link.

47
48 `present_class_sig_B_modeA`
49 Controls presenting the classification signature that is used during the third class event and all subsequent class events
50 over mode A (see 33.3.5) by the PD.
51 Values:
52 FALSE:The PD classification signature is not to be applied to the link.
53 TRUE:The PD classification signature is to be applied to the link.
54
55
56

1
2
3 present_class_sig_B_modeB
4 Controls presenting the classification signature that is used during the third class event and all subsequent class events
5 over mode B (see 33.3.5) by the PD.
6 Values:
7 FALSE:The PD classification signature is not to be applied to the link.
8 TRUE:The PD classification signature is to be applied to the link.
9
10 present_det_sig_modeA
11 Controls presenting the detection signature (see 33.3.4) by the PD over mode A.
12 Values:
13 invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any
14 voltage above Vreset applied to mode B.
15 .
16 valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage
17 above Vreset applied to mode B.
18 either: Either a valid or non-valid PD detection signature may be applied to the link.
19
20 present_det_sig_modeB
21 Controls presenting the detection signature (see 33.3.4) by the PD over mode B.
22 Values:
23 invalid: A non-valid PD detection signature is to be applied to the link over mode B regardless of any
24 voltage above Vreset applied to mode B.
25 .
26 valid:A valid PD detection signature is to be applied to the link over mode B regardless of any voltage
27 above Vreset applied to mode B.
28 either: Either a valid or non-valid PD detection signature may be applied to the link.
29
30 present_mark_sig_modeA
31 Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode A.
32 Values:
33 FALSE:The PD does not present mark event behavior.
34 TRUE:The PD does present mark event behavior.
35
36 present_mark_sig_modeB
37 Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode B.
38 Values:
39 FALSE:The PD does not present mark event behavior.
40 TRUE:The PD does present mark event behavior.
41
42 present_mps_modeA
43 Controls applying MPS over mode A (see 33.3.7.10) to the PD's PI.
44 Values:
45 FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
46 TRUE:The MPS is to be applied to the PD's PI.
47
48 present_mps_modeB
49 Controls applying MPS over mode B (see 33.3.7.10) to the PD's PI.
50 Values:
51 FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
52 TRUE:The MPS is to be applied to the PD's PI.
53
54 pse_dll_power_level_modeA
55 A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the
56 PSE by which the PD is being powered over mode A.

1 Values:

- 2 1: The PSE has allocated Class 3 power or less (default).
- 3 2: The PSE has allocated Class 4 power.
- 4 3: The PSE has allocated Class 5

5
6 pse_dll_power_level_modeB

7 A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the
8 PSE by which the PD is being powered over mode B.

9 Values:

- 10 1: The PSE has allocated Class 3 power or less (default).
- 11 2: The PSE has allocated Class 4 power.
- 12 3: The PSE has allocated Class 5

13
14 **This is not part of the base line**

pse_dll_power_type was missing from the variable list and it is used in the state machine. In addition, For dual-signature PD it is not possible that different pse_dll_power_type values for the same PSE port will be indicated by the PD as for the PSE type it is connected to. As a result pse_dll_powerType_modeA and pse_dll_powerType_modeB should be merged to pse_dll_powerType only.

15
16 pse_dll_power_type

17 A control variable output by the PD power control state diagram (Figure 33-50) that
18 indicates the PSE type connected as 1 or 2, see 79.3.2.4.1.

19 The PSE type will be set according to the pairset with the highest power capability.

20 Values:

- 21 1: The PSE is a Type 1 PSE, for a Type-1 PSE.
- 22 2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE.

23
24
25 pse_power_level_modeA

26 A control variable that indicates to the PD over mode A the level of power the PSE is supplying.

27 Values:

- 28 3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.
- 29 4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.
- 30 5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

31
32 pse_power_level_modeB

33 A control variable that indicates to the PD over mode B the level of power the PSE is supplying.

34 Values:

- 35 3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.
- 36 4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.
- 37 5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

38
39
40
41 **Editor Note:**

42 **The variables:**

43 ~~a) pse_power_type_modeA~~

44 ~~b) pse_power_type_modeB~~

45 ~~should be generated by PD Type 3 and Type 4 dual signature state machine (as pse_power_type is~~
46 ~~also needed to be generated by Type 3 and Type 4 single signature PD state machine) in order to~~

1 ~~be used later by Figure 33-50 which is the DLL state machine and as a result need to be added also~~
2 ~~to 33.6.3.3 variable list.~~
3 ~~They are not required for Type 3 and 4 single or dual signature PD state machine.~~

4
5 VPD_modeA
6 Voltage at the PD PI as defined in 1.4.425 over mode A.

7
8 VPD_modeB
9 Voltage at the PD PI as defined in 1.4.425 over mode B.
10

11 **33.3.3.13 Type 3 and Type 4 dual-signature timers**

12 All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting
13 upon entering a state where “stop x_timer” is asserted.

14 tpowerdly_timer_modeA
15 A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode A and
16 class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode A during the PSE’s inrush
17 period; see Tdelay-2P in Table 33–28.

18
19 tpowerdly_timer_modeB
20 A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode B and
21 class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode B during the PSE’s inrush
22 period; see Tdelay-2P in Table 33–28.
23

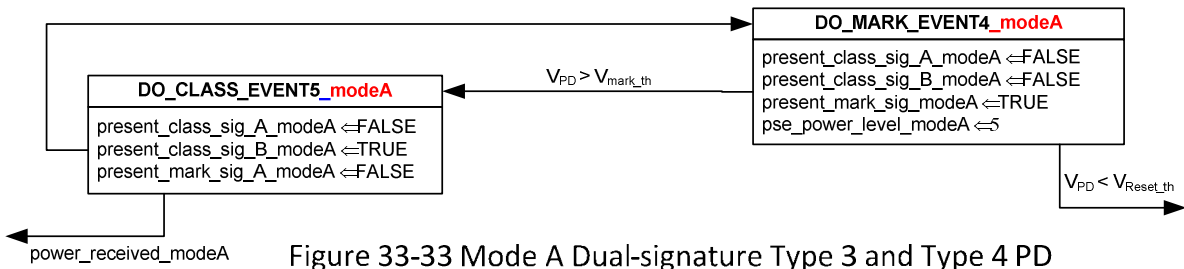
24 **33.3.3.14 Type 3 and Type 4 dual-signature functions**

25 do_class_timing_modeA
26 This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the
27 length of the class event over mode A. The class event timing requirements are defined in Table 33–26. This function
28 returns the following variable:
29 short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable
30 is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:
31 TRUE: The PSE uses Type 3, 4 MPS requirements.
32 FALSE: The PSE uses Type 1, 2 MPS requirements.

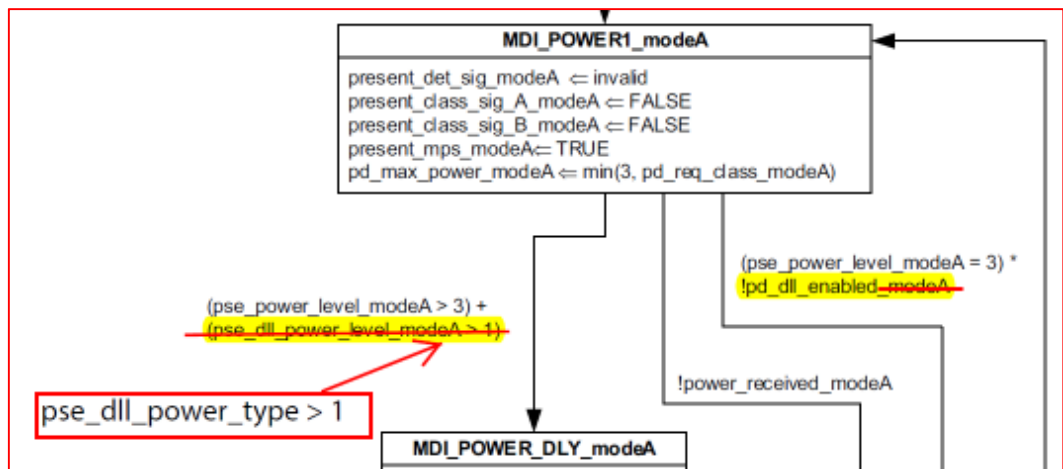
33
34
35
36 do_class_timing_modeB
37 This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the
38 length of the class event over mode B. The class event timing requirements are defined in Table 33–26. This function
39 returns the following variable:
40 short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable
41 is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:
42 TRUE: The PSE uses Type 3, 4 MPS requirements.
43 FALSE: The PSE uses Type 1, 2 MPS requirements.
44
45
46
47
48
49

33.3.3.15 Type 3 and Type 4 dual-signature state diagrams

Make the following changes on page 135 on Figure 33-33—Type 3 and Type 4 dual-signature PD state diagram for Mode A.

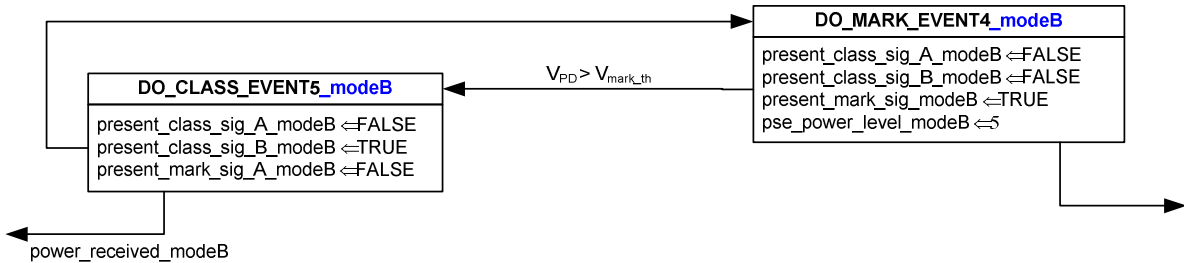


Make the following changes on Page 136 on Figure 33-33—Type 3 and Type 4 dual-signature PD state diagram for Mode A (continued).

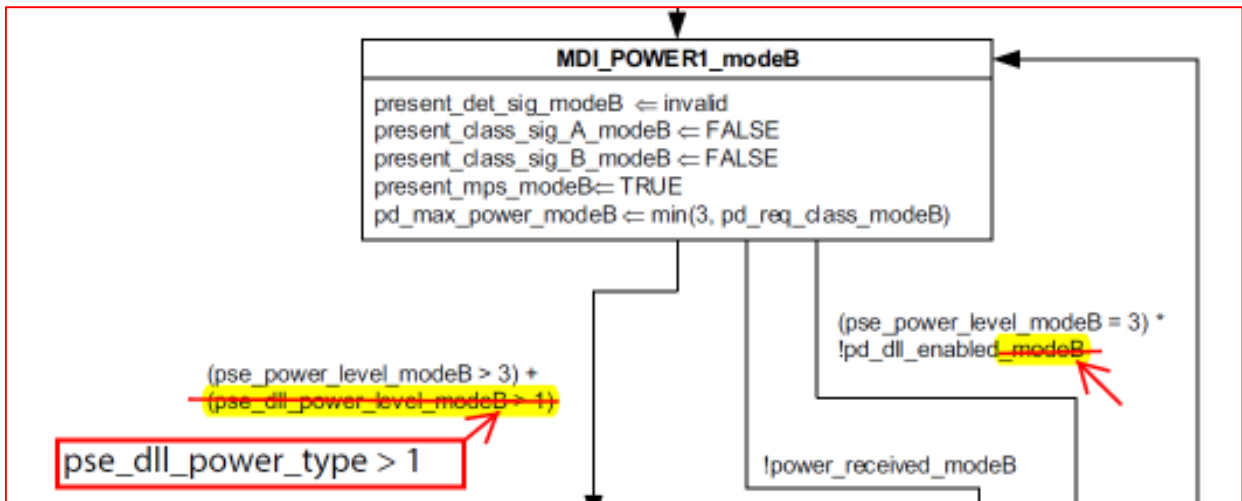


Change the exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138 should to match with the exits in Figure 33-32 page 129 with the prefix **_modeA** per the approved remedy for comments on this subject.

Make the following changes on page 137 in Figure 33–34—Type 3 and Type 4 dual-signature PD state diagram for Mode A.



Make the following changes in:
 Figure 33–34—Type 3 and Type 4 dual-signature PD state diagram for Mode B (continued), Page 138



Change the exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138 should to match with the exits in Figure 33-32 page 129 with the prefix **_modeB** per the approved remedy for comments on this subject.

1 Suggested Remedy –Option B

2 Make the following changes:

3 The following are the requirements for dual-signature PD state machine over each modeA and
4 modeB. The dual-signature state machine shall be implemented over each pairset for mode A
5 and mode B independently unless otherwise specified. All the parameters that applies to mode A
6 and mode B are denoted with the suffix “_modeY” where “Y” can be “A” or “B”. A parameter that
7 ends with the suffix “_modeY” may have different values for mode A and mode B.

8 33.3.3.11 Type 3 and Type 4 dual-signature constants

9

This is not part of the base line
--

Work need to be done to verify that single signature and dual-signature state machine and their variable list are sync with DLL state machines Figure 33-49 and Figure 33-50.

10

11 *Editor Note: DLL PSE and PD power control state diagram (Figure 33-49 and Figure 33-50) need to*
12 *be evaluate and sync with the single signature and dual-signature PD state machine.*

13

14 The PD state diagram uses the following constants:

15 VReset

16 Reset voltage per pairset (see Table 33–26)

17 VReset_th

18 Reset voltage threshold per pairset (see Table 33–26)

19 VMark_th

20 Mark event voltage threshold per pairset (see Table 33–26)

21

22 pd_req_class_modeA_modeY

23 A constant indicating the requested Class of the PD over mode Ymode A.

24

24 Values:

25 1: The PD requests Class 1.

26 2: The PD requests Class 2.

27 3: The PD requests Class 3.

28 4: The PD requests Class 4.

29 5: The PD requests Class 5.

30

31 ~~pd_req_class_modeB~~

32 ~~A constant indicating the requested Class of the PD over mode B.~~

33

33 ~~Values:~~

34 ~~1: The PD requests Class 1.~~

35 ~~2: The PD requests Class 2.~~

36 ~~3: The PD requests Class 3.~~

37 ~~4: The PD requests Class 4.~~

38 ~~5: The PD requests Class 5.~~

39

40

33.3.3.12 Type 3 and Type 4 dual-signature variables

The PD state diagram uses the following variables:

`mdi_power_required_modeYmodeA`

A control variable indicating that over `mode Ymode A`, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.

Values:

FALSE:PD functionality is disabled.

TRUE:PD functionality is enabled.

~~`mdi_power_required_modeB`~~

~~A control variable indicating that over mode B, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:~~

~~FALSE:PD functionality is disabled.~~

~~TRUE:PD functionality is enabled.~~

This is not part of the base line
When dual-signature DLL is enabled, it is enabled for both pairset. As a result <code>pd_dll_enabled</code> variable is the same for both modeA and modeB.

~~`pd_dll_enabled_modeA`~~

~~A variable indicating whether the Data Link Layer classification mechanism is enabled over mode A.~~

~~Values:~~

~~FALSE:Data Link Layer classification is not enabled.~~

~~TRUE:Data Link Layer classification is enabled.~~

~~`pd_dll_enabled_modeB`~~

~~A variable indicating whether the Data Link Layer classification mechanism is enabled over mode A.~~

~~Values:~~

~~FALSE:Data Link Layer classification is not enabled.~~

~~TRUE:Data Link Layer classification is enabled.~~

`pd_max_power_modeYmodeA`

A control variable indicating the max power that the PD may draw from the PSE over `mode Ymode A`. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power

2: PD may draw Class 2 power

3: PD may draw Class 3 power

4: PD may draw Class 4 power

5: PD may draw Class 5 power

~~`pd_max_power_modeB`~~

~~A control variable indicating the max power that the PD may draw from the PSE over modeB. See power classifications in Table 33–28.~~

~~Values:~~

~~1: PD may draw Class 1 power~~

~~2: PD may draw Class 2 power~~

~~3: PD may draw Class 3 power~~

~~4: PD may draw Class 4 power~~

1 5: PD may draw Class 5 power

2
3 pd_reset_ ~~modeY~~modeA

4 An implementation-specific control variable that unconditionally resets the PD state diagram over mode ~~A~~Y to the

5 OFFLINE_ ~~modeY~~modeA state.

6 Values:
7 FALSE: The device has not been reset (default).
8 TRUE: The device has been reset.

9
10 ~~pd_reset_modeB~~

11 ~~An implementation-specific control variable that unconditionally resets the PD state diagram over mode B to the~~

12 ~~OFFLINE_modeB state.~~

13 ~~Values:
14 FALSE: The device has not been reset (default).
15 TRUE: The device has been reset.~~

16
17 pd_undefined_ ~~modeY~~modeA

18 A control variable that indicates that the PD is in an undefined condition over ~~mode Y~~mode A. The PD may or may

19 not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class

20 current, may or may not show MPS and may change the pse_power_level_modeA variable.
21 Values:
22 FALSE: The PD is in a defined condition (default).
23 TRUE: The PD is an undefined condition.

24
25 ~~pd_undefined_modeB~~

26 ~~A control variable that indicates that the PD is in an undefined condition over mode B. The PD may or may not show~~

27 ~~a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may~~

28 ~~or may not show MPS and may change the pse_power_level_modeB variable.~~
29 ~~Values:
30 FALSE: The PD is in a defined condition (default).
31 TRUE: The PD is an undefined condition.~~

32
33
34 power_received_ ~~modeY~~modeA

35 An indication from the circuitry that power is present on the PD's PI over ~~mode Y~~mode A.

36 Values:
37 FALSE: The input voltage does not meet the requirements of VPort_PD in Table 33–28.
38 TRUE: The input voltage meets the requirements of VPort_PD.

39
40 ~~power_received_modeB~~

41 ~~An indication from the circuitry that power is present on the PD's PI over mode B.~~

42 ~~Values:
43 FALSE: The input voltage does not meet the requirements of VPort_PD in Table 33–28.
44 TRUE: The input voltage meets the requirements of VPort_PD.~~

1 present_class_sig_A_modeYmodeA
2 Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over
3 mode YmodeA.
4 Values:
5 FALSE:The PD classification signature is not to be applied to the link.
6 TRUE:The PD classification signature is to be applied to the link.
7
8
9 ~~present_class_sig_A_modeB~~
10 ~~Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over~~
11 ~~mode B.~~
12 ~~Values:~~
13 ~~FALSE:The PD classification signature is not to be applied to the link.~~
14 ~~TRUE:The PD classification signature is to be applied to the link.~~
15
16 present_class_sig_B_modeYmodeA
17 Controls presenting the classification signature that is used during the third class event and all subsequent class events
18 over mode AY (see 33.3.5) by the PD.
19 Values:
20 FALSE:The PD classification signature is not to be applied to the link.
21 TRUE:The PD classification signature is to be applied to the link.
22
23 ~~present_class_sig_B_modeB~~
24 ~~Controls presenting the classification signature that is used during the third class event and all subsequent class events~~
25 ~~over mode B (see 33.3.5) by the PD.~~
26 ~~Values:~~
27 ~~FALSE:The PD classification signature is not to be applied to the link.~~
28 ~~TRUE:The PD classification signature is to be applied to the link.~~
29
30 present_det_sig_modeYmodeA
31 Controls presenting the detection signature (see 33.3.4) by the PD over mode AY.
32 Values:
33 invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any
34 voltage above Vreset applied to mode B.
35
36 valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage
37 above Vreset applied to mode B.
38 either: Either a valid or non-valid PD detection signature may be applied to the link.
39
40 ~~present_det_sig_modeB~~
41 ~~Controls presenting the detection signature (see 33.3.4) by the PD over mode B.~~
42 ~~Values:~~
43 ~~invalid: A non-valid PD detection signature is to be applied to the link over mode B regardless of any~~
44 ~~voltage above Vreset applied to mode B.~~
45 ~~=~~
46 ~~valid:A valid PD detection signature is to be applied to the link over mode B regardless of any voltage~~
47 ~~above Vreset applied to mode B.~~
48 ~~either: Either a valid or non-valid PD detection signature may be applied to the link.~~
49
50 present_mark_sig_modeA-modeY
51 Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode AY.
52 Values:
53 FALSE:The PD does not present mark event behavior.
54 TRUE:The PD does present mark event behavior.
55
56

1 present_mark_sig_modeB

2 Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode B.

3 Values:

4 ~~FALSE: The PD does not present mark event behavior.~~

5 ~~TRUE: The PD does present mark event behavior.~~

6
7 present_mps_modeAmodeY

8 Controls applying MPS over mode ~~A~~Y (see 33.3.7.10) to the PD's PI.

9 Values:

10 FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.

11 TRUE: The MPS is to be applied to the PD's PI.

12
13 present_mps_modeB

14 Controls applying MPS over mode B (see 33.3.7.10) to the PD's PI.

15 Values:

16 ~~FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.~~

17 ~~TRUE: The MPS is to be applied to the PD's PI.~~

18
19
20 pse_dll_power_level_modeA-modeY

21 A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode ~~A~~Y.

22 Values:

23 1: The PSE has allocated Class 3 power or less (default).

24 2: The PSE has allocated Class 4 power.

25 3: The PSE has allocated Class 5

26
27
28 pse_dll_power_level_modeB

29 A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode B.

30 Values:

31 ~~1: The PSE has allocated Class 3 power or less (default).~~

32 ~~2: The PSE has allocated Class 4 power.~~

33 ~~3: The PSE has allocated Class 5~~

34
35 **This is not part of the base line**

For dual-signature PD it is not possible that different pse_dll_power_type values for the same PSE port will be indicated by the PD as for the PSE type it is connected to. As a result pse_dll_powerType_modeA and pse_dll_powerType_modeB should be merged to pse_dll_powerType only.

36
37 pse_dll_power_type

38 A control variable output by the PD power control state diagram (Figure 33-50) that indicates the PSE type connected to mode Y as 1 or 2, see 79.3.2.4.1.

39 Values:

40 1: The PSE is a Type 1 PSE, for a Type-1 PSE.

41 2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE.

1 pse_power_level_modeAmodeY

2 A control variable that indicates to the PD over mode ~~A~~Y the level of power the PSE is supplying.

3 Values:

4 3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.

5 4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.

6 5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

7
8 ~~pse_power_level_modeB~~

9 ~~A control variable that indicates to the PD over mode B the level of power the PSE is supplying.~~

10 ~~Values:~~

11 ~~3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.~~

12 ~~4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.~~

13 ~~5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.~~

14
15 Editor Note:

16 The variables:

17 a) pse_power_type_modeA

18 b) pse_power_type_modeB

19 should be generated by PD Type 3 and Type 4 dual-signature state machine (as pse_power_type is
20 also needed to be generated by Type 3 and Type 4 single-signature PD state machine) in order to
21 be used later by Figure 33-50 which is the DLL state machine and as a result need to be added also
22 to 33.6.3.3 variable list.

23 They are not required for Type 3 and 4 single or dual-signature PD state machine.

24
25
26 VPD_modeAmodeY

27 Voltage at the PD PI as defined in 1.4.425 over mode ~~A~~Y.

28
29 ~~VPD_modeB~~

30 ~~Voltage at the PD PI as defined in 1.4.425 over mode B.~~

31 32 **33.3.3.13 Type 3 and Type 4 dual-signature timers**

33 All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting
34 upon entering a state where "stop x_timer" is asserted.

35 tpowerdly_timer_modeAmodeY

36 A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode ~~A~~Y and
37 class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode ~~A~~Y during the PSE's inrush
38 period; see Tdelay-2P in Table 33-28.

39
40 ~~tpowerdly_timer_modeB~~

41 ~~A timer used to prevent class 4 Type 3 dual signature PDs from drawing more than Type 1 power over mode B and~~
42 ~~class 5 Type 4 dual signature PDs from drawing more than Class 2 power over mode B during the PSE's inrush~~
43 ~~period; see Tdelay-2P in Table 33-28.~~

33.3.3.x4 Type 3 and Type 4 dual-signature functions

do_class_timing_modeAmodeY

This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode ~~A~~Y. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.

FALSE: The PSE uses Type 1, 2 MPS requirements.

~~do_class_timing_modeB~~

~~This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode B. The class event timing requirements are defined in Table 33–26. This function returns the following variable:~~

~~short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:~~

~~TRUE: The PSE uses Type 3, 4 MPS requirements.~~

~~FALSE: The PSE uses Type 1, 2 MPS requirements.~~

Make the following changes in Figure 33-33:

1. Change the title of figure 33-33 on page 135 as follows:

“Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for ~~mode X~~mode Y”

2. Change the title of figure 33-33 on page 136 as follows:

“Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for ~~mode X~~mode Y (continued)”

3. Make the following changes in Figure 33-33 on page 135.

DO_CLASS_EVENT5 and DO_MARK_EVENT4 is missing the suffix “_modeY”.

4. Make the following changes in Figure 33-33 on both pages 135 and 136:

Replace all parameters with the suffix “modeA” with “~~mode X~~mode Y”

5. Make the following changes in Figure 33-33 on page 136:

-Replace “pse_dll_power_level_modeA” with “pse_dll_power_type ~~mode X~~mode Y”.

-Replace “!pd_dll_enabled_modeA” with “!pd_dll_enabled” .

-Replace “pse_dll_power_level_modeA” with “pse_dll_power_type”.

-Replace “pse_power_level_modeA > 3” with “pse_power_type > 3”

-Replace “pse_power_level_modeA = 3” with “pse_power_type = 3”

6. Make the following changes in Figure 33-34 on page 137 and 138:

Delete Figure 33-34 on pages 137 and 138.

7. The revised Figure 33-33 is attached below (two pages)

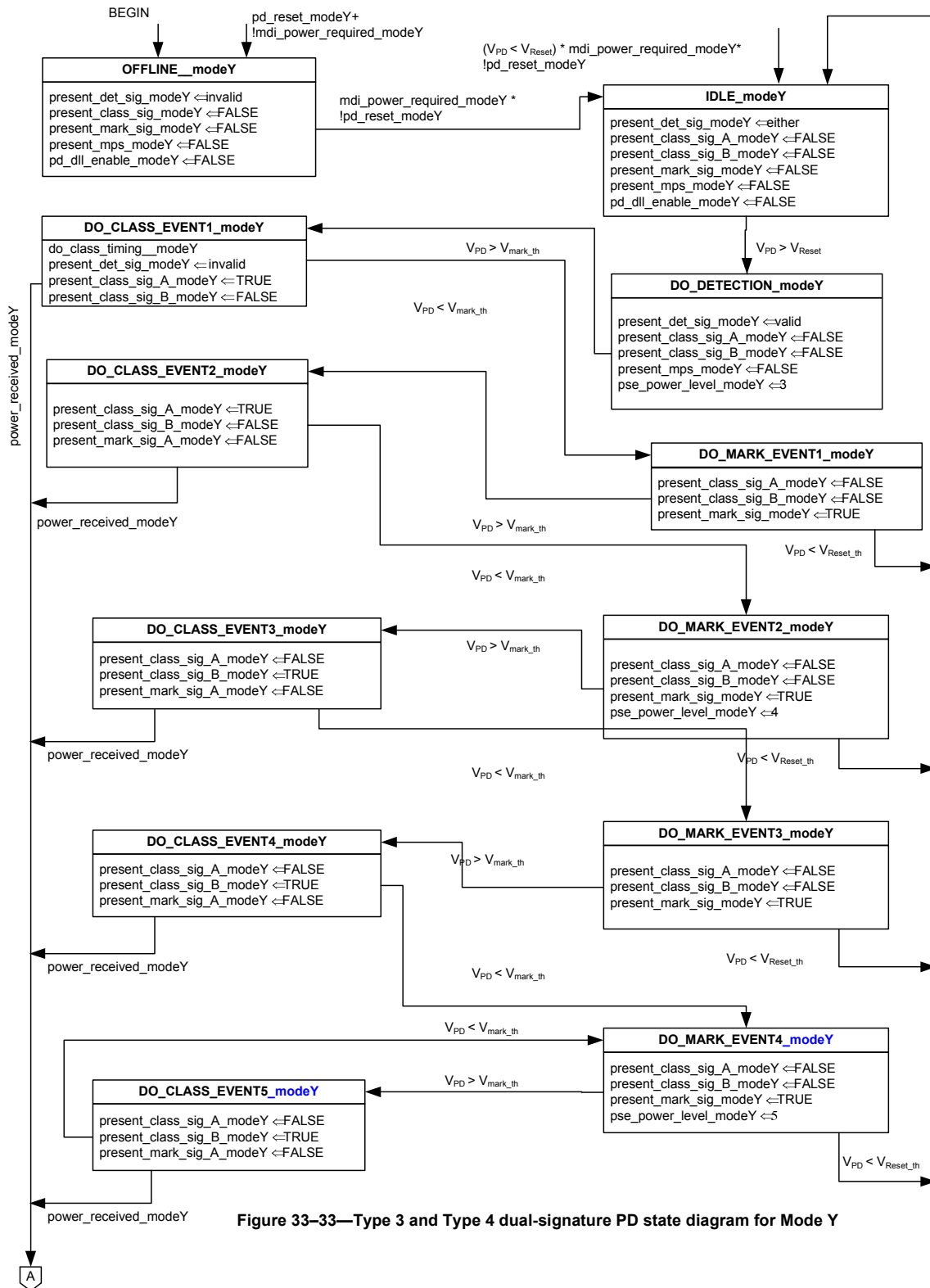


Figure 33-33—Type 3 and Type 4 dual-signature PD state diagram for Mode Y

1 8.

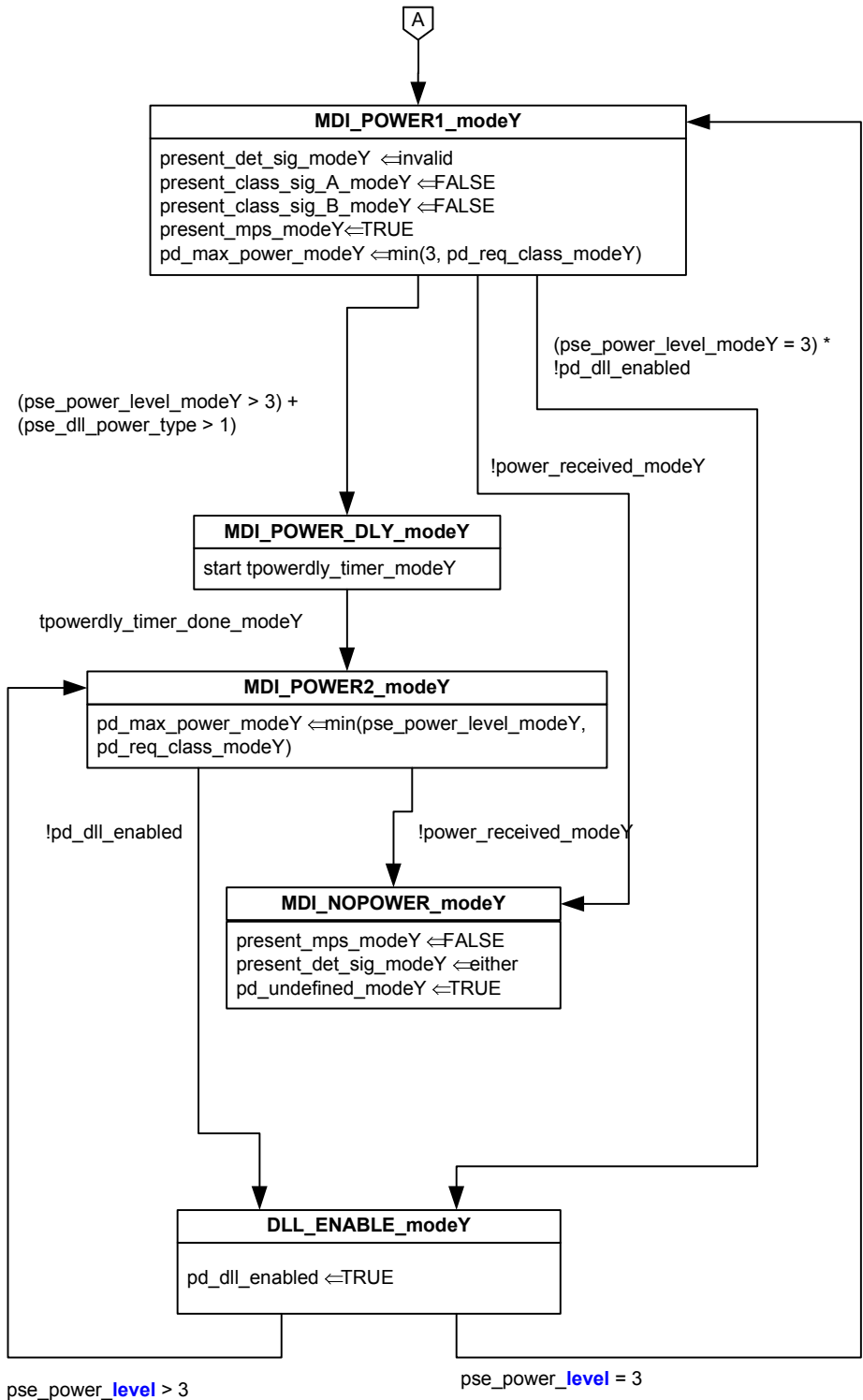


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for Mode Y (continued)

2

1
2
3
4
5
6
7
8
9
10
11

Base Line ends here

Revision History

#	Revision	Draft	Changes made
1	002	1.8	-----
2	003	2.0	1. Deleting unused variables. 2. Deleting suffix "modeA" from pd_dll_enabled and delete pd_dll_enabled_modeB 3. pse_dll_power_type was added. 4. Figures 33-33 and 33-34 where updated accordingly.
3	004		Optional solution to further simplifying dual-signature state machine was added (Option B). Suffix "X" was changed to "Y" since "X" is used in other places.

12