

# PSE State Diagram – Sequence 3

Considerations for Staggered Detection and Power-on of Dual-Signature PDs.

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# Goal(s):

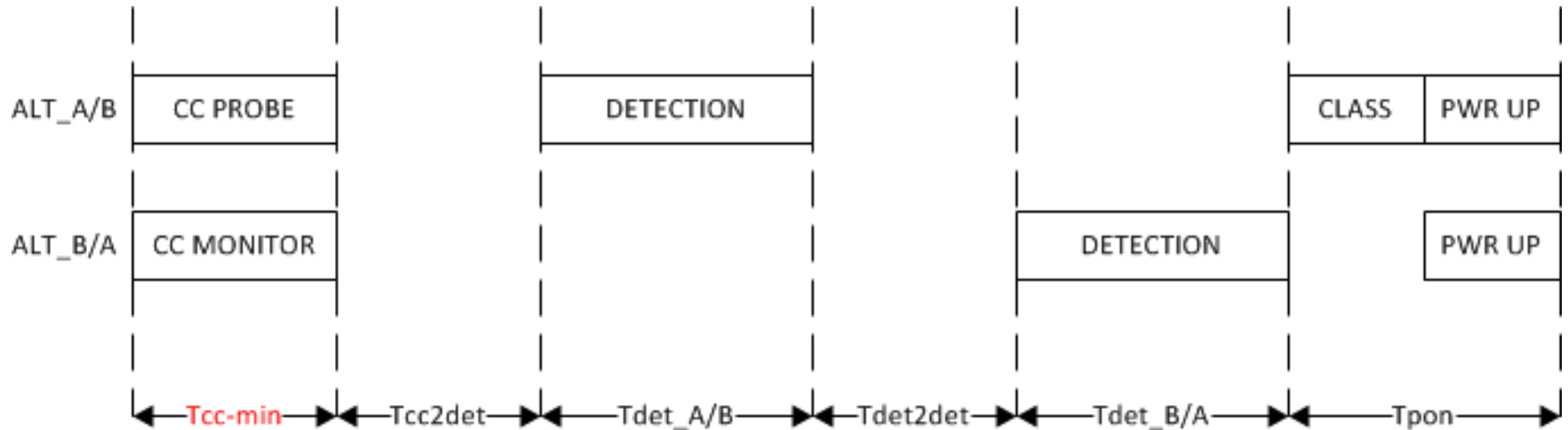
1. Add a sequence to the Type3 / Type 4 State Diagram that allows for a more cost-effective implementation in some architectures.
2. Add text to define the interchangeable nature of the treatment of alternative-A and Alternative-B in the State Diagram.

# Sequence 3:

Staggered Detection and Power-up of DS PDs.

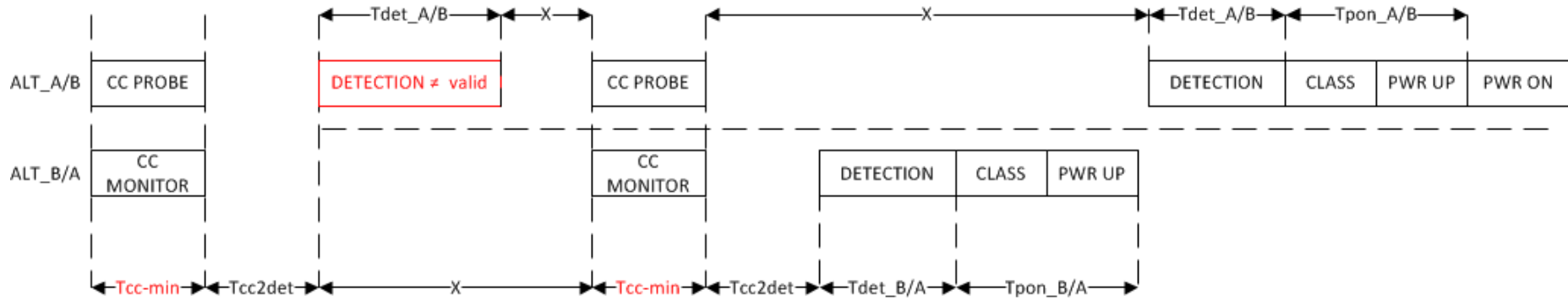
CC → Det/CIs/Pwr ALT\_A/B → Det/CIs/Pwr ALT\_B/A

# CC → Det (SS PD)



For SS PDs, Sequence 3 is identical to Sequence 0

# CC → Det/Cls/Pwr Alt\_A/B (DS PD)



$T_{cc2det}$  is enforced for the first pairset to successfully power.

$T_{det}$  and  $T_{pon}$  are enforced for each pairset.

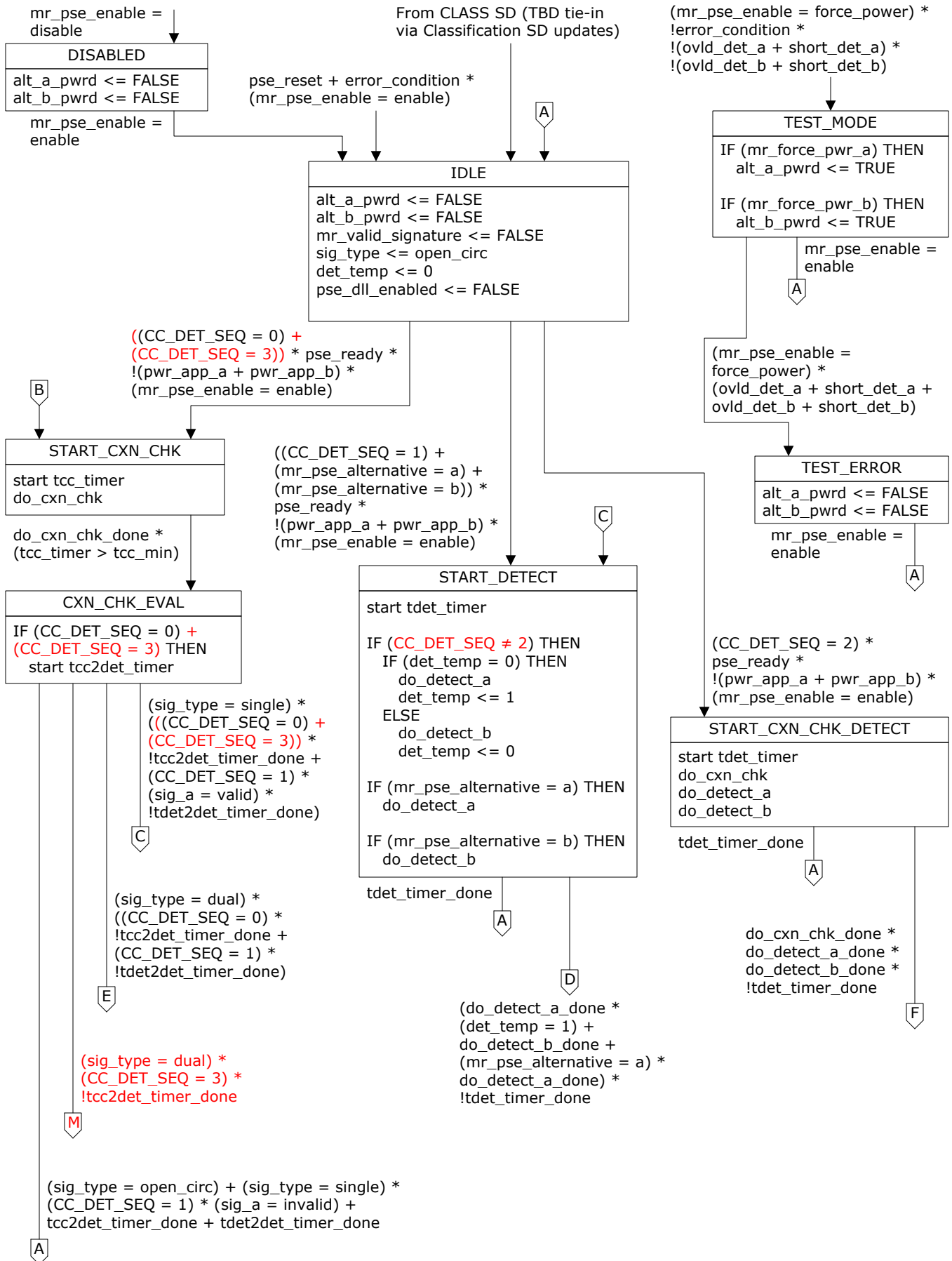
# Alternative A/B Parity:

Treatment of Alt-A and Alt-B are interchangeable for the purposes of the State Diagram

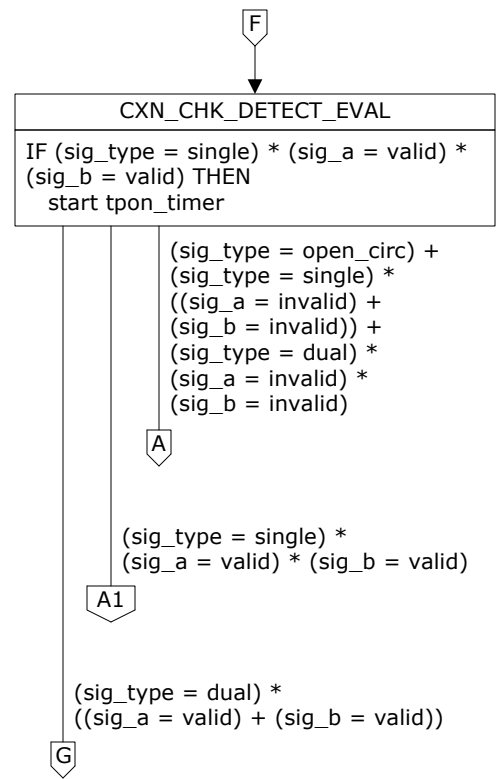
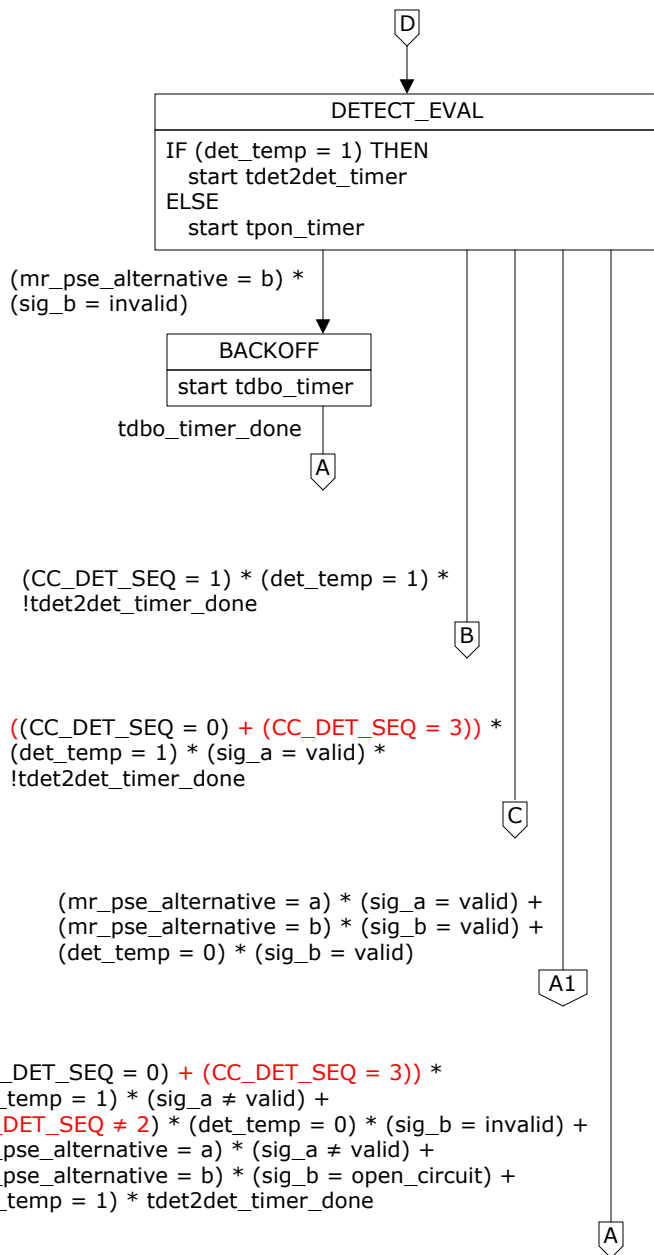
# Alternative A/B Parity text:

Add the following text in section 33.2.4.1:

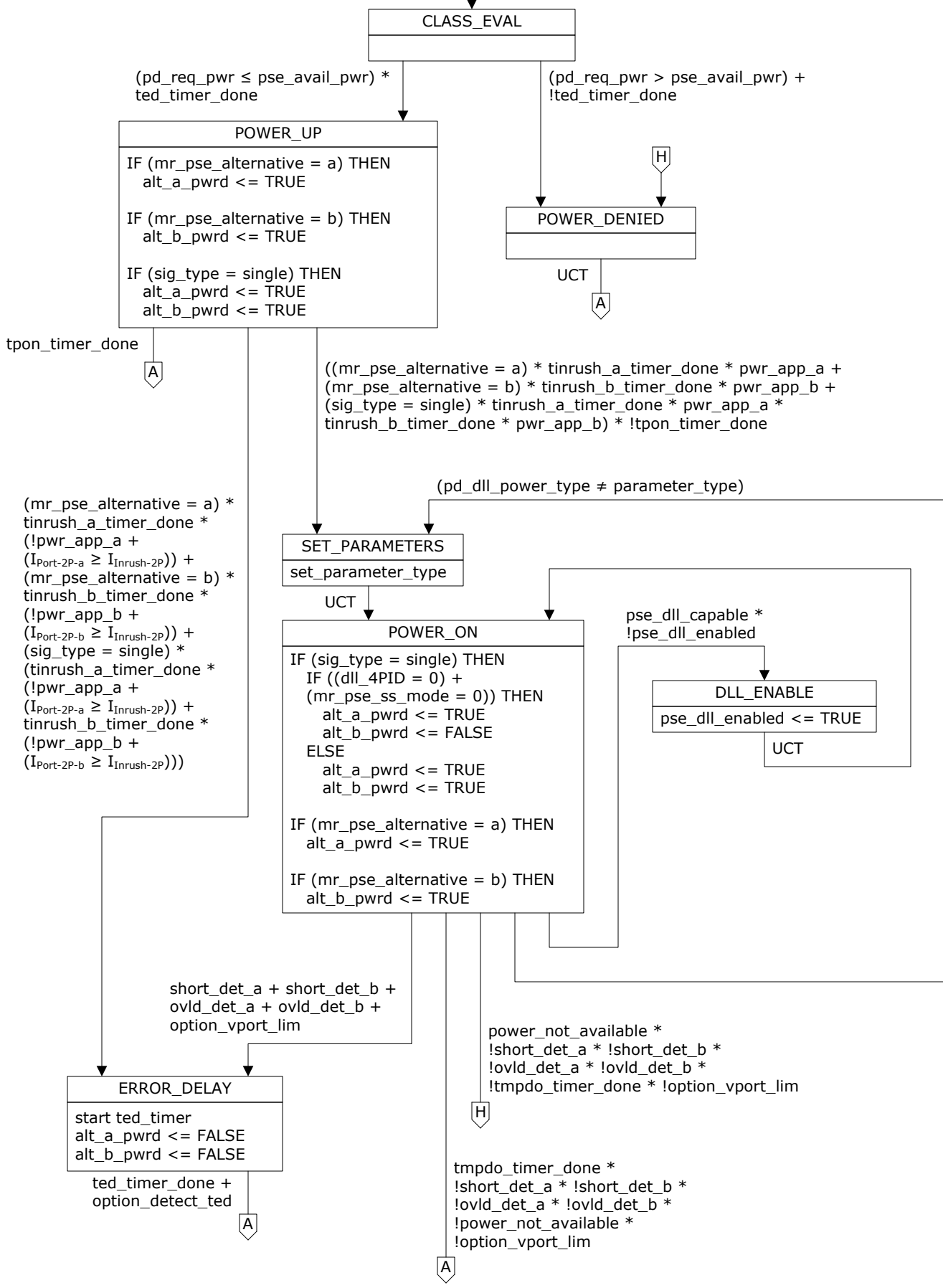
“In the Type 3 and Type 4 state diagram, Alternative A and Alternative B are depicted as serving distinct roles during 4-pair operation. In any implementation, the behaviors of the Alternatives may be reversed as long as the roles are established in IDLE and shall be maintained in every other state.”

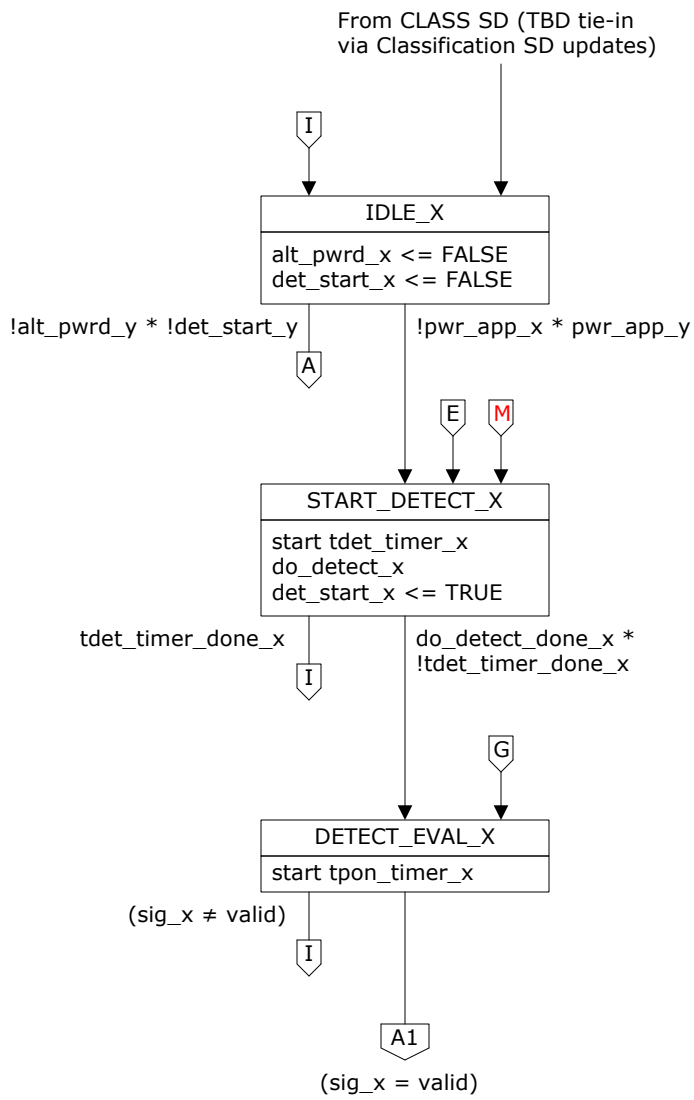




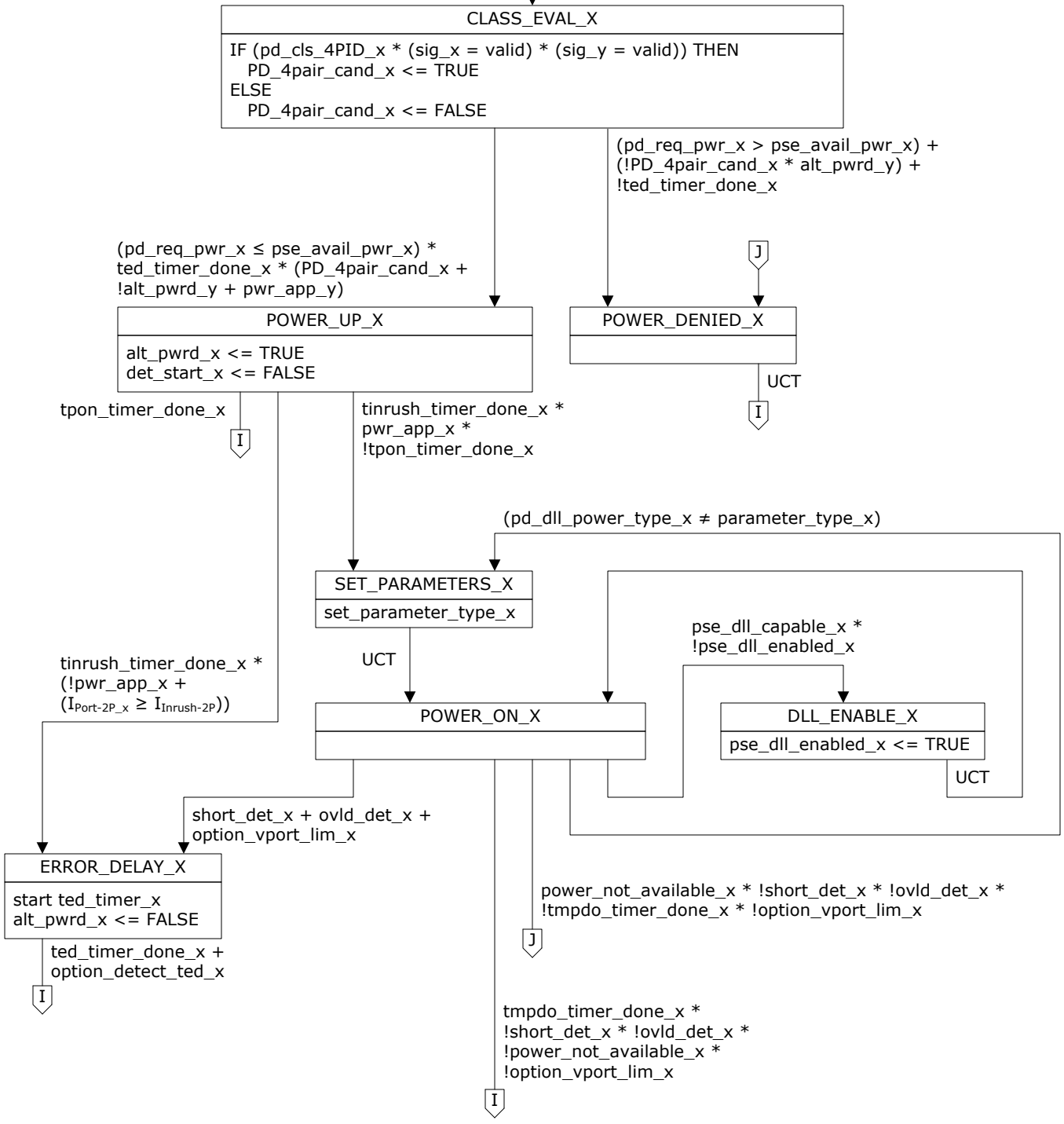


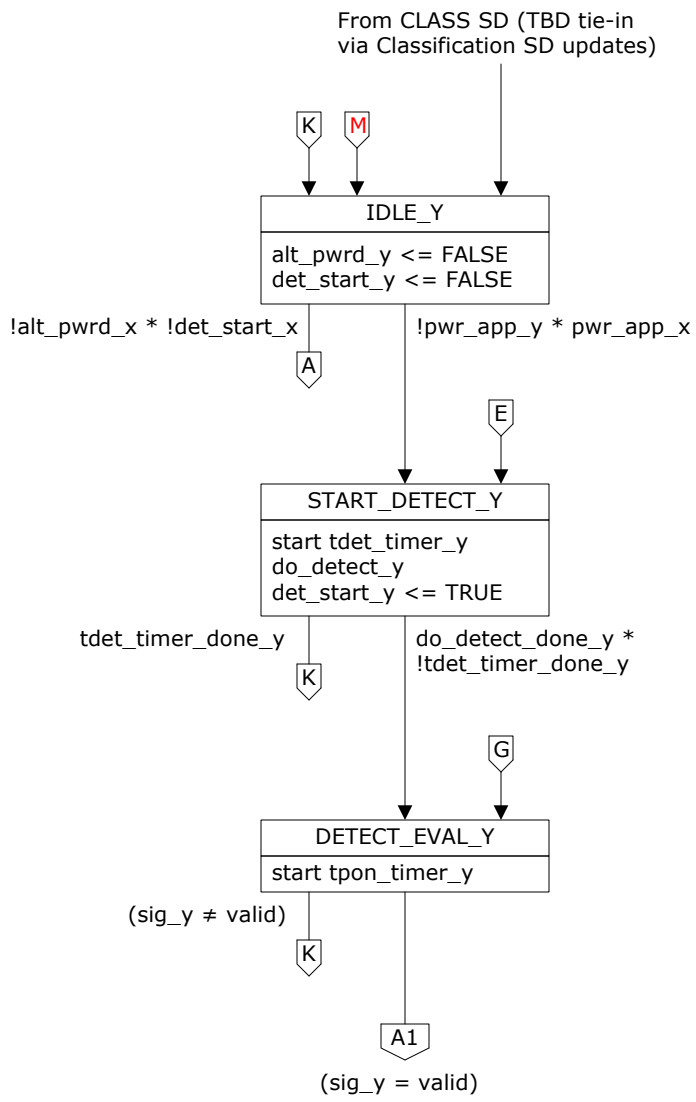
From CLASS SD (TBD tie-in via Classification SD updates)





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