

# 4P-MPS For PDs with low standby v152

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## Design goals of MPS

The purpose of MPS is to remove power when the PD is physically disconnected.

- ▶ Require as little power as technically feasible
- ▶ Straightforward implementation (PSE + PD)
- ▶ Fool proof operation, cable disconnects (including X/Y cable situations) must lead to correct power removal

4P operation requires new MPS rules that meet these design goals.

For PDs with a low power state it is essential that MPS power is low and implementing it is straightforward and reliable.

# PD MPS balance requirements

Requiring the PD to balance the MPS currents is problematic for several reasons:

- ▶ PSE induced  $V_{diff}$  can cause MPS unbalance which PD cannot influence
- ▶ Maximum diode  $V_{diff}$  is not specified in datasheet, making it hard to guarantee a correct design
- ▶ Temperature effects (uneven heating) can cause increase in unbalance<sup>1</sup>
- ▶ Uneven aging effect of diodes can cause unbalance to increase over time<sup>1</sup>

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<sup>1</sup>Lighting fixtures have a lifetime  $\geq 25$  year.

# MPS proposal

$I_{\text{Hold}}$ (Total)	Total current the PSE must measure to consider MPS met.
$I_{\text{Hold}}$ (1PS)	Current the PSE must measure on at least 1 powered pair-set to consider MPS met.
$I_{\text{Hold}}$ (Each)	Current the PSE must measure on every powered pair-set to consider MPS met.
$I_{\text{Port\_MPS}}$ (Total)	Minimum total current the PD must draw
$I_{\text{Port\_MPS}}$ (Each)	Minimum current the PD must draw on every powered pair-set
Sig	Single-Signature (=SS) or Dual-Signature (=DS) PD
Timing	PSE or PD should follow the 'old' or 'new' timing

PSE	PD	Sig	Class	PSE Requirements				PD Requirements		
				Total	$I_{\text{Hold}}$		Timing	Total	Each	Timing
					1PS	Each				
Type 1,2	Type 1,2	-	0-4	5-10 mA	-	-	Old	10 mA	-	Old
	Type 3,4	SS	0-4	5-10 mA	-	-	Old	10 mA	-	Old
	Type 3,4	DS	0-4	5-10 mA	-	-	Old	-	10 mA	Old
Type 3,4	Type 1,2	-	0-4	4-9 mA	2-5 mA	-	New	10 mA	-	Old
	Type 3,4	SS	0-4	4-9 mA	2-5 mA	-	New	10 mA	-	New
	Type 3,4	SS	5-8	4-14 mA	2-7 mA	-	New	16 mA	-	New
	Type 3,4	DS	0-8	-	-	2-7 mA	New	-	8 mA	New

## Supported MPS methods

- $I_{\text{Hold}}$  (Total)    **Total current** the PSE must measure to consider MPS met.
- $I_{\text{Hold}}$  (1PS)    Current the PSE must measure on **at least 1 powered pair-set** to consider MPS met.
- $I_{\text{Hold}}$  (Each)    Current the PSE must measure on **every powered pair-set** to consider MPS met.

For Type 1, 2 and single signature (SS) Type 3 and Type 4 PDs, the PSE may choose how to check MPS:

- ▶ Total: Compare total current (sum of both  $I_{\text{Port-2P}}$ ) to  $I_{\text{Hold}}$
- ▶ 1PS: Compare  $I_{\text{Port-2P}}$  of pair-set with highest current to  $I_{\text{Hold}}$

PDs meeting  $I_{\text{Port\_MPS}}$  guarantee meeting both  $I_{\text{Hold}}$  (Total) and  $I_{\text{Hold}}$  (1PS) at the PSE.

Each: Dual signature PDs must guarantee MPS on each pair-set.

# L1, LLDP, Autoclass

MPS specifications for single signature PDs are different depending on the value of  $P_{\text{Class\_PD}}$  (greater or smaller than Class 4 power)

**L1** The initial power allocation done through physical layer classification determines the MPS specifications for the PD.

**LLDP** If a PD re-negotiates through LLDP it can cross the Class 4 / Class 5 boundary. Such a PD must comply with the specifications associated with the PD class negotiated through LLDP.

**Auto** An Autoclass PD must follow the MPS specifications associated with the initial advertised maximum power class.

# Conclusion

This presentation proposes MPS specifications for Type 3 and Type 4

- ▶ Allows PSE flexibility to either look at the sum of MPS currents, or look at the pair-set MPS currents for single signature PDs.
- ▶ Dual signature PD rules prevent powering disconnected pairs
- ▶ MPS is as easy to implement correctly for Type 3/4 as for Type 1/2 PDs



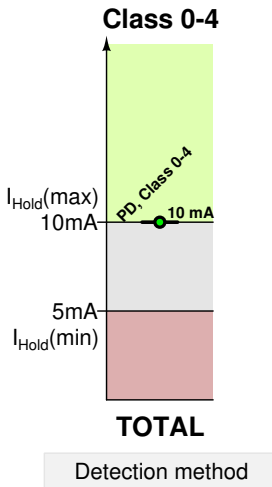


# Overview table explained

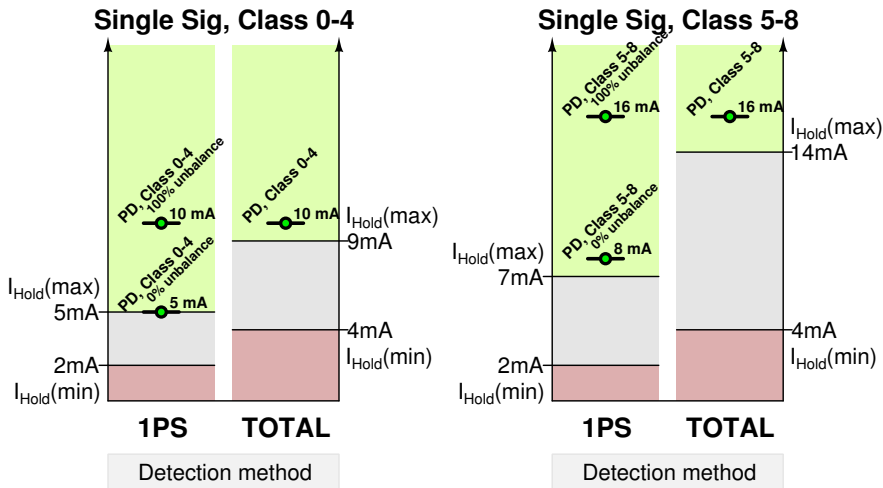
Alternate methods PSE can choose from				PSE Requirements				PD Requirements		
PSE	PD	Sig	Class	$I_{Hold}$			Timing	$I_{Port\_MPS}$		
				Total	1PS	Each		Total	Each	Timing
Type 3,4	Type 1,2	-	0-4	4-9 mA	2-5 mA	-	New	10 mA	-	Old
	Type 3,4	SS	0-4	4-9 mA	2-5 mA	-	New	10 mA	-	New
	Type 3,4	SS	5-8	4-14 mA	2-7 mA	-	New	16 mA	-	New
	Type 3,4	DS	0-8	-	-	2-7 mA	New	-	8 mA	New

- PSE cannot distinguish between these PD types. Specifications must be identical. Type 1/2 PDs will draw 10mA MPS with old timings.
  - A Type 3 PSE can apply the new MPS timing because it is backward compatible with the old MPS PD timing.
- In case of perfect balance, a PD with 10mA total current will generate 5mA on each pairset, so PSE needs to support 5mA  $I_{hold(max)}$  for this case. It is not possible to use the Type 1/2  $I_{hold}$  range of 5-10mA in 4P mode.

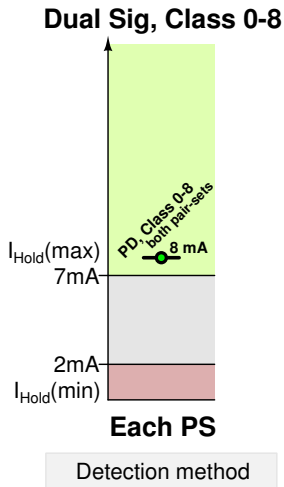
# Type 1/2 PSE MPS Graphical



# Type 3/4 PSE + SS PD MPS Graphical



# Type 3/4 PSE + DS PD MPS Graphical



## PSE Type 3/4 MPS Rules connected to...

- ▶ **PD Type 1, 2 & 3, 4 (single signature,  $P_{\text{Class\_PD}} \leq \text{Class 4}$ )**
  - ▶  $I_{\text{Hold}}$  (Total) = 4-9 mA total current, or
  - ▶  $I_{\text{Hold}}$  (1PS) = 2-5 mA on at least 1 powered pairset
  - ▶ Support new MPS timings (6 ms / 354 ms)
- ▶ **PD Type 3, 4 (single signature,  $P_{\text{Class\_PD}} \geq \text{Class 5}$ )**
  - ▶  $I_{\text{Hold}}$  (Total) = 4-14 mA total current, or
  - ▶  $I_{\text{Hold}}$  (1PS) = 2-7 mA on at least 1 powered pairset
  - ▶ Support new MPS timings (6 ms / 354 ms)
- ▶ **PD Type 3, 4 (dual signature)**
  - ▶  $I_{\text{Hold}}$  (Each) = 2-7 mA per pair-set
  - ▶ Support new MPS timings (6 ms / 354 ms)

## PD Type 3/4 MPS Rules connected to...

### ▶ PSE Type 1, 2

- ▶  $I_{\text{Port\_MPS}}$  (Total) = 10 mA, total current
- ▶ Legacy timing: 75 ms / 250 ms

### ▶ PSE Type 3, 4 (single signature PD, $P_{\text{Class\_PD}} \leq \text{Class 4}$ )

- ▶  $I_{\text{Port\_MPS}}$  (Total) = 10 mA, total current
- ▶ New timing: 7 ms / 318 ms

### ▶ PSE Type 3, 4 (single signature PD, $P_{\text{Class\_PD}} \geq \text{Class 5}$ )

- ▶  $I_{\text{Port\_MPS}}$  (Total) = 16 mA, total current
- ▶ New timing: 7 ms / 318 ms

### ▶ PSE Type 3, 4 (dual signature PD)

- ▶  $I_{\text{Port\_MPS}}$  (2PS) = 8 mA, on every powered pair-set
- ▶ New timing: 7 ms / 318 ms