Concurrency issues in the PSE state diagram (D3.1) v100

Info (not part of baseline)

The PSE state diagram consists of 9 concurrently running state machines (not counting the 5 concurrent PSE DLL power control state machines):

- Figure 145–13 The top level
- Figure 145–14 PSE Autoclass
- Figure 145–15 SISM Primary
- Figure 145–16 SISM Secondary
- Figure 145–17 MPS (tmpdo_timer)
- Figure 145–18 The Primary and Secondary MPS (tmpdo_timer_pri and _sec)
- Figure 145–19 The inrush monitors (Primary and Secondary), slated for removal

As one can imagine, there is some risk of concurrency issues, given that all of these state machines operate on the same variable space. Specifically, the variables assigned in the ENTRY_PRI and ENTRY_SEC state clobber results in the top level state machine. To resolve this, a new (assignment free) state is introduced before ENTRY_PRI (which is renamed to INIT_PRI).

At least the variables pd_4pair_cand and sig_pri are overwritten continuously by the SISM state diagrams when sism=FALSE. This interferes with detection in the top level state diagram.

145.2.5.7 State diagrams

Change Figures in 145.2.5.7 as follows:

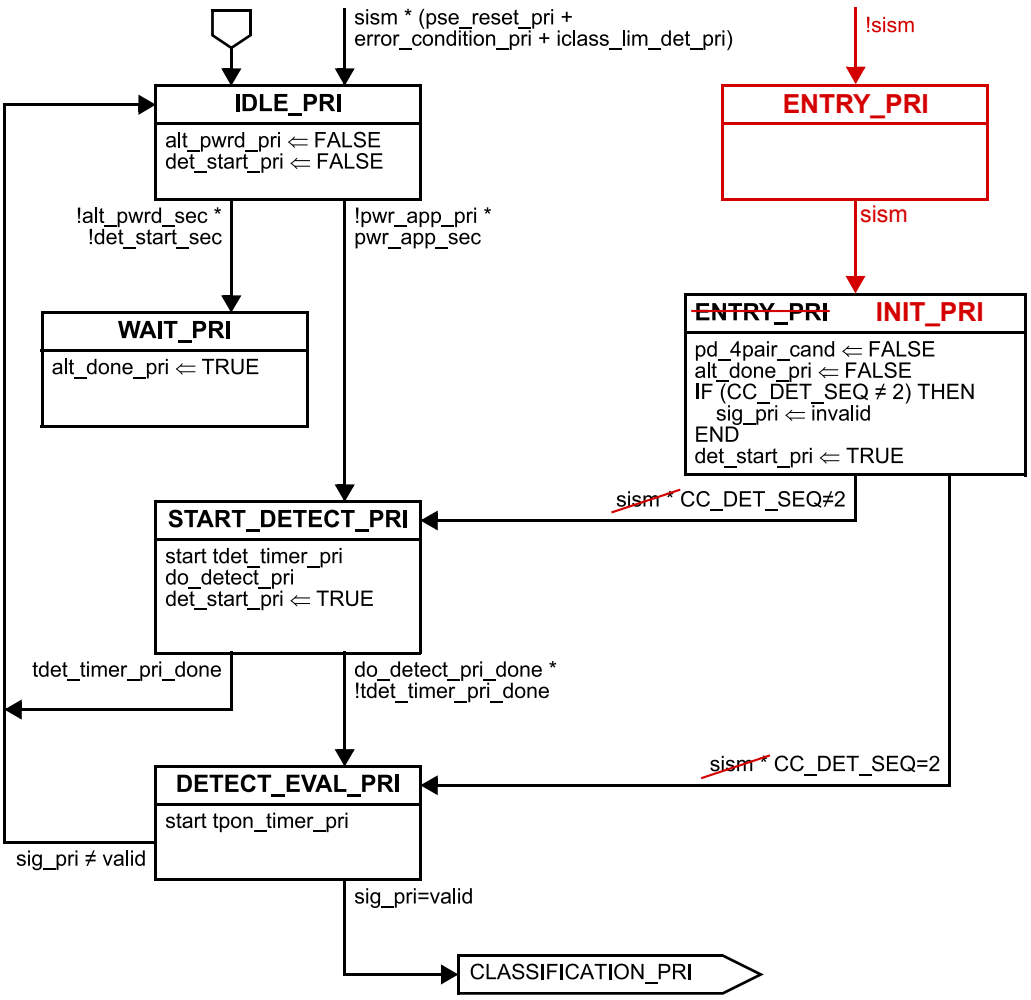

Figure 145–15—Primary Alternative dual-signature semi-independent PSE state diagram

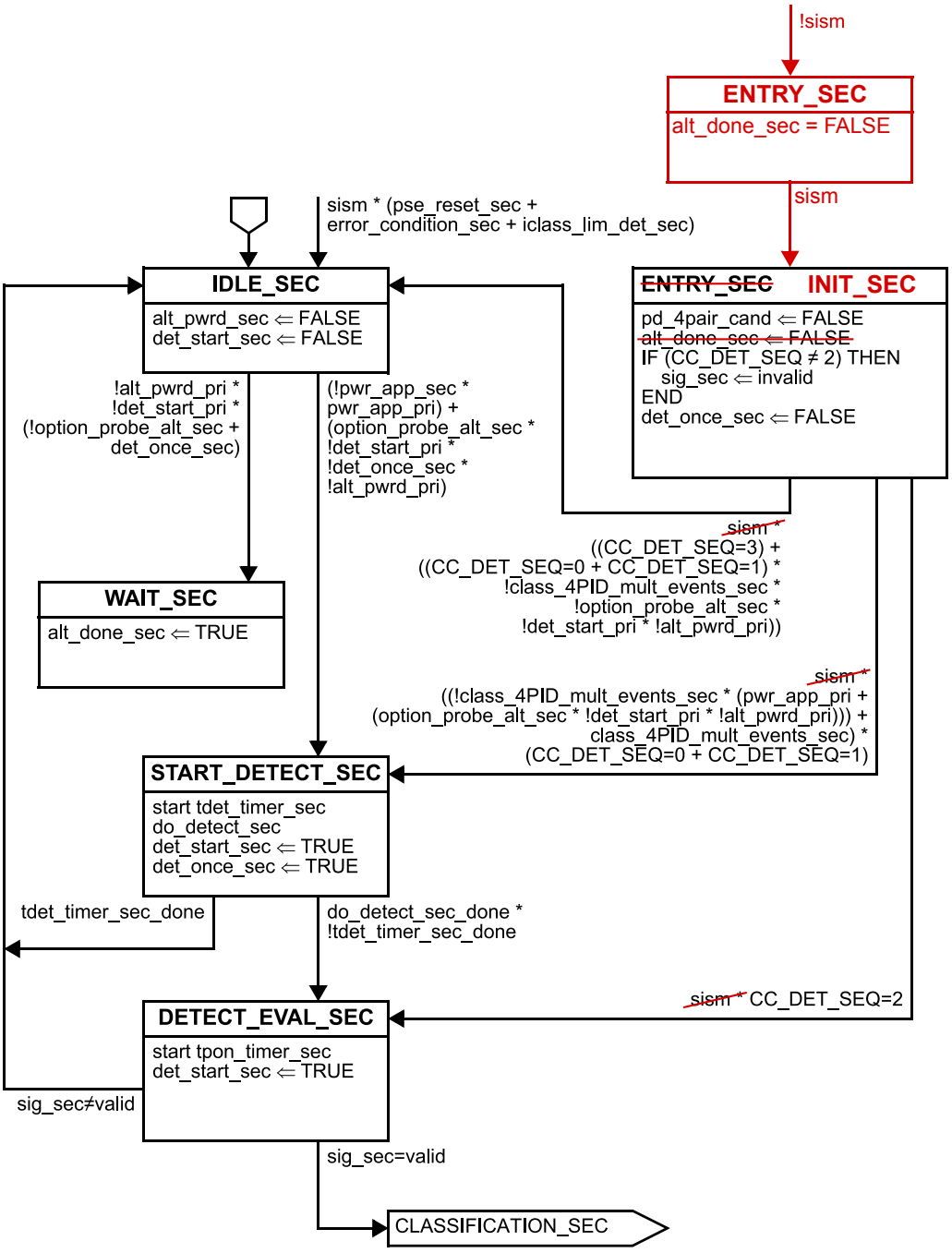

Figure 145–16—Secondary Alternative dual-signature semi-independent PSE state diagram