

Dual-signature Type 3 and Type 4 PD DLL state machine

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Power Matters

Objectives

- DLL for dual-signature PD connected to a PSE.
- Preferred with the same Figure 33-49 and Figure 33-50
- Cleanup and sync with clause 79, 33.6, 33.3.3.7.2 etc.
- Supports use cases with:
 - Power Demotion
 - -power is not sufficient for one of the modes or both modes.
 - Isolated load and common loads.
 - Single-signature and dual signature with the same SM.

Background -1: Single-Signature PDs.

- Figure 33-49 and Figure 33-50 managing the total power:
 - Port total power.
- As such it can support all Type 1,2 PDs/PSEs and Type 3/4 single-signature PDs and Type 3/4 PSEs if some comments will be implemented.
- Figure 33-49 and Figure 33-50 are not addressing power policing.
 - It is done in other places in the spec.

Background -2: Dual-Signature PDs.

- The existing Figure 33-49 and Figure 33-50 may support dual-signature PD if:
- The DLL state machine will be run on the total power per port.
 - In this case the policing can be done based on the physical layer only per pairset.
 - In this case Figure 33-49 an figure 50 can be used without modifications.

OR

- The DLL state machine will be run on mode A and then on Mode B (which will supply also the total power per port).
 - Totally independent DLL per pairset.
 - Supports power demotion
 - Support Power up/down/up sequences per pair set

Chosen Concept

- Independent DLL operation per mode.
 - Best technical solution.
 - And if we did it right, also looks the simplest.
 - Reuse of the same variable from clause 33.6 and clause 79.
 - Minimum changes for clause 79.
- Consecutive operation of the state machine on each pairset.

Concept: Consecutive Execution x2 Transactions



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Concept: Consecutive Execution x2 Transactions



Q&A - If we use total power concept, how power will be divided?

Step 1: PD wants on modeA=35W and on mode B=25W

Step 2: PSE supplies 72.8W to the port with protections of Class 5 to mode A and class 4 for mode B or class 5 for both.

Step 3: Now PSE has power budget limit of 60W.

Step 4: PD can decide:

- a) Operate mode A with 40W (as it was) and mode B with up to 14.5W so total PSE power is 60W.
- b) Operate mode A=40W shut of mode B or shut of both modes.
- c) If it is dual-sig PD with isolate load decision in made per pairset as with any independent load.
- d) If it is dual-signature single load, it behaves like single-signature PD when no sufficient power and power is divided ~0.5*Pclass per pairset and PD knows that.
- e) The information if it is isolated loads exists in the TLVs and available for the PSE and PD.

Q&A - If we use total power concept, does the power budget management is optimized?

- For dual-signature PD with single load: YES. It is the same as if single-signature PD was connected.
- For dual-signature PD with dual load (isolated) better performance and power policing can be achieved if DLL is run per pairset.
- Most of the dual-signature PDs are with dual load.

Q&A – what is the best technical concept?

- To run DLL over each pairset
- Supply the information of the power needs per pairset.
- The total power is known by PSE or PD or both by computing A+B power or by setting the information of it in the TLV fields.
- What ever the information we need to allow optimized performance we can add to the TLV (clause 79)
- PD DLL may or may not use it. It is implementation specific.
- What matters is to meet the minimum requirements of Figure 33-49 and Figure 33-50 in order to get the same quality of performance as with single-signature PDs.

Thank You

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To consider: Consecutive Execution x1 Transaction

