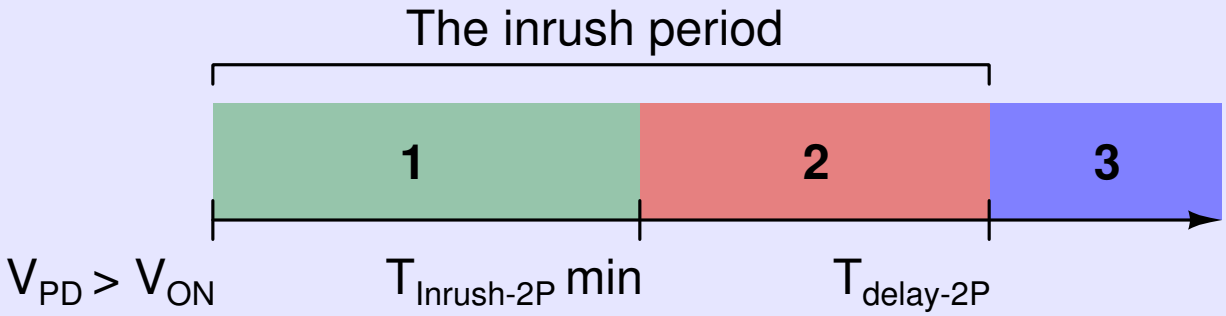
PD Inrush 33.3.7.3 cleanup v120

Info (not part of baseline)

The PD inrush section was rather obscure to begin with. Since this section has been tweaked nearly every draft, to the further detriment of the text. This has not improved the clarity of the text. This is a clean re-write based on the actual PD requirements. The D1.7 version and the 802.3-2015 version are included at the end.

Timing overview:



What are the real requirements on PDs in each of these periods ?

1. This is the time between the crossing of V_{On_PD} and $T_{Inrush-2P}$ min later. There are no specific requirements for PDs during this time. Inrush is limited by the PSE during this period.
2. This is the time between $T_{Inrush-2P}$ min and $T_{delay-2P}$. PDs need to make sure they have taken control of the input current and restrict it to less than I_{Inrush_PD} and I_{Inrush_PD-2P}. This requirement also encapsulates that a PD may not switch to a high power state (it cannot do so without violating I_{Inrush_PD} and I_{Inrush_PD-2P}).

   In addition there is a quirck that assigned Class 1,2 and 3 PDs need to take into account. They are required to restrict their power consumption below P_{Class_PD} or P_{Class_PD-2P} because the PSE may already enforce Class power at $T_{Inrush-2P}$ min.
3. Finally, this is the time after $T_{delay-2P}$. After this time the PSE is guaranteed to be in POWER_ON and the PD needs to follow the normal rules of MDI_POWER2.

33.3.7.3 Input inrush current

Replace the first two paragraphs of 33.3.7.3 (excluding the Editors Notes) by the following:

The inrush period is defined as beginning with the application of input voltage at the PI when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD} as defined in Table 33–28, and ends after $T_{delay-2P}$.

The inrush current is the initial current drawn by the PD, which is used to charge C_{Port} or $C_{Port-2P}$. The inrush current is limited by the PSE, and may be further limited by the PD to allow for large values of C_{Port} and $C_{Port-2P}$.

PDs shall draw less than I_{Inrush_PD} and I_{Inrush_PD-2P} from $T_{Inrush-2P}$ min until $T_{delay-2P}$ min. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to change the available current from the POWER_UP to the POWER_ON limits.

Single-signature PDs assigned to Class 1, 2, or 3 shall draw less than P_{Class_PD} within $T_{Inrush-2P}$ min as defined Table 33–17. Type 3 and Type 4 dual-signature PDs assigned to Class 1, 2, or 3 shall draw less than P_{Class_PD-2P} within $T_{Inrush-2P}$ min as defined Table 33–17 on that pairset.

The PD shall meet the inrush current requirements with the PSE behaviour described in 33.2.8.5.

$I_{Port\text{-}2P}$ is the current on a pairset as defined in 33.2.8.4

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with $V_{port\_PD\text{-}2P}$ requirements as defined in Table 33–28, and ending when C_{Port} has reached a steady state and is charged to 99% of its final value. This period shall be less than $T_{Inrush\text{-}2P}$ min per Table 33–17, with the PSE minimum inrush behavior defined in 33.2.8.5. Type 1, Type 2, and Type 3 PDs shall consume a maximum of Type 1 power for at least $T_{delay\text{-}2P}$ min, Type 4 PDs shall consume a maximum of Class 2 power for at least $T_{delay\text{-}2P}$ min. This allows the PSE to properly complete inrush.

Editor's Note: This paragraph needs further review as the requirement to charge the capacitor does not apply to PDs that limit their inrush current.

Editor's Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277.

$T_{delay\text{-}2P}$ for each pairset starts when V_{PD} crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time change the available current on each pairset from $I_{Inrush\text{-}2P}$ to $I_{Con\text{-}2P}$.

Input inrush currents at startup, I_{Inrush_PD} and $I_{Inrush\_PD\text{-}2P}$, as defined in Table 33–17, are limited by the PSE if $C_{Port} < 180$ µF for single-signature PDs assigned to Class 0 to 6, and if $C_{Port} < 360$ µF for PDs assigned to Class 7 or 8. Input inrush current at startup, $I_{Inrush\ PD\text{-}2P}$, is limited by the PSE if $C_{Port\text{-}2P} < 180$ µF for dual-signature PDs. If a PD has a larger C_{Port} or $C_{Port\text{-}2P}$ value, then the PD shall limit the input inrush current such that I_{Inrush_PD} max and $I_{Inrush\_PD\text{-}2P}$ max, as defined in Table 33–17, are met.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush\text{-}2P}$ min. See 33.2.8.4 for details.

C_{Port} in Table 33–28 is the total PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load when operating one or both pairsets, when connected to a single-signature PD. $C_{Port\text{-}2P}$ in Table 33–28 is the PD input capacitance during the POWER_UP and POWER_ON states that a PSE sees as load on each pairset independently, when connected to a dual-signature PD. See Figure 33–37 for a simplified PSE-PD C_{Port} and $C_{Port\text{-}2P}$ interpretation model.

33.3.7.4 Peak operating power

$V_{Overload\text{-}2P}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, with the exception of Class 6 or Class 8 PDs when additional channel DC resistance information is available to the PD, the peak power shall not exceed P_{Class_PD} max for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–17 and 5% duty cycle. Peak operating power shall not exceed P_{Peak_PD}.

For Class 6 and Class 8 PDs, when additional information is available to the PD regarding actual channel DC resistance, in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Class} at the PSE PI for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–17 and with 5% duty cycle.

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

V_{Port_PD} is the static input voltage at the PD PI
I_{Port} is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99% of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180$ μF, as specified in Table 33–11.

If $C_{Port} \geq 180$ μF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

33.3.7.4 Peak operating power

$V_{Overload}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

$$I_{Port} = \left\{ \sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2} \right\}_A \quad (33–10)$$

where
I_{Port} is the RMS input current
I_{Port_dc} is the DC component of the input current
I_{Port_ac} is the RMS value of the AC component of the input current

The maximum I_{Port} value for all operating V_{Port_PD} range shall be defined by the following equation:

$$I_{portmax} = \left\{ \frac{P_{Class\_PD}}{V_{Port\_PD}} \right\}_A \quad (33–11)$$

where
$I_{portmax}$ is the maximum DC and RMS input current
V_{Port_PD} is the static input voltage at the PD PI
P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18