PSE state machine related issues (Comment r02-137, 145.2.7 *P* 144 *L* 33)

In comment r01-174 (D3.1) we did some changes that are not required
In the exit from CLASS_EV2 to MARK_EV2 we add the variable "*(pse_alternative=both)"
In the exit from CLASS_EV2 to MARK_EV_LAST we add the variable "*(pse_alternative !=both)"
This is not required since the argument that was used to justify this change can't happen
since pse_allocated_pwr is set to 4 in CLASS_EV2 and can't be higher than 4.

SuggestedRemedy

Restore to D3.1 all the changes done for comment r01-174.

PROPOSED REJECT.

This change was implemented to make sure that 2-pair PSEs don't give more than 2 class events (since they can't ever supply more than class 4).

Yair:

(1) I disagree that this was the reason for the change i.e. that 2-pair PSE don’t give more than 2-class events if pse_avail_pwr=4. If pse_avail_pwr>4 it can issue 3 class events for 4-pairs but the 4-pair test should not be done here at the exit from CLASS_EV2. It is already done at the exits of CLASS_EV3.

The facts are:

a) When pse_avail_pwr=4, PSE working over 2-pais OR 4-pairs, can issue 3 class events if option_2ev=FALSE. It has the same meaning for the PD in terms of available power.

b) Lennart in his corner case presented in r01-174, explained that in the exit from CLASS_EV2 to MARK_EV2 the reason for his proposed changes was to address the corner case when option_2ev=TRUE and yet we issue 3 class events in the exit from CLASS_EV2 to MARK_EV2 which is the wrong way to address it.
-We issue 3 class events because pse_avail_power>4 and !option_2ev=0 which is still the correct logic in this exit. The correct way to fix his is shown below in (3).

(2) The other problem that I had is that Lennart in his arguments to r01-175 mention pse_allocated_pwr>4 which can't be the reason for the proposed changed in D3.1 since pse_allocated_pwr=4 was already assigned in CLASS_EV2. I guess it was a typo and Lennart meant to say pse_avail_pwr>4. (Lennart **confirmed it.)**

(3) The logic of the exit from CLASS_EV2 to MARK_EV2 is incorrect because this exit is only about the conditions to permit 3 class events when the 2nd pd_class_sig=4 regardless if PSE is operated over 2-pairs or 4-pairs since this condition is tested already at the exits of CLASS_EV3 and should not be tested now. The only ways to exit from CLASS_EV2 to MARK_EV2 are:

a) tcev_timer_done *(pd_class_sig = 4) * !option_2ev * (pse_avail_pwr = 4) [This solve Lennart problem in r01-174]

OR

b) tcev_timer_done *(pd_class_sig = 4) * (pse_avail_pwr > 4) [this allows 3 class events for the normal path when pse_avail_power>4 regardless of option_2ev] which results with:

tcev_timer_done * (pd_class_sig = 4) * ((pse_avail_pwr > 4) + ((pse_avail_pwr = 4) * !option_2ev))

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(4) The logic of the exit from CLASS_EV2 to MARK_EV_LAST done to prevent multiple true due the changes made for CLASS_EV2 to MARK_EV2 and is not required due to the above discussion i.e.:
tcev_timer_done *(pd_class_sig = 4) * option_2ev * ~~(~~ (pse_avail_pwr = 4) +~~(pse_alternative!=BOTH)~~) as it was in D3.1.

Proposed Remedy:

1. Change the exit from CLASS_EV2 to MARK_EV_LAST from:

tcev_timer_done *option_2ev *((pse_avail_pwr = 4) +(pse_alternative ≠ both)) *(pd_class_sig = 4)

To:

tcev_timer_done *option_2ev *(pse_avail_pwr = 4) * (pd_class_sig = 4)

2. Change the exit from CLASS_EV2 to MARK_EV2 from:

tcev_timer_done * (pd_class_sig = 4) * (((pse_avail_pwr > 4) * (pse_alternative = both)) + !option_2ev)

To:

tcev_timer_done * (pd_class_sig = 4) * ((pse_avail_pwr > 4) + ((pse_avail_pwr = 4) * !option_2ev))

New comment (not submitted. Clause 145.3.3.3.5 Page 191 line 48*)*

In the PD state machine in NOPOWER we have the assignment pse_power_level 🡐8 that may cause overload condition in the PSE whenever the assigned power is lower than the required power.
The overload condition happens when we force compliant PDs in NOPWER that do remember their assigned class (and their pse_power_level) data to redefine their pse_power_level in NOPOWER to higher power level in NOPWER when PSE has no knowledge about it.

The assignment pse_power_level 🡐8 in NOPOWER looks redundant at least if the PD remembers its pse_power_level when PD input voltage is above VReset_PD_max (2.81V), or VReset_th_max (6.9V) which ensures sufficient voltage to PD to keep its memory.

Asking PD to assign pse_power_level 🡐8 in NOPOWER for VPD<VOff_PD_min without specifying that the lowest value for VPD<VOff_PD_min is VReset_th_max is the issue.

Example for the problem:

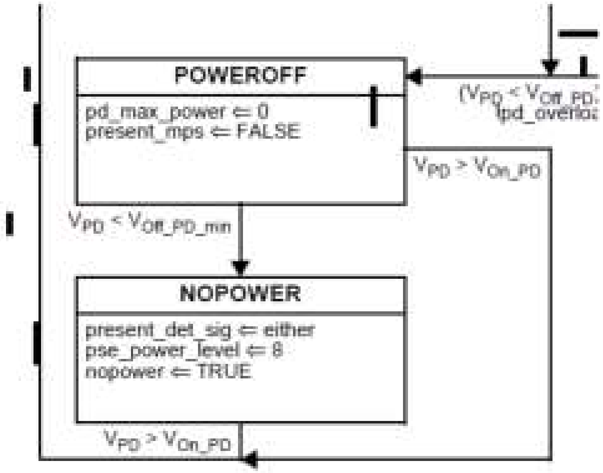
a) *PD requested class is 8 and the assigned class is* 6*.*
b) *When transitioning from NOPWER back to POWERED, the PSE has still available power of* 6 *(that is why it has assigned class to* 6*) and now power level is 8.*
   The pse_power_level=8 will cause the pse_assign_class in POWER_DELAY to be:
   *pse_assign_class = min(pse_power_level, pd_req_class)=min(8,8)=*8*.*
   This in turn will set pd_max_power in POWERED to be:
   pd_max_power 🡐 min (pse_assigned_class, pd_req_class)=min(8, 8)=8 which is > pse_available power =6 🡒 PSE OVERLOAD condition.

This comment tries to *minimize* *the exposure of a compliant PD that do remember its pse_power_level to be forced to reassign pse_power_level to 8 which will cause that PD to cause PSE overload which is uncompliant behavior after that PD that didn't go to IDLE was behave in a compliant way.*

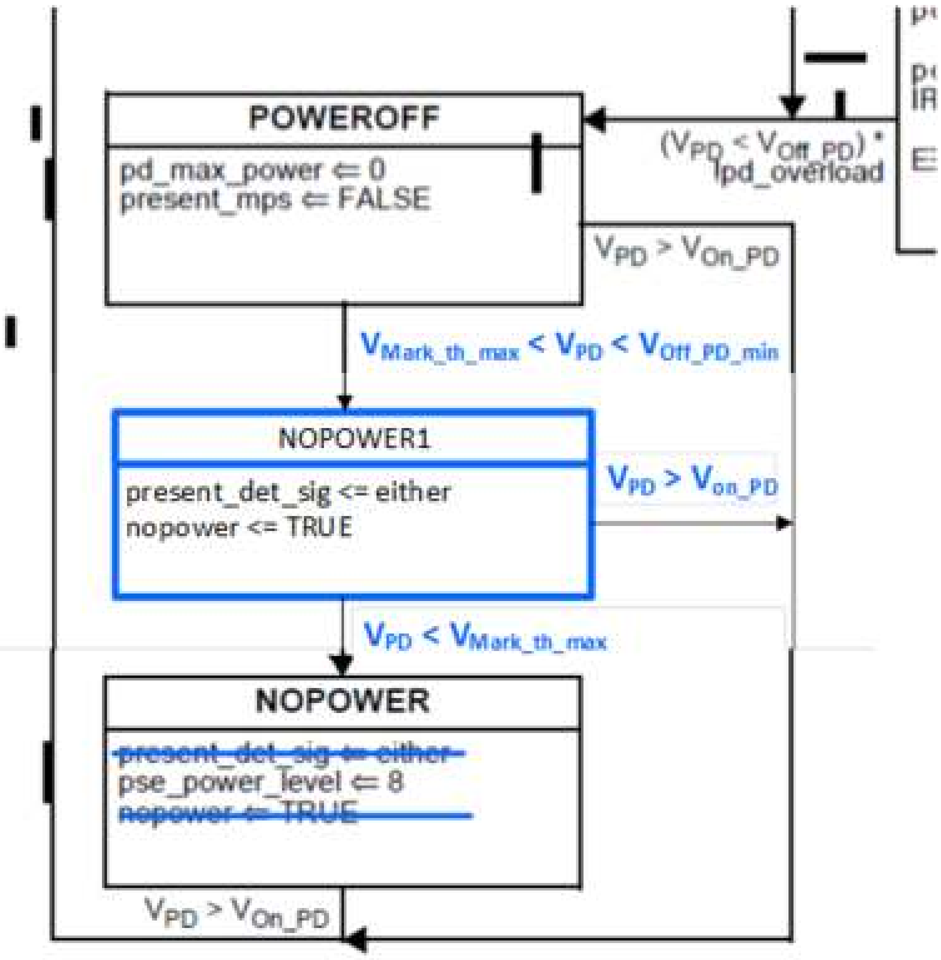
The proposed remedy is based on reducing the input voltage range in which we are forced to assign pse_power_level to 8 from: Vpd < VOff_PD_min to: Vmark_th_max < Vpd < VOff_PD_min.

Proposed Remedy:

1. ***Chane state machine from:***



To:



2. Repeat the proposed changes for dual-signature PD.

End of Remedy

Annex

1.4.417 Type 2 PD: A PD that requests Class 4 during Physical Layer classification, supports 2-Event Classification, and supports Data Link Layer classification (see IEEE 802.3, Clause 33).

1.4.418aa Type 3 PD: A single-signature PD that requests Class 1 to Class 6, or a dual-signature PD that requests Class 1 to Class 4 on both Modes, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification, and accepts power on both Modes simultaneously. (See IEEE 802.3, Clause 145).

1.4.418ac Type 4 PD: A single-signature PD that requests Class 7 or Class 8, or a dual-signature PD that request Class 5 on at least one Mode, during Physical Layer classification. Additionally, the PD implements Multiple-Event classification, is capable of Data Link Layer classification, and accepts power on both Modes simultaneously. (See IEEE 802.3, Clause 145).

option_2ev

This variable indicates if PSE will generate 2 or 3 class events when ***pse_avail_pwr is 4***.

Values:

FALSE: The PSE is not restricted to 2 class events when pse_avail_pwr is 4.

TRUE: The PSE is restricted to 2 class events when pse_avail_pwr is 4.

Conclusions:
option_2ev is used only when pse_allocated_pwr=4 which results with ***pse_avail_pwr = 4*** . It is relevant for PSEs that works over 2-pairs or 4-pairs.

pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the PI (see Table 145–3).

Values:

a: The PSE uses PSE pinout Alternative A.

b: The PSE uses PSE pinout Alternative B.

both: The PSE uses both Alternative A and Alternative B.

pse_allocated_pwr

A variable that indicates the Class that has been assigned to the PD.

Values:

0: No power has been assigned to the PD
1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

pse_avail_pwr

This variable indicates **the highest Class the PSE may assign to the PD** by Physical Layer classification.

The value is restricted to the allowed range defined in Table 145–6 and set in an implementation-specific manner.

Values:

1: Class 1
2: Class 2
3: Class 3
4: Class 4
5: Class 5
6: Class 6
7: Class 7
8: Class 8

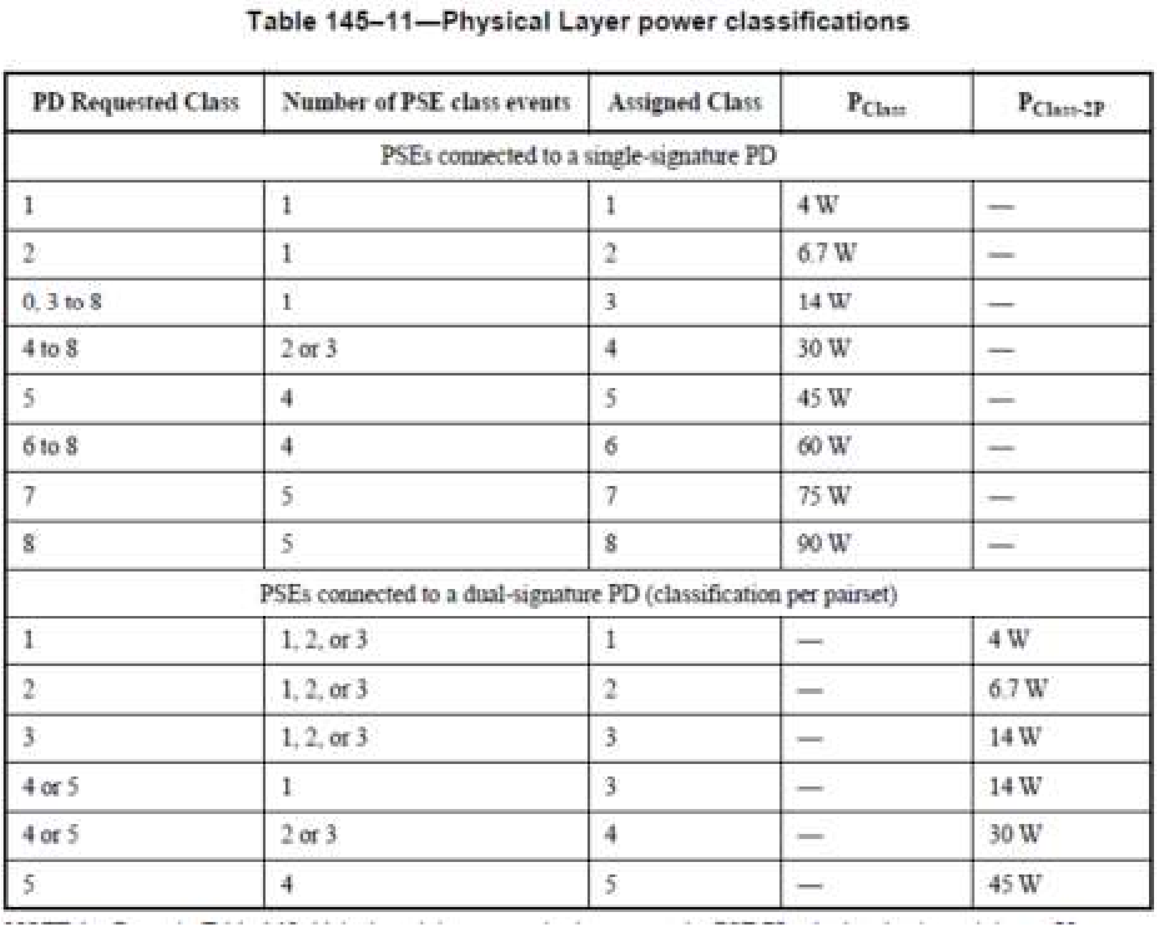


Table 145–11—Physical Layer power classifications

PD Requested Class	Number of PSE class events	Assigned Class	P_{Class}	$P_{Class\text{-}2P}$
PSEs connected to a single-signature PD				
1	1	1	4 W	—
2	1	2	6.7 W	—
0, 3 to 8	1	3	14 W	—
4 to 8	2 or 3	4	30 W	—
5	4	5	45 W	—
6 to 8	4	6	60 W	—
7	5	7	75 W	—
8	5	8	90 W	—
PSEs connected to a dual-signature PD (classification per pairset)				
1	1, 2, or 3	1	—	4 W
2	1, 2, or 3	2	—	6.7 W
3	1, 2, or 3	3	—	14 W
4 or 5	1	3	—	14 W
4 or 5	2 or 3	4	—	30 W
5	4	5	—	45 W