Cl **30** *SC* **30.9.1.1** *P* **35** *L* **8** # i-350

Thompson, Geoffrey Individual

Comment Type **TR** *Comment Status* **X** *Management*

It would appear that all of the strikethrough in this clause is incorrect as it constitutes a change to cl. 33. It is easily possible that the affected text could be improved but it is not proper to remove.

SuggestedRemedy

Restore stricken text in 30.9.1.1. Consider improvements to the text.

Proposed Response *Response Status* **W**

TFTD

This is addressed in a bunch of comments from Lennart. Let's revisit and make sure we have satisfied this comment.

LDR GT
Says we need to revisit, therefore we should discuss before a broad set of eyes. Perhaps later in the session after we are ito things.

Cl **30** *SC* **30.9.1.1.1** *P* **35** *L* **21** # i-351

Thompson, Geoffrey Individual

Comment Type **TR** *Comment Status* **D** *Pres: Yseboodt5*

Reference to control registers in cl. 145 is missing.

SuggestedRemedy

Add reference to cl. 145 after the reference to cl. 33.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The reference cannot be added as there are no comment remedies that create a section of clause 145 to point to.

TFTD

Cl **30** *SC* **30.9.1.1.4** *P* **36** *L* **15** # i-262

Stewart, Heath Analog Devices Inc.

Comment Type **TR** *Comment Status* **X** *Pres: Darshan5*

It is unclear how the disparate SISM states will be described. For example if the primary is powered and the secondary is searching, what will the returned state value be?

SuggestedRemedy

Either remove support for dual-signature PDs or complete their specification throughout the standard.

Proposed Response *Response Status* **W**

TFTD

TFTD LY
The following objects: aPSEPowerDetectionStatus, aPSEPowerClassification, and maybe a few others (30.9.1.1.7, 30.9.1.1.8, 30.9.1.1.11) need to get dual-signature equivalents for each pairset. People who care about dual-signature please to provide baseline at the meeting.

TFTD YD
See darshan_05_0917.pdf

WFP

Cl **30** *SC* **30.9.1.1.7** *P* **37** *L* **25** # i-263

Stewart, Heath — Analog Devices Inc.

Comment Type **TR** *Comment Status* **X** *Pres: Darshan5*

The PSEPowerDeniedCounter is only specified for Type 1 and Type 2 state machine references. It is not clear if this was intention or if references to Type 3 and Type 4 should be added.
Currently:
This counter is incremented when the PSE state diagram (Figure 33-9) enters the state POWER_DENIED.

SuggestedRemedy

Option 1 Change
"(Figure 33-9) enters the state POWER_DENIED"
to
"(Figure 33-9, Figure 145-13, Figure 145-15, or Figure 145-16) enters the state POWER_DENIED, POWER_DENIED_PRI, or POWER_DENIED_SEC"
Option 2 Change
"when the PSE"
to
"when the Type 1 and Type 2 PSE"

Proposed Response *Response Status* **W**

TFTD

I somewhat remember a conversation about not supporting this for Type 3/4, am I remembering correctly?

TFTD LY
That is for the aPSEInvalidSignatureCounter…

WFP

Cl **30** *SC* **30.9.1.1.8** *P* **37** *L* **35** # i-33

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *Pres: Darshan5*

This object was modified to work with Clause 145, but was not updated after the Clause split.
"This counter is incremented when the PSE state diagram (Figure 145-13, Figure 145-15, and Figure 145-16) enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC."

SuggestedRemedy

Replace by:
"For Type 1 and Type 2 PSEs, this counter is incremented when the PSE state diagram in Figure 33-9 enters the state ERROR_DELAY.
For Type 3 and Type 4 PSEs, this counter is incremented when the PSE state diagram in Figure 145-13, Figure 145-15, and Figure 145-16 enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC."

Proposed Response *Response Status* **W**

TFTD

You reference the sisms in this remedy, does that make sense?

TFTD DS
I recall agreeing Clause 145 support would not be integrated into Clause 30. Why are we adding references to Type 3 and 4 operation for only this attribute?

WFP

Cl **30** *SC* **30.9.1.1.8** *P* **37** *L* **41** # i-264

Stewart, Heath — Analog Devices Inc.

Comment Type **E** *Comment Status* **X** *Pres: Darshan5*

The reference to Figure 33-9 has been accidentally deleted.

SuggestedRemedy

Change "(Figure 145-23, " to "(Figure 33-9, Figure 145-13, "

Proposed Response *Response Status* **W**

TFTD

see 33

Cl **30** *SC* **30.9.1.1.11** *P* **38** *L* **2** # i-265

Stewart, Heath — Analog Devices Inc.

Comment Type **TR** *Comment Status* **X** *Pres: Darshan5*

The PSEMPSAbsentCounter is only specified for Type 1 and Type 2 state machine references. It is not clear if this was intention or if references to Type 3 and Type 4 should be added.
Currently:
This counter is incremented when the PSE state diagram (Figure 145-13, Figure 145-15, and Figure 145-16) enters the state ERROR_DELAY, ERROR_DELAY_PRI, or ERROR_DELAY_SEC.

SuggestedRemedy

Option 1 Change
"transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted"
to
"transitions directly from the state POWER_ON, SEMI_PWR_PRI, SEMI_PWR_SEC, POWER_ON_PRI, or POWER_ON_SEC to the state IDLE due to tmpdo_timer_done, tmpdo_timer_done_pri or tmpdo_timer_done_sec being asserted"
Option 2 Change
"when the PSE"
to
"when the Type 1 and Type 2 PSE"

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **30** *SC* **30.9.2** *P* **38** *L* **19** # i-352

Thompson, Geoffrey — Individual

Comment Type **TR** *Comment Status* **X** *Management*

Comment is out of the scope of the project.

SuggestedRemedy

Delete this line in the draft

Proposed Response *Response Status* **W**

TFTD

Lennart to provide full remedy.

Cl **30** *SC* **30.12.2.1...** *P* **40** *L* # i-355

Thompson, Geoffrey — Individual

Comment Type **E** *Comment Status* **X** *Management*

I don't understand why each attribute has a "regular" version and a local LLDP version

SuggestedRemedy

Please explain.

Proposed Response *Response Status* **W**

TFTD

Someone with management expertise, please provide a response.

LDR GT

Find Mr. Law…

Cl **30** *SC* **30.12.2.1.18i** *P* **42** *L* # i-319

Law, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt4*

The aLldpXdot3LocPowerClassxA, aLldpXdot3LocPowerClassxB, aLldpXdot3RemPowerClassxA and aLldpXdot3RemPowerClassxB attributes don't seem to map to any of the TLV fields defined in subclause 79.3.2 or its subclauses.

SuggestedRemedy

Suggest that:

[1] Delete attributes aLldpXdot3LocPowerClassxA (subclause 30.12.2.1.18i , page 42, line 22), aLldpXdot3LocPowerClassxB (subclause 30.12.2.1.18j, page 42, line 33), aLldpXdot3RemPowerClassxA (subclause 30.12.3.1.18g, page 51, line 29) and aLldpXdot3RemPowerClassxB (subclause 30.12.3.1.18h, page 51, line 41).

[2] Remove entries for aLldpXdot3LocPowerClassxA, aLldpXdot3LocPowerClassxB, aLldpXdot3RemPowerClassxA and aLldpXdot3RemPowerClassxB from Table 30-7 'LLDP capabilities' (page 32, line 38).

Proposed Response *Response Status* **W**

TFTD

I assume these were added for DS…

TFTD LY
Should be addressed by yseboodt 04

Cl **30** *SC* **30.12.2.1.18k** *P* **42** *L* **3** # i-322

Law, David — Hewlett Packard Enter

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt4*

There are no attributes provided in the subclause 30.12.2 'LLDP Local System Group managed object class' or subclause 30.12.3 'LLDP Remote System Group managed object class' for the TLV fields 'Dual-signature power Classx Mode A' and 'Dual-signature power Classx Mode B'.

SuggestedRemedy

Suggest that:

[1] The following new attributes are added in the LLDP local (aLldpXdot3LocDualSigPowerClassxModeA and aLldpXdot3LocDualSigPowerClassxModeB) and remote (aLldpXdot3RemDualSigPowerClassxModeA and aLldpXdot3RemDualSigPowerClassxModeB) managed object class to support the TLV fields 'Dual-signature power Classx Mode A' and 'Dual-signature power Classx Mode B'.

aLldpXdot3LocDualSigPowerClassxModeA

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:
singleSignature Single-signature PD
class5 Class 5
class4 Class 4
class3 Class 3
class2 Class 2
class1 Class 1

BEHAVIOUR DEFINED AS:
If the local system is a PD, a read-only value that indicates if it is a single-signature PD, or for a dual-signature PD, the requested Class for Mode A during Physical Layer Classification (see 145.3.6). If the local system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, the assigned Class for Alternative A (see 145.2.7).

aLldpXdot3LocDualSigPowerClassxModeB

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:
If the local system is a PD, a read-only value that indicates if it is a single-signature PD, or for a dual-signature PD, the requested Class for Mode B during Physical Layer Classification (see 145.3.6). If the local system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, the assigned Class for Alternative B (see 145.2.7).

aLldpXdot3RemDualSigPowerClassxModeA

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:
If the remote system is a PD, a read-only value that indicates if it is a single-signature PD, or if it is a dual-signature PD, its requested Class for Mode A during Physical Layer Classification (see 145.3.6). If the remote system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, its assigned Class for Alternative A (see 145.2.7).

aLldpXdot3RemDualSigPowerClassxModeB

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aLldpXdot3LocDualSigPowerClassxModeA.

BEHAVIOUR DEFINED AS:
If the remote system is a PD, a read-only value that indicates if it is a single-signature PD, or if it is a dual-signature PD, its requested Class for Mode B during Physical Layer Classification (see 145.3.6). If the remote system is a PSE, a read-only value that indicates if it has detected a single-signature PD, or if it has detected a dual-signature PD, its assigned Class for Alternative B (see 145.2.7).

[2] Mappings for two of the new attributes are added in Table 79-9 'IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references'. Suggest that the following two new entries are inserted between the row 'PSE power pairx' 'aLldpXdot3LocPowerPairsx' and the row 'Power classx' 'aLldpXdot3LocPowerClassx'.

'Dual-signature power Classx Mode A' 'aLldpXdot3LocDualSigPowerClassxModeA'
'Dual-signature power Classx Mode B' 'aLldpXdot3LocDualSigPowerClassxModeB'

[3] Mappings for two of the new attributes are added in Table 79-10 'IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references'. Suggest that the following two new entries are inserted between the row 'PSE

power pairx' 'aLldpXdot3RemPowerPairsx' and the row 'Power classx' 'aLldpXdot3RemPowerClassx' in both tables.

'Dual-signature power Classx Mode A' 'aLldpXdot3RemDualSigPowerClassxModeA'
'Dual-signature power Classx Mode B' 'aLldpXdot3RemDualSigPowerClassxModeB'

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **33** *SC* **33.4.6** *P* **64** *L* **34** # i-227

Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** *Comment Status* **D** *AES*

E_d_out is a time domain peak to peak voltage but the formula defines E_d_out as varying across frequency. E_d_out isn't measured at individual frequencies.

SuggestedRemedy

delete formula (33-17a) and the text defining f and fmax
change text on line 31 from:
"shall not exceed the requirements Equation (33-17a)" (note the missing 'of')
to "shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD GZ
Reason: i-219 is already TFTD and these are the same comment/issue. We are double checking on the level and test method as to whether we can just do an accept on both of these.

Cl **33** *SC* **33.4.9.1.2** *P* **66** *L* **10** # i-238

Zimmerman, George Aquantia, ADI, Comm

Comment Type **TR** *Comment Status* **D** *AES*

Missing requirement for 10GBASE-T in clause 33 (this one is OK in clause 145, just missed in clause 33)

SuggestedRemedy

Insert new equation 33-19a identical to 33-19 except 0.040 is changed to 0.020. Add text "For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 209

TFTD YD
Need to check

Cl **33** *SC* **33.4.9.1.2** *P* **66** *L* **10** # i-209

Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** *Comment Status* **D** *Pres: Zimmerman1*

missing a requirement for 10GBASE-T

SuggestedRemedy

insert new equation 33-19 identical to 33-19 except 0.040 is changed to 0.020.
Add text " For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD GZ

WFP

insert new equation 33-19a identical to 33-19 except 0.040 is changed to 0.020.
Add text " For 10GBASE-T capable midspans, insertion loss for Midspan PSE devices shall meet the values determined by Equation (33-19a) when measured for the transmit and receive pairs from 1 MHz to 500 MHz."

TFTD YD
Too tight. Channel has sufficient margin. No need to tighten Midspan connector.

Cl **79** *SC* **79** *P* **73** *L* **1** # i-38

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt4*

Dual-signature LLDP is incompletely and incorrectly defined.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDP.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **79** *SC* **79.3.2** *P* **81** *L* **33** # i-395

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

The 4PID bit need to move to legacy TLV field in order to support legacy PDs.
This will resolve also comment #130 from D2.4.

SuggestedRemedy

In Table 79-6d PD 4PID bit: Move this bit to Table 79-4 to bit 3:2 instead of the reserve bits. Make the PD 4PID bit as the reserved bits.

Proposed Response *Response Status* **W**

TFTD

Can we add to the legacy fields? I thought a Type 1/2 PD can use the fields of the new TLVs as long as some fields were 0.

TFTD LY
OBE to yseboodt 04

TFTD YD
See yseboodt_04_0917.pdf for LLDP adhoc proposed baseline

Cl **79** *SC* **79.3.2.6f** *P* **82** *L* **21** # i-460

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt7*

Table 79-6f describes autoclass field. Per the draft, autoclass can be requested any time including after the physical layer autoclass after transitioning to POWER_ON.
The are some issues that appear to be not closed.
In the case PD is and PSE supporting LLDP: Why PD will ask for autoclass through LLDP if he can do similar task by LLDP? I am asking this question since if PD eventually do this, it add a level of complexity (that can be resolved) that yet is not addressed in the standard.
for example:
a) There is no syncing or handshake mechanism defined to verify that the PD won't start to consume more power than the PSE allows it to draw, before the PSE is ready for it
b) It is also not covered in the state machine diagram at page 131 line 43, when moving from IDLE_ACS to MEASURE_ACS.
To resolve this, we need at least to add new variable "dll_autoclass_pd_pse_ready". This variable will indicate that PD has set it's requested power level for the PSE to be measure and the PSE has the available power to measure the PD requested power without going to overload/Ilim 2p condition.

SuggestedRemedy

1. add new variable "dll_autoclass_pd_pse_ready" to the variable list in 145.2.5.4 with the following definition:
"dll_autoclass_pd_pse_ready
This variable indicates that PD has set it's requested power level for the PSE to be measure and the PSE has the available power in order to stay powered and to measure the PD requested power without going to overload/Ilim 2p condition."
2. In the state machine in page 131 line 43 in the exit from IDLE_ACS to MEASURE_ACS, change from:
"MirroredPDAutoclassRequest"
To: "MirroredPDAutoclassRequest*dll_autoclass_pd_pse_ready"

Proposed Response *Response Status* **W**

TFTD

I thought Lennart added (or was planning to add LLDP support for Autoclass)…

TFTD DS
WFP yseboodt_07_0917_pdautoclassfix.pdf

Cl **145** *SC* **145.1** *P* **95** *L* **7** # i-364

Thompson, Geoffrey Individual

Comment Type **ER** *Comment Status* **X** *Pres: Thompson??*

There is no clear statement of the top level model of a PoE system in clause 145.1. such a statement is essential for someone reading the standard for the first time in order for the reader to figure out how to structure his thinking and to parse the problem.

SuggestedRemedy

See proposed text in submitted file GOT - Proposed text.txt. Pick existing text back up at the start of the list at line 27.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.1** *P* **95** *L* **9** # i-43

Yseboodt, Lennart Philips Lighting

Comment Type **E** *Comment Status* **X** *Pres: Thompson*

"This clause defines the functional and electrical characteristics for providing an enhancement of the Power over Ethernet (PoE) system defined in Clause 33 for deployment over balanced twisted-pair cabling."

Makes it seem that Clause 145 is an 'add-on' to Clause 33. It isn't, it is a complete, standalone PoE Clause.

SuggestedRemedy

"This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system originally defined in Clause 33 for deployment over balanced twisted-pair cabling."

Proposed Response *Response Status* **W**

TFTD

This new text makes it seem that an "enhanced PoE system" was defined in Clause 33.

TFTD LY
True... Maybe split up: “This clause defines the functional and electrical characteristics of an enhanced Power over Ethernet (PoE) system for deployment over balanced twisted-pair cabling. The original PoE system is defined in Clause 33”.

TFTD CJ
Surprised you just didn’t suggest this as the remedy: "This clause defines the functional and electrical characteristics of a Power over Ethernet (PoE) system originally defined in Clause 33 for deployment over balanced twisted-pair cabling."

Cl **145** *SC* **145.1.3** *P* **97** *L* **38** # i-394

Diminico, Christopher

Comment Type **TR** *Comment Status* **X** *Pres: Diminico*

For a constant power load and a worse case PSE the current per pair (ICable, A) is dependent on the loop resistance (equation 145-2). The current per pair/conductor is a parameter used to limit the number of 4-pair cables in a cable bundle. The 802.3bt nominal highest current per pair (ICable, A) derived by assuming the worse case DC loop restistance (RCh), associated with 100 meters of cabling, is being used to limit the number of 4-pair cables in a bundle for all cabling lengths (DCR). Assuming the worse case DCR (length) for all cabling topologies leads to overly pessimistic limits on the number of 4-pair cables in a cable bundle.

SuggestedRemedy

Develop informative Annex to characterize the current as a function of DCR (length) for constant power loads and worse case PSEs (equation 145-2). Presention of proposed Annex to be provided.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.1.3.1** *P* **98** *L* **28** # i-379

Thompson, Geoffrey Individual

Comment Type **ER** *Comment Status* **D** *Pres: Yseboodt9*

The placement of the cabling specifications in 145.1.3 System Parameters is wrong. Cabling is not a "system parameter". Placement there is organizationally confusing. Cabling is a full element of the the specified 3 element system. The cabling should have its own sub-clause at a peer level with 145.2 PSE and 145.3 PD.

SuggestedRemedy

Move the specification (whether it be by reference or local) for cabling to its own higher level clause, presumably cl. 145.4 which would bump the rest of the clause further out.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Move clause 145.1.3.1 (which now has what used to be 145.1.3.2 in it) to new clause 145.1.4 and increment all further clauses.

TFTD
WFP - Lennart to attempt to remove SHALLS after 145.1.1.

Cl **145** *SC* **145.2.4** *P* **107** *L* **40** # i-49

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Darshan12*

A PD's diode bridge is the dominant, and most unpredicatable, contributor to pair-to-pair current unbalance.
Diode specifications generally do not include information or guarantees about the maximum spread in forward voltage between samples.
This makes it hard to get to a provable correct design that will always meet the current unbalance spec.
It is however not impossible, analysis over the course of this project has shown that diode forward voltage differences of more than 60mV are extremely rare. This number has been used to calculate the unbalance budget for the PD.

What isn't taken into account is diode aging. As diodes are exposed to current and temperature, their forward voltage will begin to drift.
A pair of parallel diodes exposed to roughly the same current may be expected to age in the same way (this is uncertain, but let's accept it for the moment).

If 4-pair PSEs are allowed to provide power in polarity configurations that can result in ONE pairset having the other polarity between two PSEs,
this would mean that a PD that has been exposed to a certain current configuration, would find itself powered in a way that has one 'aged' diode conduct, and another 'new' diode in parallel. By 'new' I refer to a diode that has not seen any significant current over it's lifetime.

At the moment of writing this comment, it is unknown what the magnitude of this issue is. Test to determine this are planned.

SuggestedRemedy

1. Quantify this issue for the November meeting
2. Appropriate solition, if needed to be presented then

Proposed Response *Response Status* **W**

TFTD

TFTD YD
See darshan_12_0917.pdf

WFP

TFTD DS
The PD designer has multiple options to circumvent this issue: Request greater Class, utilize less of P_Class_PD, or take active control of PD contribution to system unbalance. The TF have specified unbalance numbers that compromise between substantial PD unbalance contributions and burden on other system objects to 'ballast' PD contributions. PD designers with marginal designs and high P_Class_PD utilization should be cautioned to consider unbalance effects (perhaps a note in PD unbalance section).

TFTD CJ

Proposed reject. The comment has served its purpose. We reject, he says unsatisfied, it remains in scope for November.
Incidentally, I did some measurements of 'used' diodes versus unused and found indistinguishable difference in Vf.

Cl **145** *SC* **145.2.5.4** *P* **111** *L* **36** # i-457

Darshan, Yair

Comment Type **E** *Comment Status* **D** *Pres: Yseboodt4*

In the variable description dll_4PID "dll_4PID A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power."
it doesn't say with what they were negotiate etc.

SuggestedRemedy

Change from "dll_4PID
A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power."
To: "dll_4PID
A variable that indicates whether the PSE and PD have negotiated 2-pair or 4-pair power capability via the Data Link Layer."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change to "dll_4PID: A variable indicating the state of the PD 4PID bit in the Power type/source/priority field, as defined in Table 79-4."

TFTD

Cl **145** *SC* **145.2.5.4** *P* **113** *L* **24** # i-269

Stewart, Heath — Analog Devices Inc.

Comment Type **T** *Comment Status* **X** *PSE SD*

option_class_probe can be utilized to both reduce dissapated heat during classification and increase classification flexibility.
See stewart_0917_01.

SuggestedRemedy

Adopt stewart_0917_01.

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD YD
See also darshan_04_0917.pdf

Cl **145** *SC* **145.2.5.7** *P* **125** *L* **1** # i-66

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt6*

The PSE state diagram currently requires a PSE to either turn on, or go back to IDLE within Tpon referenced at the end of detection.
Another option is to 'renew' Tpon by checking is the PD is drawing a correct mark current.
This flexibility has a number of use cases as explained in
http://www.ieee802.org/3/bt/public/may17/lukacs_01_0517_Mark&Hold_rev1.0.pdf

SuggestedRemedy

Adopt yseboodt_06_0917_markhold.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD LY
Also see lukacs 01 on reliability testing.

Cl **145** *SC* **145.2.5.7** *P* **128** *L* **46** # i-459

Darshan, Yair

Comment Type **T** *Comment Status* **X** *PSE SD*

In the exit from CLASS_EV3 MARK_EV3 "tcle3_timer_done * (pse_alternative = both) *(pd_class_sig ? 4) *((pse_avail_pwr ? pd_class_sig+5) +(pse_avail_pwr > 5))",
the "+" in pd_class_sig+5 is (according to page 109 line 22) "a Boolean OR" while in the intent here is to used as mathematical sum. There is a need to either update the '+' definition or add another symbol for mathematical summation.

SuggestedRemedy

1. add '++' symbol to table in page 109 and define this symbol as mathematical summation.
2. Change from "pd_class_sig+5)" to "pd_class_sig++5)"
3. Fix the same problem in P128, l46 in MARK_EV3 state.

Proposed Response *Response Status* **W**

TFTD LY
This is really a problem. The “+” operator is use for logical OR, and in these statements for addition as well.
Remedy:
– replace “pd req pwr = pd class sig+5” by “pd req pwr = sum(pd class sig, 5)” in MARK EV3
– replace “((pse avail pwr >= pd class sig+5) +” by “((pse avail pwr >= sum(pd class sig, 5)) +”
in the arc from CLASS EV3 to MARK EV3

TFTD DS
The term in question is trying to allow PSE w/ Class 5 power available, to negotiate w/ Class 5 PD.
This revision to transition logic does not make use of math operations:
CLASS_EV3 -> MARK_EV3
tcle3_timer_done * (pse_alternative = both) * (pd_class_sig != 4) * (pse_avail_pwr > 4) * ((pd_class_sig = 0) + (pse_avail_pwr > 5))
CLASS_EV3 -> MARK_EV_LAST
tcle3_timer_done * ((pse_alternative != both) + (pd_class_sig = 4) + (pse_avail_pwr <= 4) + ((pd_class_sig != 0) * (pse_avail_pwr <= 5)))

Review DS's logic!!!!!

Cl **145** *SC* **145.2.5.7** *P* **128** *L* **46** # i-458

Darshan, Yair

Comment Type **T** *Comment Status* **X** *PSE SD*

In the exit from CLASS_EV3 MARK_EV3 "tcle3_timer_done * (pse_alternative = both) *(pd_class_sig ? 4) *((pse_avail_pwr ? pd_class_sig+5) +(pse_avail_pwr > 5))", missing parenthesis in pd_class_sig+5.

SuggestedRemedy

Change from: " "tcle3_timer_done * (pse_alternative = both) *(pd_class_sig ? 4) *((pse_avail_pwr ? pd_class_sig+5) +(pse_avail_pwr > 5))""
To: "tcle3_timer_done * (pse_alternative = both) *(pd_class_sig ? 4) *((pse_avail_pwr ? (pd_class_sig+5)) +(pse_avail_pwr > 5))"

Proposed Response *Response Status* **W**

TFTD

Wait for outcome of 459

Cl **145** *SC* **145.2.5.7** *P* **131** *L* **39** # i-404

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt7*

In the Exit from IDLE_ACS to WAIT_ACS we have the following conditions:
pd_autoclass * !tpon_timer_done *tinrush_timer_pri_done * pwr_app_pri *(!alt_pwrd_sec + (tinrush_timer_sec_done * pwr_app_sec))
It looks that we have two issues here:
1) redundancy in the term " tinrush_timer_pri_done * pwr_app_pri. If pwr_app_pri is true, it means that tinrush_timer_pri_done is TRUE as well.
2) the term (!alt_pwrd_sec + (tinrush_timer_sec_done * pwr_app_sec)) is always TRUE.
- alt_pwrd_sec in false meaning that "The PSE is not to apply power to the Primary Alternative. "
- tirnush_timer_sec_done *pwr_app_pri indicates that we POWER up secondary pair and inrush is done in the secondary.
So, we have a condition that if we power up/or not power up.
It's like doing (X or not X) that is always true, which requires to remove this term completely...
In order to find what we really need here, let's expand the whole original term. It is equivalent to the following two parts:
a) pd_autoclass * !tpon_timer_done *tinrush_timer_pri_done * pwr_app_pri*!alt_pwrd_sec +
b) pd_autoclass * !tpon_timer_done *tinrush_timer_pri_done * pwr_app_pri *tinrush_timer_sec_done * pwr_app_sec
I believe that our intent is to allow Autoclass for Type 3 and 4 PSEs supporting single-signature PDs over 4-pairs or Type 3 PSE supporting SS-PD over 2-pairs.
There are few issues:
In part (a), redundancy in the term " tinrush_timer_pri_done * pwr_app_pri ".
If pwr_app_pri is true, it means that tinrush_timer_pri_done is TRUE as well.
As a result, it is sufficient to reduce this term from " tinrush_timer_pri_done * pwr_app_pri " to "pwr_app_pri", resulting with term (a):
"pd_autoclass * !tpon_timer_done * pwr_app_pri*!alt_pwrd_sec"
In part (b), the same concept as in part (a) applies to tinrush_timer_sec_done * pwr_app_sec i.e. If pwr_app_sec is true, it means that tinrush_timer_sec_done is TRUE as well.
As a result, we can reduce term (b) to:
"pd_autoclass * !tpon_timer_done * pwr_app_pri * pwr_app_sec"
The net result is:
pd_autoclass * !tpon_timer_done * pwr_app_pri*!alt_pwrd_sec + pd_autoclass * !tpon_timer_done * pwr_app_pri * pwr_app_sec =
pd_autoclass * !tpon_timer_done * pwr_app_pri*(!alt_pwrd_sec + pwr_app_sec)

SuggestedRemedy

Change from:
"pd_autoclass * !tpon_timer_done *tinrush_timer_pri_done * pwr_app_pri *(!alt_pwrd_sec + (tinrush_timer_sec_done * pwr_app_sec))"
To:
"pd_autoclass * !tpon_timer_done * pwr_app_pri*(!alt_pwrd_sec + pwr_app_sec)"

Proposed Response *Response Status* **W**

TFTD

Can someone confirm this logic?

TFTD LY
It is not fully equivalent and introduces a difference in timing. Probably OBE by yseboodt 07

WFP

TFTD DS
Reject.
Addressing the commentor's points:
1) This is a straight copy-paste of transition logic from POWER_UP to POWER_ON, as intended. The timer check should remain in both locations, as pwr_app_x does not evaluate inrush timer.
2) Disagree. If the PSE is applying power on alt_sec and inrush is not completed on alt_sec, this argument is false. I assume you ultimately came to agree on this point, as the suggested remedy maintains the logic "!alt_pwrd_sec + pwr_app_sec".

Cl **145** *SC* **145.2.5.7** *P* **132** *L* **4** # i-195

Peker, Arkadiy Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Stewart1*

Missing error_condition_pri at the input to the state IDLE_PRI at the condition iclass_lim_det_pri.

SuggestedRemedy

1. Change from: "iclass_lim_det_pri" to "iclass_lim_det_pri + error_condition_pri"
2. Add new variable to 145.2.5.4:
"error_condition_pri
A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145-16 and that require the PSE not to source power over the Primary Alternative.
Values:
FALSE: No fault indication.
TRUE: A fault indication exists.

Proposed Response *Response Status* **W**

TFTD

Do we want to create pri and sec versions of error_condition?

WFP

Cl **145** *SC* **145.2.5.7** *P* **133** *L* **5** # i-198

Peker, Arkadiy Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan4*

Figure 145-15 doesn't have the option of using short class event when doing "class probe" functionality as we have in single-signature class probe case. This cost with more time to complete process and more power dissipation. The same applies to the secondary part in page 137. It is suggested to replicate CLASSIFICATION pre-state and CLASS_PROBE from page Figure 145-13 page 128 in primary and secondary state machines with the relevant modifications.

SuggestedRemedy

Adopt darshan_04_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.5.7** *P* **133** *L* **13** # i-229

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **D** *PSE SD*

"In the exit from CLASS_EV2_PRI to MARK_EV2_PRI, the variable option_2ev is missing in the condition:
tcle2_timer_pri_done *(pd_class_sig_pri = temp_var_pri) * (class_4PID_mult_events_pri +(pse_avail_pwr_pri > 4)).
It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:
"tcle2_timer_pri_done *(pd_class_sig_pri = temp_var_pri) * (class_4PID_mult_events_pri +(pse_avail_pwr_pri > 4))"
To:
"tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * (
(class_4PID_mult_events_pri * !option_2ev)+ (pse_avail_pwr_pri > 4)) "

Proposed Response *Response Status* **W**

TFTD

Do we want to use the same variable for SS and DS?

TFTD LY
This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD YD
"1. There is an error in the proposed remedy: It should be:""tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * ((class_4PID_mult_events_pri + !option_2ev + (pse_avail_pwr_pri > 4)) ""

2. And the answer for comment editor question ""Do we want to use the same varible for both SS and DS"" is YES since not need to seperate within a port the option for primary and secondary."

TFTD DS
Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

Yair to check DS's comment.

Cl **145** *SC* **145.2.5.8** *P* **133** *L* **18** # i-230

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *PSE SD*

"In the exit from CLASS_EV2_PRI to MARK_EV_LAST_PRI, the variable option_2ev is missing in the condition:
"tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * !class_4PID_mult_events_pri * pse_avail_pwr_pri = 4".
It needs to be the same concept as in the single-signature case."

SuggestedRemedy

"Change from:
"tcle2_timer_pri_done * (pd_class_sig_pri = temp_var_pri) * !class_4PID_mult_events_pri * pse_avail_pwr_pri = 4"
To:
"tcle2_timer_pri_done * option_2ev * (pd_class_sig_pri = temp_var_pri) * !class_4PID_mult_events_pri * pse_avail_pwr_pri = 4"

Proposed Response *Response Status* **W**

TFTD

Do we want to use same variable for SS and DS?

TFTD LY
This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD DS
Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events. We do not need an option_ev2 for dual-signature diagrams.

Yair to check DS's comment.

Cl **145** *SC* **145.2.5.7** *P* **136** *L* **4** # i-199

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Stewart1*

Missing error_condition_sec at the input to the state IDLE_SEC at the condition iclass_lim_det_sec.

SuggestedRemedy

"1. Change from: ""iclass_lim_det_sec"" to ""iclass_lim_det_sec + error_condition_sec""
2. Add new variable to 145.2.5.4:
""error_condition_sec
A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 145-16 and that require the PSE not to source power over the Secondary Alternative.
Values:
FALSE: No fault indication.
TRUE: A fault indication exists."

Proposed Response *Response Status* **W**

TFTD

Do we want pri and sec versions of error_condition?

WFP

Cl **145** *SC* **145.2.5.7** *P* **136** *L* **11** # i-254

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan13*

In the exit from IDLE_SEC to START_DETECT_SEC we have the following condition:
"(!pwr_app_sec * pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec)"
Based on the description in page 109 lines 37-38 for CC_DET_SEQ and specifically, CC_DET_SEQ=3 for dual-signature means: Connection check is followed by staggered detection
(The analysis and simulations results for other sequences 0, 1 and 2 are covered by other comments and most of them are OK).

The staggered detection range may occur with starting the secondary detection after doing the primary detection (option 1) up to doing the secondary detection only if the primary is on (option 2). This covers the full range of possibilities.
Option 1 is normally used when class_4PID_mult_events_sec=TRUE. This currently is not covered by the state machine.
Option 2 is normally used when class_4PID_mult_events_sec=FALSE and it is covered in the 1st part of the condition: (!pwr_app_sec * pwr_app_pri).
Option 3 is covers the case that the primary return to IDLE_PRI due to various reasons and the secondary didn't detect even once: ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec).

The current state diagram covers option 2 and 3, and does not cover option 1!

The state diagram should allow staggered detection before Primary power up, after primary power up, and during power up in case that class_4PID_mult_events_sec is set to FALSE.
The proposed changes in the state diagram will allow staggered detection after Primary finished its 1st detection without affecting the previous functionality and flow, by oring the additional missing possibility (option 1).
The proposed changes do not affect:
a) The behavior of other "CC_DET_SEQ NE 3" flows.
b) Previous state diagram possibilities.

In addition, the proposed changes also required to cover multiple cycles of detection+classification until host decides to power on the port (which is covered by darshan_04_0917.pdf).
The additional missing possibility is covered by adding the following part:
+ (class_4PID_mult_events_sec*(CC_DET_SEQ=3) * !det_once_sec * det_once_pri)
In order to implement the addition, we need to add the following variable for the primary side (similar variable is already exist for the secondary):

"det_once_pri
This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI.
Values:
FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.

TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram."

In the above proposed change, det_once_pri is used as a condition for starting detection in the secondary any time until power up, after primary was detected at least once.
det_once_pri is set to FALSE when sism = FALSE at ENTRY_PRI.
det_once_pri is set to TRUE when Primary state diagram reaches to "DETECT_EVAL_PRI", to clearly indicate that detection on primary has ended before tdet_timer_pri expired."

SuggestedRemedy

1. Change from:
"(!pwr_app_sec *pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec)""
To:
"(!pwr_app_sec *pwr_app_pri) + ((CC_DET_SEQ=3) * option_probe_alt_sec * !det_start_pri * !det_once_sec) +
(class_4PID_mult_events_sec*(CC_DET_SEQ=3) * !det_once_sec * det_once_pri)
2. Add the following variable to the variable list:
det_once_pri
This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI. Values:
FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.
TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram.
"

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.5.7** *P* **136** *L* **20** # i-251

Peker, Arkadiy Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan13*

In Figure 145-16, in the exit from ENTRY_SEC to START_DET_SEC, when selecting CC_DET_SEQ 0 or 1, and class_4PID_multi_event_sec = FALSE, the secondary state machine allows to move from ENTRY_SEC state to START_DETECT_SEC only if pwr_app_pri = TRUE per the existing condition:
sism * ((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)

If Primary fails to powerup, the Primary state machine returns back to IDLE_PRI. As a result, pwr_app_pri variable will remain in FALSE, and the secondary state machine won't be able to exit from ENTRY_SEC i.e. will be stuck there.
The easy way to handle this problem is to enable moving to START_DETECT_SEC from ENTRY_SEC, also if primary performed detection at least once and is now in IDLE_PRI state which prevents stuck at ENTRY_SEC. This solution requires the addition of new variable det_once_pri (the current draft has only det_once_sec) which is required also by other comments that all related to each other and can be see in darshan_04_0917.pdf. "

SuggestedRemedy

See darshan_04_0917.pdf for how the following change is also addresses other issues including the possibility to do cycles of detection + class_probe events on primary and secondary with the option to go to IDLE_PRI/SEC and WAIT_PRI/SEC.
---
1) Add the following variable:
det_once_pri
This variable indicates if the PSE has probed the Primary Alternative at least once, when entering to DETECT_EVAL_PRI. Values:
FALSE: The PSE has not probed on the Primary Alternative since entering the Primary Alternative state diagram.
TRUE: The PSE has probed the Primary Alternative at least once since entering the Primary Alternative state diagram.
2) Change from:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
To:
sism * ((!class_4PID_mult_events_sec * (pwr_app_pri + det_once_pri * !det_start_pri)) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)."

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.5.7** *P* **136** *L* **20** # i-250

Peker, Arkadiy — Microsemi Corporation

Comment Type **ER** *Comment Status* **X** *Pres: Darshan4*

There is redundant parenthesis in the exit from ENTRY_SEC to START_DETECT_SEC:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
in the part: (!class_4PID_mult_events_sec * pwr_app_pri). "

SuggestedRemedy

Change from:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
To:
"sism *(!class_4PID_mult_events_sec * pwr_app_pri + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"

See darshan_04_0917.pdf for additional changes proposed to this condition due to other comments."

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD LY
By removing these parens we both reduce clarity, and we now depend on operator precendence and-before-or. Something we said we would avoid.

TFTD YD
"This is no longer in darshan_04 and the prposed remedy is complete without the need for presentation.Deletete the text ""See darshan_04_0917.pdf for additional changes proposed to this condition due to othercomments."""

Cl **145** *SC* **145.2.5.7** *P* **136** *L* **21** # i-252

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan13*

In the transition between ENTRY_SEC to START_DET_SEC we have the following condition:
"sism * ((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
In this condition, when class_4PID_mult_events_sec=FALSE, and CC_DET_SEQ=0 OR 1, If START_DET_PRI exit to IDLE_PRI due to tdet_timer_pri_done, the pwr_app_pri will remain in FALSE which won't allow exiting from ENTRY_SEC to START_DETECT_SEC and the secondary state machine remain stuck in ENTRY_SEC.

The proposed solution for this problem is:
1) To add stop_tdet_timer_pri in the DETECT_EVAL_PRI state. This action ensures that tdet_timer_pri_done will remain FALSE when moving from START_DETECT_PRI to DETECT_EVAL_PRI. This modification is required since even if we did detection before tdet_timer_pri is expired, we will get tdet_timer_pri_done anyway. This action will enables the usage of tdet_timer_pri_done in the secondary state machine at the exit from ENTRY_SEC to START_DETECT_SEC when we will add this variable in (2).
2. To add ""tdet_timer_pri_done to the condition of the exit from ENTRY_SEC to START_DETECT_SEC as follows:
""sism *((!class_4PID_mult_events_sec * (pwr_app_pri + tdet_timer_pri_done)) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"" . This change will allow to move to START_DETECT_SEC in case that we move from START_DETECT_PRI to IDLE_PRI due to tdet_timer_pri expiration."

SuggestedRemedy

1. Add "stop_tdet_timer_pri"" to the DETECT_EVAL_PRI state.
2. Add "tdet_timer_pri_done to the condition of the exit from ENTRY_SEC to START_DETECT_SEC by performing the following change:
Change from:
"sism *((!class_4PID_mult_events_sec * pwr_app_pri) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"
To:
"sism *((!class_4PID_mult_events_sec * (pwr_app_pri + tdet_timer_pri_done)) + class_4PID_mult_events_sec) * (CC_DET_SEQ=0 + CC_DET_SEQ=1)"

Due to the fact that item 2 need additional changes due to other comments, and in order to meet the requirement that we need single independent comment for each issue which I did here but may cause editor confusion of how to apply the remedies of other comments, See darshan_04_0917.pdf for how the above change is combined with other changes i.e. the possibility to do cycles of detection + class_probe events on primary and secondary with the option to go to IDLE_PRI/SEC and WAIT_PRI/SEC."

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.5.8** *P* **137** *L* **13** # i-231

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *PSE SD*

"In the exit from CLASS_EV2_SEC to MARK_EV2_SEC, the variable option_2ev is missing in the condition:
""tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * (class_4PID_mult_events_sec +(pse_avail_pwr_sec > 4))"".
It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:"tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * (class_4PID_mult_events_sec +(pse_avail_pwr_sec > 4))"
To: "tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * ((class_4PID_mult_events_sec * !option_2ev) + (pse_avail_pwr_sec > 4))"

Proposed Response *Response Status* **W**

TFTD

Do we want to use the same varible for both SS and DS?

TFTD LY
This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD YD
"1. There is an error in the proposed remedy: It should be:""tcle2_timer_sec_done *(pd_class_sig_sec = temp_var_sec) * ((class_4PID_mult_events_sec + !option_2ev + (pse_avail_pwr_sec > 4))"".2. And the answer for comment editor question ""Do we want to use the same varible for both SS and DS"" is YES since not need to seperate within a port the option for primary and secondary."

TFTD DS
Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events.
We do not need an option_ev2 for dual-signature diagrams.

Yair to review DS's suggestion.

Cl **145** *SC* **145.2.5.8** *P* **137** *L* **18** # i-232

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *PSE SD*

In the exit from CLASS_EV2_SEC to MARK_EV_LAST_SEC, the variable option_2ev is missing in the condition:
"tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4".
It needs to be the same concept as in the single-signature case."

SuggestedRemedy

Change from:
"tcle2_timer_sec_done * (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"
To:
"tcle2_timer_sec_done * option_2ev* (pd_class_sig_sec = temp_var_sec) * !class_4PID_mult_events_sec * pse_avail_pwr_sec = 4"

Proposed Response *Response Status* **W**

TFTD

Do we want to use the same varible for both SS and DS?

TFTD LY
This logic is wrong. To make sure we adopt the corrected version (Yair has it).

TFTD DS
Setting class_4PID_mult_events_x FALSE already enables PSE to limit to 2 class events.
We do not need an option_ev2 for dual-signature diagrams.

Yair to review DS's suggestion.

Cl **145** *SC* **145.2.6** *P* **141** *L* **20** # i-73

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *PSE Detection*

"In any operational state, the PSE shall not apply operating power to a pairset until the PSE has successfully detected a valid signature over that pairset."

A PSE does not apply power, it applies voltage and the PD draws current, causing power to be sourced.
The term 'operating power' is not defined either.
"In any operation state" are 4 redundant words.

SuggestedRemedy

"The PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
Change to: "The PSE shall not apply operating voltage to a pairset until the PSE has

successfully detected a valid signature over that pairset, with the exception of operating in a test mode."

TFTD DS
The state diagram and the other normative statements in the PSE detection section make this a redundant requirement. Repairing this statement would require a lot of nuance (considerations for TEST_MODE states, "greater than v_valid" vs "operating voltage"). Delete redundant requirement.

"In any operational state, the PSE shall not apply operating voltage to a pairset until the PSE has successfully detected a valid signature over that pairset."

Heath to propose removal of test modes.

Cl **145** *SC* **145** *P* **142** *L* **10** # i-1

Anslow, Peter — Ciena Corporation

Comment Type **TR** *Comment Status* **D** *Editorial*

The IEEE-SA Standards Style Manual 13.3.2 says "An em dash (--) should be used to indicate the lack of data for a particular cell in a table."
Comment #29 against P802.3bt D2.4 was: "Several tables in Clause 145 have blank cells in the min or max columns, which should contain an em-dash", but this was rejected with the rebuttal:
"The lack of em-dashes is intentional. The em-dash would convey that there is no relevant information, while the lack of the em-dash conveys that there is no specific number."
This makes no sense.
The first example of this issue is in Table 145-7. "Connection check to detection time" Tcc2det has a maximum value of 0.4 s, but the min column is blank. According to the IEEE style manual the cell should contain an em dash, which would indicate that there is no minimum requirement for this time. If there is some requirement on the minimum (not just a number) then an indication of this should be made via an entry in the cell such as "See 145.x.x". If this is not the case, then the cell should contain an em dash.

SuggestedRemedy

Make sure all tables have an entry of em-dash or pointer to the requirement in currently blank min or max columns.
In particular, Tables 145-7, 145-8, 145-9, 145-10, 145-14, 145-16, 145-20, 145-27, 145-28, 145-30, 145-31, 145-32.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

TFTD (talk to Katherine)

There is a distinction between an em-dash, which indicates 'a lack of data', and leaving a cell blank. Eg. For parameters that convey a range, having a blank 'Min' cell, does NOT indicate there is lack of data, rather that the minimum value is open-ended. An em-dash would convey an incorrect message. Em-dashes
have been put in all cells where it is appropriate. This seems consistent with other Clauses, I found many tables with empty cells: Table 78–4, 80–2, 80–3, 80–4, 82–1, 85–1, 85–5, 85–7, 86–2, 86–6, 86–7, 88–9, 89–6, 91–1, 92–8, 94–16, 94–17, 95–6, 95–7.

Cl **145** *SC* **145.2.7** *P* **146** *L* **41** # i-79

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *PSE Power*

Topic: SLIDING
"Measurements should be averaged using any sliding window with a width of 1 s."

This sentence follows after the definition of PClass and PClass-2P. That whole section is informative in nature.
- Why is this a should ?
- Measurements of what ? PClass is a capability.
- The actual power requirement of a PSE is encoded in ICon-2P.

SuggestedRemedy

Remove quoted sentence.

Proposed Response *Response Status* **W**

TFTD

I believe this is the only mention of the window for Pclass. Is it ok to remove it?

Lennart's homework…

Cl **145** *SC* **145.2.8** *P* **152** *L* **46** # i-419

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan3*

Icon-2P_unb in Table 145-16 item 5 needs some updates to sync with latest changes and to fit the test verification models accuracy.

SuggestedRemedy

Adopt the changes proposed in darshan_03_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8** *P* **152** *L* **46** # i-463

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan12*

The following question has been asked regarding diode aging and its affect on PD_Vdiff that affect unbalance.
Background:
Our spec defines unbalance requirements for the PSE in terms of VPort_PSE-2P, Icon-2P_unb and for the PD in terms of Icon-2P_unb and inexplicit design requirement to keep PD_Vdiff=60mV max measured at 1-10mA range. The PD_Vdiff has the highest effect on the system current/resistance unbalance.
The following use case has been investigated:
A PD is connected to a PSE over 4-pairs. The PSE is using Alt A (MDI) and Alt B (X) resulting with 1,2 and 7,8 are positive and 3,6 and 4,5 are negative. It runs this way for MANY years. The PD front end is not an active bridge, it is a diode bridge. The PSE has been replaced and it uses Alt A (MDI) and Alt B (S). Now, 1,2 and 4,5 are positive and 3,6 and 7,8 are negative. Now we have diodes that have been aged (1,2 and 3,6) in parallel with diodes that have never have current through them (the ones in 4,5 and 7,8). This is not simply switching from the old diodes to the new ones, its mixing old with new. The questions are:
1. If the aging has an effect on Vf, then we may have higher mismatch between the diodes in parallel leading to higher unbalance.
2. In an extreme case, we may have a runaway situation as the aged diode drops more power and heats more than the 'new' diode.
Answers:
1. All diodes in the diode bridge has to have 60mV maximum Vdiff between any permutations of each two diodes.
2. Silicon doesn't have a memory. The performance characteristics change may changed after diode end of life time period due to mechanical construction and other issues that are function of current conduction.
3. Diodes that are at their end of life will introduce higher leakage current, higher VF, and other parameters will exceed the spec.
4. As long as the diode is kept with their allowed operating conditions, VF will not change significantly during the diode defined life time with or without current conduction.
5. Life time of a diode of reliable vendor can be 20 years. The lowest life time value of reliable vendors is 10 years. The typical is somewhere between these ranges.
6. As a result of the above, any component in the PD or PSE need to be selected with life time which exceed the product life time like any other designs.
7. If vendor follow the above rules, the effect of aging should not be a problem for VF (or other parameter).

SuggestedRemedy

See darshan_12_0917.pdf for details

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8** *P* **153** *L* **16** # i-92

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *PSE Inrush*

Table 145-16, Iinrush (item 6) lists minimum values for dual-signature PDs. Dual-signature PDs may be started up in a staggered fashion, making this parameter meaningless. In general, dual-sig PDs are specified exclusively on a per pairset basis only, this needs to be the same here.

SuggestedRemedy

- Remove the two rows for dual-signature PDs in Item 6 of Table 145-16
- Remove the two rows for dual-signature PDs in Item 4 of Table 145-28

Proposed Response *Response Status* **W**

Remove minimum values in Item 6 of Table 145-16.

TFTD

Inrush group to discuss

Cl **145** *SC* **145.2.8** *P* **153** *L* **16** # i-291

Stover, David — Analog Devices Inc.

Comment Type **TR** *Comment Status* **X** *PSE Inrush*

The PSE inrush requirements "I_Inrush" and "I_Inrush-2P" always apply. However, dual-signature PDs may be powered over one or both pairs. For this reason, specifying total output current (I_Inrush) for dual-signature PDs is problematic. For example: When a single pairset of a Type 4/Class 5 dual-signature PD is inrushed, the PSE shall provide an I_Inrush of at least 0.65A and shall not provide an I_Inrush-2P of more than 0.6A.
For dual-signature PDs, output current during inrush should only be specified per-pairset.

SuggestedRemedy

Remove I_Inrush entries for dual-signature PDs.

Proposed Response *Response Status* **W**

TFTD

OBE by 92

TFTD YD
"-The remedy doesn't make sense with the comment..which rows to remove? We can't remove any row..-You may want to remove only the minimum value of the total current for dual-sig row in item 6."

TFTD DS
Comment i-92 presents a superior remedy.

Cl **145** *SC* **145.2.8** *P* **153** *L* **16** # i-290

Stover, David — Analog Devices Inc.

Comment Type **T** *Comment Status* **X** *PSE Inrush*

Item 6 specifies "Total output current...in the POWER_UP state per the assigned Class", but includes rows for "Type 3" and "Type 4" dual-signature PDs.

SuggestedRemedy

Change from "Type 3 dual-signature PD" to "Dual-signature PD, Class 1 to 4"; Change from "Type 4 dual-signature PD" to "Dual-signature PD, Class 5".

Proposed Response *Response Status* **W**

TFTD

Wait for outocme of 92

Cl **145** *SC* **145.2.8** *P* **153** *L* **31** # i-485

Johnson, Peter

Comment Type **T** *Comment Status* **X** *PSE Inrush*

Dual Signature Class 5 Minimum I_Inrush-2P is specified as 325 mA. Class 5 Dual Signature PD's are specified in 145.3.8.3 as allowing up to 180uF for C_Port-2P without PD current limiting. Is there a rationale why 325mA current limiting meets the needs of a Class 5 Dual Signature but we require 400mA for all other cases where C_Port or C_Port-2P can go up to 180uF ?

SuggestedRemedy

Unless there is a justifiable reason, I_Inrush should be 800mA and I_Inrush-2P 400mA for the Type-4 Dual Signature case.

Proposed Response *Response Status* **W**

TFTD

That is a very good question Pete.

TFTD YD
"1. The rational was to allow foldback current limit that will start with 325mA.

2. To acount for unbalance at the pair with the minimum current i.e. to ensure the the minimum current will be 325mA minimum after unbalance effect. This was proven by calculations made by me Yair and David Stover. I agree that it is better to set it to 0.4A as the rest."

Cl **145** *SC* **145.2.8** *P* **153** *L* **33** # i-205

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan13*

"Table 145-16, item 8, Tinrush: It is clear from the state machine that Tpon includes Tinrush. It means that effective Tpon is (400-50) msec=350ms or (400-75) ms=325mse which needs to cover long 1st class events, + 4 class events + design margin. group to discuss if it sufficient for their designs and applications in both single and dual-signatures. To consider if Tpon need to be increased by approximately 50mse to compensate for the increase in the 1st long class events to keep our margins as in 802.3af/at. It doesn't affect reliability etc. since we had so far 200msec margin from the 600msec value from the 802.3af experiments and the actual spec numbers."

SuggestedRemedy

Increase Tpon from 400msec to 450msec or to what ever the group decides.

Proposed Response *Response Status* **W**

TFTD

wait for outcome of staggered presentation…

Adding up the class events you get:
95ms + 4*12ms + 5*9ms
(1st finger, 4 short class events, 5 mark events)

= 188ms

There seems to be plenty of margin.

TFTD YD
Response to David's calculations: If we want to power on at the same time it is marginal with typical numbers. If we power_on in staggered manar, then there is no issue.

TFTD CJ
I think worst case numbers are 105+4*20+5*12 = 255.

Response DNA: The PSE can choose not use worst case numbers…

Cl **145** *SC* **145.2.8.3** *P* **156** *L* **8** # i-337

Lemahieu, Joris — ON Semiconductor

Comment Type **TR** *Comment Status* **X** *PSE Power*

Input Voltage drop to 0V is excessive.

Drop to 0V during 30us spec seems to be written for (theoretical) diode bridge at PD input. Have diode reverse recovery and cable inductance effects (peak reverse recovery current) been taken into account here?

Active bridges seem very popular in 802.3bt PD solutions to reduce dissipation in the input rectifier stage.
An immediate short at the input would significantly discharge Cport as it takes time to turn off the mosfet.

SuggestedRemedy

Increase minimum voltage level during first 30us and make spec compliant with active bridges at the PD input.

Proposed Response *Response Status* **W**

TFTD

See 248

Cl **145** *SC* **145.2.8.3** *P* **156** *L* **8** # i-248

Picard, Jean — Texas Instruments Inc

Comment Type **TR** *Comment Status* **X** *PSE Power*

The following sentence does not make sense. In reality the PSE cannot really short the PI voltage, all it can do is temporarily turn off its port (it's only a low side switch after all, with a 0.1uF cap).

"The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145-28, allows a PD to operate for input voltage transients which cause VPD to drop as low as 0 V, lasting less than 30 us as specified in 145.3.8.6."

SuggestedRemedy

Use similar wording to the "at" standard, removing "which cause VPD to drop as low as 0 V".
The wording becomes this:
"The minimum PD input capacitance CPort min or CPort-2P min defined in Table 145-28, allows a PD to operate for input voltage transients lasting less than 30 us as specified in 145.3.8.6"

Proposed Response *Response Status* **W**

TFTD

Delete sentence. Put something in PD section…

include limit for PSE transients less than 30us.

TFTD YD
This is at the PD PI not at the PSE PI. At the PD the voltage can get to 0 or negative due to voltage changes in the PSE. You have LCR circuit on the way from PSE to PD. This was meant to protect ideal diode bridges.

Cl **145** *SC* **145.2.8.5** *P* **156** *L* **51** # i-204

Peker, Arkadiy — Microsemi Corporation

Comment Type **TR** *Comment Status* **X** *Pres: Darshan9*

"Equation 145-8 contains the parts that allow us to calculate the value of Icon-2P in case of operating over 2-pairs and for the dual-signature case.
However, for the most important use case which is operating over 4-pairs.
Equation 145-8 contains the part ""Icon-2P=min(Icon - IPort-2P-other, ICon-2P-unb) when operating over 4-pairs.
-Icon is defined in Equation 145-9.
-Icon-2P_unb is defined in Table 145-16 item 5.
There is no information to find the value of Icon-2P_other in order to calculate the value of Icon-2P. As a result, the spec is broken."

SuggestedRemedy

Adopt darshan_09_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.5** *P* **157** *L* **13** # i-101

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt3*

"A minimum current of I Con-2P-unb over one of the pairs of the same polarity under maximum unbalance condition (see 145.2.8.5.1) in the POWER_ON state."

The unbalance specification is tied together by ICon-2P-unb which serves 3 distinct roles:
- It is the minimum current a PSE must be able to supply on a pairset
- It is the maximum current a PSE may source when connected to a worst-case unbalance cable + PD
- It is the maximum current a PD may draw when connected to a worst-case unbalance cable + PSE

That makes it that there is ZERO margin between PSE minimum and PD maximum.

SuggestedRemedy

Adopt yseboodt_03_0917_unbalancemargin.pdf which aims to create margin by introducing a new parameter that takes the role of specifying the minimum current a PSE must support on a pairset.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.5** *P* **158** *L* **10** # i-104

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *Pres: Darshan15*

"I Peak-2P-unb , defined in Equation (145-12), is the minimum current due to unbalance effects that a PSE supports on a pairset when powering a single-signature PD over 4 pairs."

What follows is a set of equations that define the value of IPeak-2P-unb as function of IPeak (which in turns depends on VPSE and RChan) and RChan-2P.

See: http://www.ieee802.org/3/bt/public/mar17/yseboodt_02_0317_ipeak2punb.pdf
The value of IPeak-2P-unb is often lower than that of ICon-2P-unb. The PSE needs to support ICon-2P-unb, so this has the effect of 'clipping' IPeak-2P-unb to be at least ICon-2P-unb.

The real issue arises in the PD section, where we require a PD never to draw more than IPeak-2P-unb on any given pair.
If that is a requirement (and it should be), then we can't have IPeak-2P-unb depend on VPSE and RChan, both parameters the PD knows nothing about.

Given that there is almost no gain for PSEs to be had from being able to tune IPeak-2P-unb, the most effective solution is to make IPeak-2P-unb a fixed number.

SuggestedRemedy

- Replace page 158, lines 12 through 44 by:

IPeak-2P-unb = {ILIM-2P - 0.002

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Lennart, did this comment get imported correctly?

TFTD LY
I forgot I'm not allowed to use "fg" in my comment text. The last line should be:
IPeak-2P-unb = {ILIM-2P - 0.002}A

TFTD YD
See darshan_15_0917.pdf.

WFP

TFTD CJ
I will only agree to this comment if we get agreement that the way to test this parameter is to place a worst case PD unbalance circuit and not some current sink that checks for the actual current. The PD has to adhere to limits based on connection to a worst case PSE circuit, the PSE should be treated the same. It's great to have the numbers in the spec and those that don't deeply understand will design to those limits. But those that understand the way a system really works should be able to exploit that to their benefit and not fail only when tested by some non-PD circuit.

Cl **145** *SC* **145.2.8.5.1** *P* **158** *L* **45** # i-424

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan3*

Icon-2P_unb values need to be verified when using Equation 145-15 (Rpse_min/max) and Equation 145-26 (Rpd_min/max) with the test verification models described in Table 145-17 and Rsource_min/max requirements with their defined accuracies (+1/-%).

SuggestedRemedy

Adopt darshan_03_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.5.1** *P* **158** *L* **46** # i-425

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Pres: Darshan1*

The changes we did when we move from "channel" to "Link section" breaks some of the work we did for pair to pair resistance unbalance. To fix it, we need to add a text that defines the equipment connector as part of the PSE PI and PD PI when tested for pair-to-pair resistance unbalance for compliance. In this way we don't break the link section definition due to the fact that the PSE load when PSE is tested for compliance and PD voltage source output resistance, Rsource, when PD is tested for compliance include the effect of the equivalent portion of the link section.

SuggestedRemedy

Adopt darshan_01_0917.pdf for detailed analysis and proposed baseline.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.5.1** *P* **158** *L* **47** # i-392

Thompson, Geoffrey Individual

Comment Type **ER** *Comment Status* **X** *Pres: Yseboodt2*

This seems like an attempt to control the system imbalance (which is controlled by the combined specifications of the three elements, one of which is externally specified) from within the PSE spec.

SuggestedRemedy

This is all valuable tutorial material that would be valuable for further work on the topic so it should be moved (with suitable editing) to an informative annex.

Proposed Response *Response Status* **W**

TFTD

TFTD YD
"Reject this comment due to the following:1. No clear remedy what do.

2. No clear instructions what should stay and what should move to annex3. We already been in Spec, Move to Annex, Back to spec several times with many comments until it was clear that what we have now is important to have in the standard and not in the annex."

LDR GT

Cl **145** *SC* **145.2.8.5.1** *P* **159** *L* **27** # i-426

Darshan, Yair

Comment Type **T** *Comment Status* **D** *Pres: Darshan2*

This comment is not about active current balancing. This comment is about the typical use of PSE resistive elements to form Rpse_min and Rpse_max that meet equation 145-15 and when PSE connected to the PSE load specified in Table 145-17, will meet the values Icon-2P_unb in Table 145-16.
In D3.0, the maximum value of Rpse_min is not limited. Rpse_max is function of Rpse_min. If Rpse_min maximum value is not limited, it will cause the following issues:
(a) The internal PSE power supply open load voltage to significantly increase in order to keep the PSE voltage at the PI 50V min or 52V min pending the PSE Type under load. This will result with working outside the PSE operating voltage range.
(b) power loss at extreme values of Rpse_min which doesn't make sense.
(c) Per Equation 145-15, if Rpse_min is increased, Rpse_max is increased and at higher values of Rpse_min (starting at 0.5 ohms at Class 7-8 and 1 ohm at class 5-6), the contribution of Rpse to unbalance compared to the channel and PD, resulting with the increase of system unbalance at long cable which violates Icon-2P_unb when tested with test verification model in Table 145-17.
(d) there is no practical benefit to increase Rpse_min to any value.
(e) The above is not relevant to active current balancing.
See calculation results in darshan_02_0917.pdf.

SuggestedRemedy

(See calculation results in darshan_02_0917.pdf.)
Change from: "RPSE_min is the lower PSE common mode effective resistance in the powered pairs of the
same polarity."
To: "RPSE_min is the lower PSE common mode effective resistance in the powered pairs of the same polarity. The value of Rpse_min shall be limited to:
a) 1 ohms for class 5 and 6
b) 0.5 ohm for class 7 and 8.
The value of Rpse_min is not limited when active current balancing is used.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

TFTD

WFP

There is no reason to specify this. Reasons a, b, d, and e listed in the comment are not reasons to specify something, they are reasons for people not to make a product with high values of RPSE_min. Reason C (and A) points out that if they try to use a value that is too high, they will fail other specs.

TFTD LY
Fully agree this cannot be a 'shall', but we do have to specify over what range the RPSE equation produces valid results.

TFTD YD
"The main reason that we need to do it is that Equation 145-15 ACCURACY depends on the range of Rpse_min (the arguments used in the comment was the source of the inacuarcies). In other words: Typically, equation, any equation, has a range when it is valid. When the range is minus infity to plus infinity it means that it always correct. Since this equation done based on linear curve fitting, its range of existance is depened on limited value range of its subject parameter, Rpse_min, in this case. As a result, Rpse_min maximum value has to be limited.Change the proposed remedy to:After line 28, add the following text:""Equation 145-15 is valid for R_pse_min up to a value of 1 ohm for Class 5 and Class 6, and 0.5 ohm forClass7 and Class 8."""

Cl **145** *SC* **145.2.8.5.1** *P* **159** *L* **34** # i-427

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Unbalance*

In the text below:
"A PSE shall not source more than ICon-2P-unb min on any pair when connected to a **load** as shown in Figure 145-22, using values of Rload_min and Rload_max as specified in Equation (145-16) and Equation (145-17).", Need to be "PSE load" as in Figure 145-22.

SuggestedRemedy

Change text to "A PSE shall not source more than ICon-2P-unb min on any pair when connected to the PSE load as shown in Figure 145-22, using values of Rload_min and Rload_max as specified in Equation (145-16) and Equation (145-17)."

Proposed Response *Response Status* **W**

TFTD

See 107

TFTD YD
Should be OBE by 107 since "PSE load" is impllied in the "test fixture" that Lennart is using in his proposed remedy

---

Cl **145** *SC* **145.2.8.5.1** *P* **159** *L* **34** # i-107

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *Pres: Yseboodt2*

"A PSE shall not source more than I Con-2P-unb min on any pair when connected to a load as shown in Figure 145-22, using values of R load_min and R load_max as defined in Equation (145-16) and Equation (145-17)."

- ICon-2P-unb is a minimum, no need to specify I Con-2P-unb min
- We should make it obvious that this shall applies when connected to a given test fixture described in the next paragraphs.

SuggestedRemedy

Change quoted text to:
"A PSE shall not source more than I Con-2P-unb on any pair when connected to a test fixture described in Figure 145-22, using values of R load_min and R load_max as defined in Equation (145-16) and Equation (145-17)."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD

See 427

Cl **145** *SC* **145.2.8.5.1** *P* **160** *L* **1** # i-108

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Darshan3*

Table 145-17 contains the values needed to determine Rload, which is the load with which PSE unbalance is checked.
Calculations show that when plugging in these numbers, some of the Classes fail to meet ICon-2P-unb.
Eg, with an RPSE_min=0.3 ICon-2P-unb for Class 7 (low channel conditions) is not met:

Class 7, low channel conditions, iport=1.195 i=0.784/0.412/0.784/0.412, VSupply=52.370 VPSEPI=52.003
RPSE_min = 0.250 and RPSE_max = 0.446
PPD = 62.0, VLoad = 51.08, Vpd[1-4] = 52.11 52.14 0.26 0.23 = 51.92
FAILS to meet ICon-2P-unb of 0.781

Other values of RPSE cause more errors, but all in Class 7.

SuggestedRemedy

Either we need to update ICon-2P-unb, or we need to update the values in Table 145-17. Input Yair is needed.

Proposed Response *Response Status* **W**

TFTD

WFP

TFTD YD
The problem was resolved by accepting comment i-420. See full update for Icon-2P_unb for all classes in darshan_03_0917.pdf for comment 419. In fact, make 420 and 108, OBE to 419. It will save time.

Cl **145** *SC* **145.2.8.5.1** *P* **160** *L* **39** # i-422

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment is marked as LOWER02.
In the following text:
"ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P from 0.2 ? to 12.5 ? and worst-case unbalance contribution by a PD. PSEs that support channel common mode resistance less than 0.2 ?, or if RChan is less than 0.1 ?, the PSE should meet ICon-2P-unb requirements when connected to (Rload_min - 0.5 * RChan-2P) and (Rload_max - 0.5 * RChan-2P). This can be achieved by using a lower RPSE_max or higher RPSE_min than required by Equation (145-15). Lower RPSE _max values may be obtained by using smaller constant ? or higher RPSE_min in Equation (145-15) in the form of RPSE_max = ? * RPSE_min + ?."

The following may be improved:
1. The "total" is not required.
2. To simplify and clarify the text that explains what to do when shorter cabling than 0.2 ohm is used
3. To simplify the use of " RPSE_max = ? * RPSE_min + ?"

SuggestedRemedy

Replaced the called out text with:
"The values for ICon-2P-unb and the relationship between RPSE_max and RPSE_min (Equation (145-15)) are valid given that RChan-2P (see 145.1.3) ranges from 0.2 ? to 12.5 ? and that the PD meets 145.3.8.10. In cases where RChan-2P is less than 0.2 ?, or RChan is less than 0.1 ?, PSE compliance with ICon-2P-unb can be evaluated using Rload_min and Rload_max both reduced by 0.5 * RChan-2P. This compliance will require a reduction in the ratio of RPSE_max to RPSE_min presented by Equation (145-15). "

Proposed Response *Response Status* **W**

TFTD

DS wants this open pending outcome of yseboodt2

See 428, 109

TFTD YD
This text was discussed with Ken, Pete and Yair and agreed as better than the current text

TFTD DS
The reference text calls into question the accuracy of the PSE unbalance test as a de-facto guarantee that PSEs will provide interoperability, which must not be the case. Furthermore, the referenced text adds uncertainty for all PSE designers by suggesting a stricter set of PSE requirements might apply to them; in actuality, this refers to an application-specific case with extremely low resistance connections between PSE and PD.
Propose this paragraph be deleted or moved to Annex 145A.

Cl **145** *SC* **145.2.8.5.1** *P* **160** *L* **39** # i-428

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

This comment will be OBE by comment marked LOWER02 if LOWER02 will be accepted. In the text "ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P" the word "total" is not required. Remove it.

SuggestedRemedy

Change from "ICon-2P-unb and Equation (145-15) are specified for total channel common mode pair resistance RChan-2P" the word "total" is not required."
To: "ICon-2P-unb and Equation (145-15) are specified for channel common mode pair resistance RChan-2P" the word "total" is not required."

Proposed Response *Response Status* **W**

TFTD

See 422, 109

TFTD YD
Should be OBE to 422 if 422 will be accepted.

Cl **145** *SC* **145.2.8.5.1** *P* **160** *L* **45** # i-109

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt2*

"This can be achieved by using a lower R PSE_max or higher R PSE_min than required by Equation (145-15). Lower R PSE _max values may be obtained by using smaller constant a or higher R PSE_min in Equation (145-15) in the form of R PSE_max = a x R PSE_min + b."

Very long/complicated way to say that it can be achieved by decreasing the difference between Rpsemin and Rpsemax.

SuggestedRemedy

Change to:
"This can be achieved by decreasing the difference between R_PSE_min and R_PSE_max as defined in Equation 145-15."

Proposed Response *Response Status* **W**

TFTD

See 422, 428

TFTD YD
The proposed remedy cant be accepted as is. This is not just to decrease the difference it also touches the absolute values of Rpse_min/max. Instead, adopt 422 which is technically correct and clearer.

TFTD DS
The reference text calls into question the accuracy of the PSE unbalance test as a de-facto guarantee that PSEs will provide interoperability, which must not be the case. Furthermore, the referenced text adds uncertainty for all PSE designers by suggesting a stricter set of PSE requirements might apply to them; in actuality, this refers to an application-specific case with extremely low resistance connections between PSE and PD.
Propose this paragraph be deleted or moved to Annex 145A.

Cl **145** *SC* **145.2.8.5.1** *P* **161** *L* **1** # i-110

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt2*

Comparing Figure 145-22 with it's PD counterpart (Fig. 145-31), it contains a large amount of detail which is not relevant to the evaluation of Icon-2P-unb.

SuggestedRemedy

Adopt yseboodt_02_0917_Figure_145_22.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

See 393

Cl **145** *SC* **145.2.8.5.1** *P* **161** *L* **2** # i-393

Thompson, Geoffrey — Individual

Comment Type **ER** *Comment Status* **X** *Pres: Yseboodt2*

Figure 145-22. This figure is very valuable in understanding the overall problem of resistance imbalance in a PoE system, however it doesn't help with the problem of designing a PSE when one has no control of the link section or the PD.

SuggestedRemedy

Tutorial material that would be valuable for further work on the topic. It should be moved to an informative annex.

Proposed Response *Response Status* **W**

TFTD

See 110

TFTD YD
"Reject this comment due to the following:1. Figure 145-22 is needed for the spec. No clear remedy what to do instead.
2. No clear instructions what should stay and what should move to the informative annex
3. We already been in Spec, Move to Annex, Back to spec several times with many comments until it was clear that what we have now is important to have in the standard and not in the annex."

TFTD DS
The normative statement in this section is tied to Figure 145-22; equations 145-16, 145-17. These items should likely stay in the section.

LDR GT

Cl **145** *SC* **145.2.8.5.2** *P* **161** *L* **18** # i-434

Darshan, Yair

Comment Type **E** *Comment Status* **X** *Pres: Yseboodt2*

In the bottom of Figure 145-22, there is an arrow with a text "End-to-end pair-to-pair resistance".
This text need to be accurate and reflect the following:
a) It is End-to-end pair to pair effective resistance and not just resistance.
b) It is the boundaries of where the system unbalance is defined. This helps to understand the boundaries of the PSE PI to the PSE power supply elements that affect the unbalance and the same for the PD and the link segment.
c) The term End to End effective resistance unbalance is describe in 145.2.8.5.1 e.g. P.158 L48 and many other places in the spec.

SuggestedRemedy

Change from "End-to-end pair-to-pair resistance"
To: "End-to-end pair-to-pair effective resistance unbalance boundaries"

Proposed Response *Response Status* **W**

TFTD

These terms are becoming very confusing and need simplifing.

Cl **145** *SC* **145.2.8.5.1** *P* **161** *L* **20** # i-429

Darshan, Yair

Comment Type **E** *Comment Status* **X** *Pres: Yseboodt2*

The title of figure 145-22 is good but not sufficiently accurate. It is system effective resistance unbalance and not just system resistance unbalance. This is in sync with the title of the clause "145.2.8.5.1 PSE PI pair-to-pair effective resistance and current unbalance" and the text all over clause 145.2.8.5.1 and 145.3.8.10 (44 occurrences).

SuggestedRemedy

Change from Figure 145-22--PSE PI unbalance specification and system resistance unbalance"
To: "Figure 145-22--PSE PI unbalance specification and system effective resistance unbalance"

Proposed Response *Response Status* **W**

TFTD

TFTD LY
OBE to yseboodt 02 (do not adopt both, creates conflict)

WFP

Cl **145** *SC* **145.2.8.5.2** *P* **161** *L* **26** # i-431

Darshan, Yair

Comment Type **E** *Comment Status* **D** *Pres: Yseboodt2*

In the text "With the PSE powered on, adjust the load to PClass_PD.", missing "at the PD PI"

SuggestedRemedy

Change to: "With the PSE powered on, adjust the PSE load to PClass_PD at the PD PI."

Proposed Response *Response Status* **W**

TFTD

This instruction doesn't make sense. The PSE Load is the entire box in Figure 145-22. What are they supposed to adjust? I assume this really means to adjust the current draw in the small box that says "adjust" in it. We need to make this more clear.

See 431

WFP

TFTD YD
"1."" See 431""? This is 431.
2. I agree the remedy is not clear. Change the remedy to: ""Adjust to load such that a power of Pclass-PD is consumed at the PD PI."". See i-112."

Cl **145** *SC* **145.2.8.5.1** *P* **161** *L* **26** # i-112

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt2*

In the evaluation method for Figure 145-22, item b) says:
"With the PSE powered on, adjust the load to P Class_PD ."

Which is wrong since the PSE load also comprises of the R_Ch_unb resistors.

SuggestedRemedy

Replace by:
"Adjust to load such that a power of PClass-PD is consumed at the PD PI."

Note: text may need adjustment based on yseboodt_02_0917_Figure_145_22.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.5.1** *P* **161** *L* **28** # i-113

Yseboodt, Lennart Philips Lighting

Comment Type **T** *Comment Status* **D** *Pres: Yseboodt2*

In the evaluation method for Figure 145-22, step 'e' (check the current), comes after the Rload_min/max exchange.

SuggestedRemedy

Swap steps d) and e) and adjust labels accordingly.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
The remedy is incorrect. The order of d and e are correct

Cl **145** *SC* **145.2.8.6** *P* **161** *L* **45** # i-116

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **D** *PSE Inrush*

"The PSE shall limit I Inrush-2P and I Inrush during POWER_UP per the requirements of Table 145-16."

Nowhere in this subclause do we explain what these parameters are and how they relate to each other.

SuggestedRemedy

Insert the following text after the paragraph containing the quoted text:
"IInrush-2P is the current to which the PSE limits it's pairset output current while in POWER_UP. IInrush is the total current to which the PSE limits it's output current while in POWER_UP. When connected to a single-signature PD, IInrush is the total inrush current limit, and IInrush-2P serves as the limit for 2-pair inrush, or as the inrush unbalance limit during 4-pair inrush.
When connected to a dual-signature PD, only IInrush-2P is specified and serves as the inrush limit for each pairset independently."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD. Need to make sure DS lines get deleted for Iinrush for this text to be accurate.

TFTD YD
The text is correct without deleting the lines suggested by Lennart in other comment. I disagree with deleting DS lines in item 6 Table 145-16 since there is a raeson for it (limits the maximum current to 0.9A instead of 1.2A.)

Cl **145** *SC* **145.2.8.6** *P* **162** *L* **1** # i-301

Stover, David — Analog Devices Inc.

Comment Type **T** *Comment Status* **X** *PSE Inrush*

Figure 145-23 specifies the PSE inrush upperbound template; requirements for both Iport-2P and Iport as shown apply simultaneously. In Figure 145-23, Iport is limited to Iinrush,max while Iport-2P may load step up to 50A (>>Iinrush,max). As drawn, Iport-2p is limited to the lesser of these requirements: IInrush,max.

SuggestedRemedy

Remove IPort axis from Figure 145-23 or specify IPort behavior during load step.

Proposed Response *Response Status* **W**

TFTD

Delete Iport axis from figure.

Add sentence "

inrush group to discuss.

I don't follow your interpretation of the drawing.

TFTD DS
What is the upper bound of Iport during the 50A Iport-2P load step event? Figure 145-23 shows an 'exception' to the Iport-2P requirement without guidance on Iport requirements during this event.

Cl **145** *SC* **145.2.8.5.3** *P* **162** *L* **10** # i-433

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan10*

The shape of the load need to be circle and not rectangular since it is constant power sink. All our spec is based on the fact that the PD load is constant power sink

SuggestedRemedy

Adopt the changes proposed in darshan_10_0917.pdf marked in BLUE.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.2.8.8** *P* **164** *L* **32** # i-123

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **D** *Sliding*

Topic:SLIDING
Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.
Aim: get everything in the form "measure xxx using a xx time sliding window".

"The PSE shall limit a pairset current to I LIM-2P for a duration of up to T LIM-2P in order to account for PSE dV/dt transients at the pairset.
The cumulative duration of T LIM-2P may be measured with a sliding window."

Oh joy, a sliding window without any limitation on the width.

SuggestedRemedy

Replace the last quoted sentence by:
"The cumulative duration of T LIM-2P may be measured using sliding window of at least 1 second width."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Replace the last quoted sentence by:
"The cumulative duration of T LIM-2P may be measured using sliding window of at most 1 second width."

TFTD

homework…

Cl **145** *SC* **145.2.8.13** *P* **166** *L* **6** # i-130

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *Pres: Stewart1*

"PSEs, when connected to a single-signature PD, shall reach the POWER_ON state within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the POWER_ON state for a pairset within T pon after completing detection on the same pairset."
Statename should not be using word "state".

SuggestedRemedy

Change to:
"PSEs, when connected to a single-signature PD, shall reach POWER_ON within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach POWER_ON for a pairset within Tpon after completing detection on the same pairset."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Change to:
"PSEs, when connected to a single-signature PD, shall reach POWER_ON within Tpon after completing detection on the last pairset. When connected to a dual-signature PD, PSEs shall reach the respective power on state for a pairset within Tpon after completing detection on the same pairset."

TFTD HS

Second, this brings up another deficiency in this text. A invalid detect can take up to 499ms. This creates the opportunity for a new PD to be inserted. I'm still working on a fix for this. Tpon should only be restarted based on completion of a _valid_ detection on either pairset. Tpon should be stopped when either pairset is in a power on state. A new _detection_ or power on on either pairset should not be started if tpon has expired.

Cl **145** *SC* **145.3.2** *P* **168** *L* **31** # i-131

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt1*

This subclause deals with what kind of input power configurations a PD must be able to handle and operate under.
It does not properly cover all of the compliant configurations a PSE can have.

SuggestedRemedy

Adopt yseboodt_01_0917_pdinputpower.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.3.3.4** *P* **170** *L* **48** # i-136

Yseboodt, Lennart — Philips Lighting

Comment Type **T** *Comment Status* **D** *PD SD*

Variable pd_current_limit in the PD state diagram.
The description of TRUE/FALSE says "The PD is (not) required to control the input current."

What this is really about is _limiting_ the input current.

SuggestedRemedy

Replace 'control' in the text with the TRUE/FALSE values by 'limit'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD DS
Delete pd_current_limit. In all cases pd_current_limit is either redundant or misleading to pd_max_power usage:
In INRUSH:
pd_max_power <= inrush (no limit)
pd_current_limit <= false (no limit)
In POWER_DELAY:
pd_max_power <= min(3,pd_req_class)
pd_current_limit <= true (limit to I_Inrush_PD(-2P))
in POWERED:
pd_max_power <= min(pse_assigned_class, pd_req_class)
pd_current_limit <= false (no limit)

Cl **145** *SC* **145.3.3.7** *P* **174** *L* **23** # i-138

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt7*

The variable pd_acs_req indicates if a PD saw a long class event and must do Autoclass. This variable's description is very misleading in 145.3.3.4, moreover, we don't need it because we can use "long_class_event * pd_autoclass_enabled" to get the same effect.

I now also notice that Figure 145-27 doesn't work (eg. pd_acs_req is set to FALSE in IDLE_ACS, preventing it from being true in the arc from IDLE_ACS to WAIT_ACS).

SuggestedRemedy

Adopt yseboodt_07_0917_pdautoclassfix.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.3.5** *P* **183** *L* **22** # i-143

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Yseboodt8*

"A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B."

The requirement only holds for corrupting voltages above 10.1V, whereas connection check entirely operates below 10.1V.
See http://www.ieee802.org/3/bt/public/may17/yseboodt_09_0517_signature.pdf for problem description.

SuggestedRemedy

Change first paragraph of 145.3.5 to read:
"A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall not present a valid detection signature on that Mode when any voltage between 3.7 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B.
NOTE - A detection signature is only considered valid when it meets Table 145-20 over the entire PD detection voltage range of 2.7 V to 10.1 V."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.5** *P* **183** *L* **24** # i-436

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt8*

In the text "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode
when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on
that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements
apply to both Mode A and Mode B."

The part "and shall present an invalid detection signature on that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements apply to both Mode A and Mode B." doesn't guarantee (especially "between 10.1 V and 57 V") that for any voltage X in the range of 2.7V to 57V that is applied to the 1st pair and is higher by 1 V from the voltage applied to the 2nd pair that is being detected, will be result with invalid signature in the pair that is being detected.

SuggestedRemedy

Change from: "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode
when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on
that Mode when any voltage between 10.1 V and 57 V is applied to the other Mode. These requirements
apply to both Mode A and Mode B."

To: "A single-signature PD shall present a valid detection signature, as defined in Table 145-20, on a given Mode when no voltage or current is applied to the other Mode, and shall present an invalid detection signature on that Mode when any voltage between Vx and 57 V is applied to the other Mode when Vx is greater by at least 1V from the voltage applied to the other mode. These requirements apply to both Mode A and Mode B."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.6.1** *P* **186** *L* **32** # i-153

Yseboodt, Lennart — Philips Lighting

Comment Type **TR** *Comment Status* **X** *PD Reset*

In Table 145-26, Item 6, we find V_Reset_PD which is a range between 0V and 2.81V.
The additional information points to 145.3.8.1, which says nothing about this parameter.

VReset_PD isn't mentioned abywhere in the document, with the exception that it is used in the state diagram.
Specifically, there is a global arc into IDLE with VPD < V_Reset_PD * other_conditions.

Because V_Reset_PD is a range, consistent with other parameters that are a range, this means the PD can choose any voltage between 0V and 2.81V and use this as the reset threshold.
This is wrong - the PD should return to IDLE and stay there whenever the voltage is less than 2.81V.

SuggestedRemedy

- Change the definition of VReset_PD in 145.3.3.3 to read as follows:
"VReset_PD max: The maximum PD reset voltage (see Table 145-26).
- Change all occurences of "VReset_PD" to "VReset_PD max" in the state diagrams in 145.3.3.7
- Change the additional information in Table 145-26, item 6 to read "See 145.3.6.1" (PD Multiple-Event class signature)
- Append a paragraph to 145.3.6.1 that reads as follows:
"V_Reset_PD, as defined in Table 145-26, is the voltage range in which the PD transitions to IDLE, thereby resetting the class event count."
- Make the same changes for dual-signature as appropriate.

Proposed Response *Response Status* **W**

TFTD

HS to check.

- Change the definition of Vreset_PD in 145.3.3.3 to read as follows:
"Vreset_PD max: The maximum PD reset voltage (see Table 145-26).
- Change all occurences of "Vreset_PD" to "Vreset_PD max" in the state diagrams in 145.3.3.7
- Change the additional information in Table 145-26, item 6 to read "See 145.3.6.1" (PD Multiple-Event class signature)
- Append a paragraph to 145.3.6.1 that reads as follows:
"V_Reset_PD, as defined in Table 145-26, is the voltage range in which the PD remains in IDLE."
- Make the same changes for dual-signature as appropriate.
- Editor to make sure Vreset_PD Max is in the constants list (overrides any comment that suggests otherwise).

Cl **145** *SC* **145.3.8** *P* **188** *L* **21** # i-156

Yseboodt, Lennart — Philips Lighting

Comment Type **ER** *Comment Status* **D** *PD Power*

Table 145-28, item 2, V_Tran_lo-2P says in the additional information "For time duration defined in 145.2.8.3".
It is not immediately apparant that this applies to transients of no more than 250 microseconds.
In general pointing to the PSE section inside of the PD section for parameters is bad.

SuggestedRemedy

- Replace add. info by: "See 145.3.8.1."
- Add the following to 145.3.8.1:
"During a voltage transient, VPD may fall as low as VTran_lo-2P for up to 250 microseconds."

Note: if the other comment on KTran/VTran is accepted, the parameter name is VTran_PD-2P rather than VTran_lo-2P.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD

Wait for outcome of 337

Cl **145** *SC* **145.3.8.2** *P* **191** *L* **27** # i-341

Jones, Chad — Cisco Systems, Inc.

Comment Type **ER** *Comment Status* **D**

missing comma in this text:
including any peak power drawn per 145.3.8.4 [comma] shall be calculated over a 1 second sliding

SuggestedRemedy

change to: including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding

Proposed Response *Response Status* **W**

TFTD

wait for 330, 159

TFTD CJ
I neglected to actually include the comma in my suggested remedy…
Assuming we will accept 159 (because 330 removes the shall) the sentence should read:

The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, shall be measured using a 1 second sliding window.

Cl **145** *SC* **145.3.8.2** *P* **191** *L* **27** # i-330

Abramson, David — Texas Instruments Inc

Comment Type **TR** *Comment Status* **X** *PD Power*

"The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding window."

What/Who is this a requirement on? The PSE? The guy in the lab who is measuring it during QC?

SuggestedRemedy

Change to: "The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 is calculated over a 1 second sliding window."

Proposed Response *Response Status* **W**

TFTD

HS has homework to split Pport into averaged and instantaneous.

See 159

TFTD DS
The best of both worlds:
"The maximum average power, Pclass_PD or Pclass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, is measured using a sliding window with a width of 1 second."

Change to: "The average power, Pport_PD or Pport_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, is averaged over a 1 second sliding window."

Cl **145** *SC* **145.3.8.2** *P* **191** *L* **27** # i-159

Yseboodt, Lennart — Philips Lighting

Comment Type **ER** *Comment Status* **X** *Sliding*

Topic:SLIDING
Issue: we use the concept of 'sliding windows' in our draft very inconsistently, the SLIDING comments try to make the whole bunch consistent.
Aim: get everything in the form "measure xxx using a xx time sliding window".

"The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be calculated over a 1 second sliding window."

SuggestedRemedy

"The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4 shall be measured using a 1 second sliding window."

Proposed Response *Response Status* **W**

TFTD

See 330

TFTD DS
The best of both worlds:
"The maximum average power, PClass_PD or PClass_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, is measured using a sliding window with a width of 1 second."

TFTD CJ
I neglected to actually include the comma in my suggested remedy…
Assuming we will accept 159 (because 330 removes the shall) the sentence should read:

The maximum average power, P Class_PD or P Class_PD-2P in Table 145-28 or PDMaxPowerValue in 145.5.3.3.3, including any peak power drawn per 145.3.8.4, shall be measured using a 1 second sliding window.

Cl **145** *SC* **145.3.8.4.1** *P* **193** *L* **41** # i-483

Bennet, Ken

Comment Type **T** *Comment Status* **D** *PD Power*

"This comment addresses all statements in this paragraph that reference Pport_PD (and Pport_PD-2P). One example is: ""the peak power shall not exceed PPort_PD for...."".

""Pport_PD"" is the input average power. The statements should reference the MAXIMUM input average power to be correct. "

SuggestedRemedy

For each occurrence of Pport_PD and Pport_PD-2P, either preceed it with "maximum", or add a "_max" suffix.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD Ken and Lennart have homework.

Editorial license given to make sure maximum is apporpriate for each occurance.

TFTD LY
Agree with prepending with word “maximum”. Ken - please provide specific editing instructions.

Cl **145** *SC* **145.3.8.6** *P* **194** *L* **4** # i-484

Bennett, Ken

Comment Type **T** *Comment Status* **X** *PD Power*

"The sentence starting with ""A single-signature PD includes CPort..."" leads into a listing of PD Types and Cport values that ""Intrinsically meet the requirements in this subclause"". These are informative statements, and are not entirely correct:

1) A type 4 PD with 360uF can be assigned a class corresponding to Type 3 limits. The Type 3 limit is 180uF, so the Type 4 limit of 360uF is not true in this case.

2) It's conceivable for any of the cases that a transient could cause a power surge and/or fault in a PD for reasons other than just Cport."

SuggestedRemedy

Delete the text starting at line 4 ("A single signature PD includes...") and ending at line 17, just after the list of PD types and capacitances.

Proposed Response *Response Status* **W**

TFTD

Should we just transition this list to class based?

Issues:
list doesn't work for demotion
list doesn't consider active bridges

Cl **145** *SC* **145.3.8.6** *P* **194** *L* **30** # i-315

Stover, David Analog Devices Inc.

Comment Type **TR** *Comment Status* **D** *PD Power*

*** Comment submitted with the file 94179800003-i_tr_3.png attached ***

Math for TR3 doesn't pencil out given the input cap requirements listed in this section. See attachment for simulation showcasing the problem statement. As a result, I_TR_LIM,max for assigned Class >= 5 needs slightly increased.

SuggestedRemedy

Modify I_TR3,max for single-signature PDs assigned Class >= 5 from "3" to "3.1"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD. Table 145-29 needs to be fixed for 2p vs. 4p current limits.

Change sentence from: When transient TR3 is applied, the peak current shall not exceed ITR_LIM, as defined in Table 145–30, and
the PD shall meet the operating power limits after 4 ms.

To: When transient TR3 is applied, the PD shall meet the operating power limits within 4 ms.

Delete table 145-30

Cl **145** *SC* **145.3.8.6** *P* **194** *L* **37** # i-338

Lemahieu, Joris ON Semiconductor

Comment Type **TR** *Comment Status* **D** *PD Power*

The PD state diagram states that does not need to implement a current limit in the POWERED state.
(pd_current_limit <= FALSE)

This new ITR_LIM spec now seems to indicate the opposite.

SuggestedRemedy

Suppress the ITR_LIM requirement:
- Delete "the peak current shall not exceed ITR_LIM, as defined in Table 145-30, and"
- Delete Table 145-30

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 315

TFTD

Cl **145** *SC* **145.3.8.10** *P* **196** *L* **7** # i-487

Johnson, Peter

Comment Type **T** *Comment Status* **X** *Pres: Darshan15*

The text "Single-signature PDs shall not exceed ICon-2P-unb for longer than TCUT-2P min and 5 % duty cycle, and shall not exceed IPeak-2P-unb, as defined in Equation (145-12) on any pair..." fails to account for the fact that there are many combinations of PSE voltage and PD class where IPeak-2P_unb is a value LESS than ICon-2P-unb. It makes no sense that peak power must be less than continuous power.

SuggestedRemedy

This creates a fundmental dilemma because IPeak-2P_unb is a function of V_PSE and therefore only the PSE knows what IPeak-2P_unb current is, not the PD. To be universal, PD current balance, both instantaneous and average, must therefore be restricted to Icon-2P-unb. Language would be: "Single-signature PDs shall not exceed ICon-2P-unb on any pair..."

Proposed Response *Response Status* **W**

TFTD

Cl **145** *SC* **145.3.8.10** *P* **196** *L* **7** # i-313

Stover, David Analog Devices Inc.

Comment Type **TR** *Comment Status* **D** *Pres: Yseboodt3*

Icon-2p-unb has no maximum; this statement ("Single-signature PDs shall not exceed ICon-2P-unb for longer than TCUT-2P min and 5% duty cycle") does not enforce any current limitation on the PD.

SuggestedRemedy

Change "Icon-2p-unb" to "Icon-2p-unb,min"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD LY
See yseboodt 03 which makes ICon-2P-unb a maximum.

Cl **145** *SC* **145.3.8.10** *P* **197** *L* **1** # i-173

Yseboodt, Lennart Philips Lighting

Comment Type **TR** *Comment Status* **X** *Pres: Darshan3*

Calculations using the model in Figure 145-31, Equation 145-27, and Equation 145-26 show that pair currents often exceed ICon-2P-unb, even though line 39 on page 195 promises: "PDs that meet Equation (145-26) intrinsically meet unbalance requirements."

I guess... that changes in earlier drafts to power parameters require us to update the magic numbers in Equation 145-26.

SuggestedRemedy

Don't know how to fix this... Yair ?

Proposed Response *Response Status* **W**

TFTD

TFTD YD
See darshan_03_0917.pdf for remedy

WFP

Cl **145** *SC* **145.4.6** *P* **205** *L* **42** # i-219

Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** *Comment Status* **D** *AES*

E_d_out is a time domain peak to peak voltage but the formula defines E_d_out as varying across frequency. E_d_out isn't measured at individual frequencies.

SuggestedRemedy

delete formula (145-31) and the text defining f and fmax
change text on line 38 from:
"shall not exceed the requirements Equation (145-31)" (note the missing 'of')
to "shall not exceed 10 mV peak-to-peak when measured in the band from 1 MHz to 10 MHz and shall not exceed 1mV peak-to-peak when measured in the band from 10 MHz to 100 MHz for 2.5GBASE-T, 10 MHz to 250 MHz for 5GBASE-T, and 10 MHz to 500 MHz for 10GBASE-T"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD GZ

Same as 227

Cl **145** *SC* **145.4.7** *P* **205** *L* **51** # i-387

Thompson, Geoffrey Individual

Comment Type **TR** *Comment Status* **X** *AES*

It is unclear whether this is a spec for the cabling or a load spec for the PSE. It needs to have a more complete requirement and be moved to the PSE or link segment clause. Expressing it in terms of the "PHY" and the "MDI" causes further confusion as which MDI is not specified nor is what to be done for a midspan system.

SuggestedRemedy

Clarify and place as appropriate.

Proposed Response *Response Status* **W**

TFTD

LDR GT

Cl **145** *SC* **145.4.9.2** *P* **210** *L* **19** # i-336

Maguire, Valerie The Siemon Company

Comment Type **T** *Comment Status* **D** *AES*

Support of 2.5GBASE-T with category 5e and support of 5GBASE-T with category 6 is only in the case that the cabling meets the additional requirements specified in clause 126.7 of 802.3bz.

SuggestedRemedy

Add a footnote referencing back to the 2.5GBASE-T and 5GBASE-T column rows that says, "For defined uses cases (refer to IEEE Std 802.3bz(TM)-2016). Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2 recommended."

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

GZ has homework now…

TFTD LY
Very terse sentences,,, suggest: “For defined use cases refer to IEEE Std 802.3bz™-2016. Use of Category 6A cord in ISO/IEC 11801-1 or ANSI/TIA-568-C.2 is recommended.”

TFTD CJ
I don’t know that we reference to specific TF documents (802.3bz…) nor use ™ in our docs. At a minimum replace BZ with Clause 126.

Cl **145** *SC* **145.5.3.6.3** *P* **226** *L* **2** # i-441

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

This comment is marked LLDP?_ADHOC_1.
In the LLDP adhoc we made some changes to the PSE DLL state machine to reflect the changes made in the concept of how to fill in the TLV values of the pse_allocated_power and pse_allocated_power_alt(X) fields.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDP.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.5.3.6.3** *P* **226** *L* **5** # i-442

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

This comment is marked LLDP?_ADHOC_2.
This comment and proposed remedy depend on the outcome of the LLDP adhoc recommendations regarding the question if pse_dll_ready_alt(X) need to be specified per alternative as currently is or need to be pse_dll_ready. In case that it is going to be pse_dll_ready, see the proposed remedy.

SuggestedRemedy

1. Change from: " (!pse_dll_enable_alt(X) + !pse_dll_ready_alt(X)) * (sig_type = dual)"
To: (!pse_dll_enable_alt(X) + !pse_dll_ready * (sig_type = dual)
2. In page 224 line 41 to change the pse_dll_ready_alt(X) variable definition to:
"pse_dll_ready
An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:
FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization.
3. Delete aLldpXdot3LocReadyA and aLldpXdot3LocReadyB from Table 30-7.
4) Delete 30.12.2.1.18a aLldpXdot3LocReadyA content.
5) Delete 30.12.2.1.18b aLldpXdot3LocReadyB content.
6) In Table 145-50 page 222 in the PSE section: Change from "aLldpXdot3LocReadyA" to "aLldpXdot3LocReady" and from "pse_dll_ready_alt(X=A)" to "pse_dll_ready)" .
7) In Table 145-50 page 222 in the PSE section: Delete "aLldpXdot3LocReadyB" and "pse_dll_ready_alt(X=B)".

Proposed Response *Response Status* **W**

TFTD

Need input from LLDP ad hoc.

Cl **145** *SC* **145.5.3.7.4** *P* **229** *L* **2** # i-443

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

This comment is marked LLDP?_ADHOC_3.
In the LLDP adhoc we made some changes to the PD DLL state machine to reflect the changes made in the concept of how to fill in the TLV values of the pd_requested_power and pd_requested_power_mode(X) fields.

SuggestedRemedy

Adopt yseboodt_04_0917_LLDP.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145** *SC* **145.5.3.7.4** *P* **229** *L* **5** # i-444

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Yseboodt4*

This comment is marked LLDP?_ADHOC_4.
In the condition (!pd_dll_enable_mode(X) + !pd_dll_ready_mode(X)) to the IDLE state the pd_dll_ready_mode(X) need to be pd_dll_ready In order to allow progressing to the INITIALIZE state in case PD want power on the unpowered pairset.

SuggestedRemedy

1. Change from: "(!pd_dll_enable_mode(X) + !pd_dll_ready_mode(X))"
To: (!pd_dll_enable_mode(X) + !pd_dll_ready)
2. In page 228 line 28 to change the pd_dll_ready_mode(X) variable definition to:
"pd_dll_ready
An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:
FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization."
3) In Table 145-40 page 222, PD section: Change from "aLldpXdot3LocReadyA" to "aLldpXdot3LocReady" and from "pd_dll_ready_mode(X=A)" to "pd_dll_ready)".
4. In Table 145-40 page 222, PD section delete the row "aLldpXdot3LocReadyB" , "pd_dll_ready_mode(X=B)"

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145A** *SC* **145A.2** *P* **261** *L* **39** # i-185

Yseboodt, Lennart — Philips Lighting

Comment Type **E** *Comment Status* **D** *Annex*

Rdiff is defined in equation 145A-3 but nowhere used.

SuggestedRemedy

Remove equation 145A-3 + the sentence above.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

TFTD YD
Rdiff is required. It is the 100 miliohm. We need to integrate Rdiff in the text and then it will be OK

Cl **145A3** *SC* **145A3.1** *P* **262** *L* **51** # i-447

Darshan, Yair

Comment Type **E** *Comment Status* **X** *Pres: Darshan7*

In the text: "The effective resistance is the measured voltage Veff, divided by the current through the path e.g. the effective value of RPSE_min for i1 is RPSE_min=Veff1 / i1 as shown in Figure 145A-2.". The effective resistance of what?

SuggestedRemedy

Change the mentioned text to (**):
"The effective resistance **Rpse_min or RPSE_max** is the measured voltage Veff, divided by the current through the path e.g. the effective value of RPSE_min for i1 is RPSE_min=Veff1 / i1 as shown in Figure 145A-2.

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145A3** *SC* **145A3.2** *P* **262** *L* **52** # i-448

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan7*

The verification procedure of the measurements of Rpse_min and Rpse_max is missing from 145A.3

SuggestedRemedy

Add the following text after line 54 in page 262:
"Rpse_min and RPSE_max effective resistance verification procedure is described below:
1) With the PSE powered on and connected to a constant power sink in the PD section through the elements shown in Figure 145A-2, which is set to PClass_PD measured at the PD PI, measure the currents i1, i2, i3 and i4 and the voltages Veff1, Veff2, Veff3 and Veff4.
2) Calculate the RPSE_min and RPSE_max values of each pair of the same polarity by calculating the following:
For the positive pairs:
R1=RPSE_min=Veff1/i1
R2=RPSE_max=Veff2/i2
For the negative pairs:
R3=RPSE_min=Veff3/i3
R4=RPSE_max=Veff4/i4
3) Verify that on each pair of the same polarity, RPSE_min and RPSE_max meets Equation 145-15.
4) Repeat steps 1 to 3 with the RCh_unb_min, RPD_min swapped location with RCh_unb_max, RPD_max. "

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145A3** *SC* **145A3.2** *P* **263** *L* **5** # i-449

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan7*

Figure 145A-2 needs some improvements and corrections:
a) It needs to be in sync with Figure 145-22 regarding the separation of Rload_min/max to its components in order to allow setting Pclass_PD at the PD PI.
B) To describe the PSE load in a clear way.
C) Adding the borders of the link section
d) defining from what Rpse_min and Rpse_max consist of?
e) Clear definition of the measurements point of Veff_i
f) To correct the left border of the End to End pair to pair resistance arrow.

SuggestedRemedy

Replace Figure 145A-2 with the new proposal in darshan_07_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145B** *SC* **145B** *P* **267** *L* **7** # i-451

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan11*

Figure 145B-6 for the staggered option for the dual signature for CC_DET_SEQ=1, shows that the second alternative
DETECTION starts only after the Power up of the primary alternative which is OK but not limited just to this use case. The detection can starts also after the detection of the primary alternative. We need show it by additional drawing (145-6A), or drawing that shows all possibilities.

SuggestedRemedy

Adopt darshan_11_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145B** *SC* **145B.1.2** *P* **267** *L* **11** # i-452

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan11*

The title of Figure 145B-6 is "Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual,
staggered power on" which is correct per the drawing description however per the definition of CC_DET_SEQ=1 for dual-signature in page 109 line 43, CC_DET_SEQ is about Connection check and detection sequences while if it is staggered power on or not in dual-signature PD, is not the main issue to emphasis.

SuggestedRemedy

Change the title of Figure 145b-6 from:
"Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered power on"
To : "Figure 145B-6--PSE implementing CC_DET_SEQ=1, do_cxn_chk result is dual, staggered detection and staggered power on"

Proposed Response *Response Status* **W**

TFTD

WFP

Cl **145B** *SC* **145B.1.4** *P* **268** *L* **46** # i-454

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan8*

The title of Figure 145B-11 is "Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual", missing the remain fact that it is staggered detection per the definition of CC_DET_SEQ=3 for dual-signature in page 109 line 48.

SuggestedRemedy

Change the title of Figure 145B-9 from :
"Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual"
To : "Figure 145B-11--PSE implementing CC_DET_SEQ=3, do_cxn_chk result is dual, staggered detection and staggered power on"

Proposed Response *Response Status* **W**

TFTD

WFP

The more comments about these figures I see, the more it would make sense for only optional behavior or function results are called out. For example, SEQ 3 says that CC is followed by staggered detection, so why do we need to call that out in the figure title?

Cl **145B** *SC* **145B.1.4** *P* **268** *L* **268** # i-455

Darshan, Yair

Comment Type **T** *Comment Status* **X** *Pres: Darshan8*

CC_DET_SEQ=3 means: Connection check is followed by staggered detection. Figure 145B-11 for dual-signature PD shows that CC_DEC_SEQ=3 is only possible when the Detection of the 2nd pairset starts after Tpon +Tx of 1st pairset which is possible but not the only possibility per CC_DET_SEQ=3 definition.
We need clearly to show that first we see CC, and then staggered detection, and then the classification and power_on can be staggered or not. We need to add Figure 145B-11A to show this possibility that shows all possibilities.

SuggestedRemedy

Adopt darshan_08_0917.pdf

Proposed Response *Response Status* **W**

TFTD

WFP