Simplified classification in the State Diagram v120

Info (not part of baseline)

These are the classification related fixes that can be adopted for D2.2

Fixes to the Type 3/4 PSE state diagram

Make changes as follows in Figure 33–15 through 33–22:

FROM state	TO state	Change
DETECT_EVAL	IDLE	(pse_alternative = both) * ((det_temp = only_one) * (sig_pri ≠ valid) + (det_temp = both_neither) * (sig_sec ≠ valid) + (((CC_DET_SEQ = 0) + (CC_DET_SEQ = 3)) * (det_temp = only_one) * tdet2det_timer_done)) + (pse_alternative ≠ both) * (sig_pri ≠ valid)
IDLE_INRUSH_PRI	MONITOR_INRUSH_PRI	alt_pwrd_pri ~~* !pwr_app_pri~~
IDLE_INRUSH_SEC	MONITOR_INRUSH_SEC	alt_pwrd_sec ~~* !pwr_app_sec~~

Simplified classification

Info (not part of baseline)

Below are the 'shall' statements currently still in the variable list. They will be removed from the variable list in January, we can already include the requirements in the classification section.

33.2.7 PSE classification of PDs and mutual identification

Change the text on page 106, line 5 as follows:

Physical Layer classification occurs before a PSE supplies power to a PD, when the PSE asserts a voltage in the range of V Class as defined in Table 33–17 onto one or both pairsets. This is called a class event. The PD responds to each class event with a current representing one of a limited number of classification signatures.

The assigned Class is the result of the PDs requested Class and the number of class events produced by the PSE as shown in Table 33–13 and Table 33–14. See 33.3.6 for PD classification behavior. When a single- signature PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE shall assign~~s~~ the PD to Class 3, 4, or 6, whichever is the highest that it can support. When a dual-signature PD requests a higher Class than a Type 3 or Type 4 PSE can support, the PSE assigns the PD Class 3 or 4, whichever is the highest that it can support.

33.2.7.2 PSE Multiple-Event Physical Layer classification

Make changes to 33.2.7.2 as follows:

Type 2 PSEs shall provide a maximum of two class events and two mark events. Type 3 PSEs shall provide a maximum of four class events and four mark events for single-signature PDs and a maximum of three class events and three mark events on each pairset for dual-signature PDs unless a class reset event clears the class and mark event counts. Type 4 PSEs shall provide a maximum of five class events and five mark events for single-signature PDs and a maximum of four class events and four mark events on each pairset for dual-sig- nature PDs unless a class reset event clears the class and mark event counts. Type 3 and Type 4 PSEs may issue a class reset event to perform mutual identification or to discover the requested Class of the PD when the PSE's power budget only allows a single classification event.

All class event voltages and mark event voltages shall have the same polarity as defined for $V_{Port\_PSE\text{-}2P}$ in 33.2.4. Type 3 and Type 4 PSEs may issue classification events on one or both pairsets, when connected to a single-signature PD and operating over 4-pairs.

Fixes to the PD state diagram

Info (not part of baseline)

No default value is set for the variable pse_dll_power_type. This causes an invalid comparison on the exit from MDI_POWER1 to MDI_POWER2. Best solution is to set pse_dll_power_type to '1' in the IDLE state.

Append the IDLE state in Figure 33–32 with the statement as follows:

pse_dll_power_type $\Leftarrow$ 1