Replace Table 33–17 items (7) and (8) as follows:

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	Applies to all Type 1 and 2 PSEs. Applies to Type 3 and 4 PSEs when both pairsets are in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			~~0.800~~ 0.650	0.900	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~
8	Output current per pairset in the POWER_UP state as function of the assigned Class						
	Single-signature PD Class 0 to 4 Dual-signature PD Class 1 to 4	$I_{Inrush-2P}$	A	0.400	0.450	3, 4	Applies to Type 3 and 4 PSEs when only one pairset is in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	~~Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4~~			~~0.150~~	~~0.600~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5			~~0.400~~ 0.325	0.600	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~

Replace Table 33–28 items (6) and (7) as follows:

6	Input inrush current						
	Single-signature PD Class 0 to 6 Dual-signature PD Class 1 to 4	I_{Inrush_PD}	A		0.400	All	Peak value—See 33.3.7.3
	Single-signature PD Class 7to 8 Dual-signature PD Class 5				~~0.800~~ 0.650	4	
7	Input inrush current per pairset						
	Dual-signature PD Class 1 to 4	$I_{Inrush\_PD\text{-}2P}$	A		0.400	3	Peak value—See 33.3.7.3
	~~Single-signature PD~~ ~~Class 5 to 6~~ ~~Dual-signature PD~~				~~0.300/~~ ~~TBD~~	~~3, 4~~	
	~~Single-signature PD~~ ~~Class 7 to 8~~ Dual-signature PD Class 5				~~0.600~~ 0.325	4	

Modify section 33.3.7.3 as follows:

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with $V_{port\_PD\text{-}2P}$ requirements as defined in Table 33–28, and ending when C_{Port} has reached a steady state and is charged to 99% of its final value. This period shall be less than $T_{Inrush\text{-}2P}$ min per Table 33–17, with the PSE minimum inrush behavior defined in 33.2.8.5. All PDs shall consume a maximum of Type 1 power for at least $T_{delay\text{-}2P\ min}$. This allows the PSE to properly complete inrush.

Editor's Note: This paragraph has changed as a result of MR1277. Do not change this paragraph without consulting the request of MR1277.

$T_{delay\text{-}2P}$ for each pairset starts when $V_{PD\text{-}2P}$ crosses the PD power supply turn on voltage, V_{On_PD}. This delay is required so that the Type 2, Type 3 and Type 4 PD does not enter a high power state before the PSE has had time to switch current limits on each pairset from $I_{Inrush\text{-}2P}$ to $I_{LIM\text{-}2P}$.

~~Input inrush currents at startup, IInrush_PD and IInrush_PD-2P are limited by the PSE if CPort per pairset is less than 180 µF for:~~

~~— single-signature PDs, assigned to Class 0 to 6~~

~~— dual-signature PDs assigned to Class 1 to 5~~

~~and if CPort per pairset is less than 360 µF for single-signature PDs assigned to Class 7 to 8, as specified in Table 33–17. If C_{Port} per pairset is larger, input inrush current shall be limited by the PD such that $I_{Inrush\_PD\ max}$ and $I_{Inrush\_PD\_2P\ max}$ are satisfied.~~

For Type 1 and Type 2 PDs, input inrush current at startup is limited by the PSE if $C_{Port} < 180\ \mu F$, as specified in Table 33–11.

For Type 1 and Type 2 PDs, if $C_{Port} \geq 180\mu F$, input inrush current shall be limited by the PD so that $I_{Inrush\_PD\ max}$ is satisfied.

The PSE minimum guaranteed charge when both pairsets are in POWER_UP state, Q_{Inrush}, is described by Equation 33–A:

$$\{Q_{Inrush}\}_C = I_{Inrush\ min} * T_{Inrush\text{-}2P\ min} \qquad (33\text{–}A)$$

Input inrush current at startup I_{Inrush_PD} is limited by the PSE if the combination of PD C_{Port} and I_{Load} satisfy Equation (33–B).

$$\{Q_{Inrush}\}_C > \{C_{Port} * V_{Port\_PSE\text{-}2P\ max}\}_C + \{I_{Load} * t_{Inrush\text{-}2P\ min}\}_C \qquad (33\text{–}B)$$

where

C_{Port} is the total capacitance seen on both pairsets as defined in Figure 33–33

I_{Load} is the PD load current during PSE POWER_UP state on both pairsets simultaneously

For all Type 3 and Type 4 PDs, if the combination of C_{Port} and I_{Load} exceeds the PSE minimum guaranteed charge Q_{Inrush}, input inrush current shall be limited by the PD such that I_{Inrush_PD-max} is satisfied.

The PSE minimum guaranteed charge when only one pairset is in POWER_UP state, $Q_{Inrush-2P}$, is described by Equation 33–C:

$$\{Q_{Inrush-2P}\}_C = I_{Inrush-2P\ min} * T_{Inrush-2P\ min} \quad (33–C)$$

Input inrush current at startup I_{Inrush_PD-2P} is limited by the PSE if the combination of PD C_{Port} and $I_{Load-2P}$ satisfy Equation (33–D).

$$\{Q_{Inrush-2P}\}_C > \{C_{Port} * V_{Port\_PSE-2P\ max}\}_C + \{I_{Load-2P} * t_{Inrush-2P\ min}\}_C \quad (33–D)$$

where

C_{Port} is the capacitance seen on a particular pairset as defined in Figure 33–33
$I_{Load-2P}$ is the PD load during PSE POWER_UP state on only that pairset

For Type 3 and Type 4 dual-signature PDs, if the combination of C_{Port} and $I_{Load-2P}$ exceeds the PSE minimum guaranteed charge $Q_{Inrush-2P}$, input inrush current shall be limited by the PD such that $I_{Inrush\_PD-2P\ max}$ is satisfied.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after $T_{inrush-2P\ min}$. See 33.2.8.4 for details.

C_{Port} in Table 33–28 is the total PD input capacitance during POWER_UP and POWER_ON states that a PSE encounters when operating one or both pairsets, when connected to a single-signature PD. When a PSE is connected to a dual-signature PD, C_{Port} value requirements are specified in 33.3.7.6. See Figure 33–33 for a simplified PSE-PD C_{Port} interpretation model.

Remove section 33.2.8.5.1:

~~33.2.8.5.1 IInrush-2P minimum and IInrush minimum requirements~~

~~A Type 4 PSE, when connected to a single signature PD with assigned Class 7 or Class 8, may optionally implement a minimum IInrush-2P and IInrush lower than defined in Table 33–17, but not less than 0.15A and 0.4A respectively. When a Type 4 PSE is connected to a single-signature PD with assigned Class 7 or Class 8 and uses a lower IInrush-2P and IInrush than those defined in Table 33–17, it shall successfully power up a single-signature PD comprised of a parallel combination of CPort per pairset as defined in 33.3.7.3 and a Class 2 load within TInrush-2p min without startup oscillations during the POWER_UP period, when connected to the PD through channel resistance of 0.1Ω to 12.5Ω per pairset.~~