145.7 Protocol implementation conformance statement (PICS) proforma for Clause 145, Power over Ethernet[4]

145.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 145, Power over Ethernet, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

145.7.2 Identification

145.7.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

145.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bt-201x, Clause 145, Power over Ethernet
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bt-201x.)	
Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

145.7.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT3	Type 3 PD implementation	145.3.1	PD is Type 3	O	Yes [ ] No [ ]
*PDT3L	Type 3 PD implementation	145.3.1	PD is Type 3 and requests Class 1, Class 2, or Class 3	O	Yes [ ] No [ ]
*PDT3H	Type 3 PD implementation	145.3.1	PD is Type 3 and requests Class 4, Class 5, or Class 6	O	Yes [ ] No [ ]
*PDT4	Type 4 PD implementation	145.3.1	PD is Type 4	O	Yes [ ] No [ ]
*PDSS	Single-signature PD	145.3.1	PD is single-signature	O	Yes [ ] No [ ]
*PDDS	Dual-signature PD	145.3.1	PD is dual-signature	O	Yes [ ] No [ ]
*PDCL	PD Classification	145.3.6	PD supports classification	PDT3:M PDT4:M	Yes [ ] No [ ]
*PDAC	Autoclass implementation	145.3.6.2	PD supports Autoclass	O	Yes [ ] No [ ]
*PDCLM	Implementation supports Multiple-Event class signature	145.3.6	PD supports Multiple-Event class signature	PDT3:M PDT4:M	Yes [ ] No [ ]
*WEXP	Implementation supports exceeding P_{Class_PD}	145.3.8.2.1, 145.3.8.4.1	PD supports behavior described in 145.3.8.2.1 and 145.3.8.4.1	PDT3:O PDT4:O	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	145.5	PD supports Data Link Layer classification	PDT3L:O PDT3H:M PDT4:M	Yes [ ] No [ ]

145.7.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET3	Type 3 PSE implementation	145.2.1	Optional	O	Yes [ ] No [ ]
*PSET3L	Type 3 PSE implementation	145.2.1	Type 3 PSE that supports up to Class 4 power	O	Yes [ ] No [ ]
*PSET4H	Type 3 PSE implementation	145.2.1	Type 3 PSE that support more than Class 4 power	O	Yes [ ] No [ ]
*PSET4	Type 4 PSE implementation	145.2.1	Optional	O	Yes [ ] No [ ]
*PSE4P	4-pair capability	145.2.1	PSE supports powering over 4 pairs	PSET3L:O PSET3H:M PSET4:M	Yes [ ] No [ ]
*MID	Midspan PSE	145.2.3	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	145.2.3	Midspan PSE implements Alternative A	MID:O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	145.2.7	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	145.5	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*SEPLC	Implementation supports Single-Event Physical Layer classification	145.2.7.1	Optional	O	Yes [ ] No [ ]
*MEPLC	Implementation supports Multiple-Event Physical Layer classification	145.2.7.1	Optional	PDT3:M PDT4:M	Yes [ ] No [ ]
*PSEAC	Autoclass implementation	145.2.7.2	PSE implements Autoclass	O	Yes [ ] No [ ]
*PA	Power Allocation	145.2.9	PSE implements power supply allocation	O	Yes [ ] No [ ]
*DC	Monitor DC MPS	145.2.10.1.2	PSE monitors for DC MPS	PSET3:M PSET4:M	Yes [ ] No [ ]

145.7.3 PICS proforma tables for Power over Ethernet

145.7.3.1 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	145.2.2	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	PSE permitted polarity configurations	145.2.4	To be associated with Alternative A or Alternative B listed in Table 145–4 corresponding with their Type	M	Yes [ ]
PSE3	Alternative A and Alternative B for Type 3 PSEs	145.2.4	Implement Alternative A, Alternative B, or both	PSET3:M	Yes [ ] N/A [ ]
PSE4	Alternative A and Alternative B for Type 3 PSEs providing Class 5 or Class 6 power levels and Type 4 PSEs	145.2.4	Implement Alternative A and Alternative B	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE5	PSE behavior for Type 3 and Type 4 PSEs	145.2.5	In accordance with state diagrams shown in Figure 145–13 to Figure 145–19	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE6	PSE performing detection only on Alternative B fails to detect a valid PD detection signature	145.2.5.1	Back off for at least T_{dbo} as defined in Table 145–16 before attempting another detection, except in the case of an open circuit as defined in 145.2.6.6	M	Yes [ ]
PSE7	Backoff voltage	145.2.5.1	Not greater than V_{Off}	M	Yes [ ]
PSE8	Alternative roles during 4-pair operation	145.2.5.1	Established in IDLE and maintained in every other state	PSE4P:M	Yes [ ] N/A [ ]
PSE9	pse_avail_pwr, pse_avail_pwr_pri, and pse_avail_pwr_sec	145.2.5.4	Set from the range described in Table 145–6	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE10	Applying operating voltage to a pairset	145.2.6	Not until a valid signature has been successfully detected on that pairset	M	Yes [ ]
PSE11	Connection check	145.2.6.1	Complete connection check prior to the classification of a PD, as defined in 145.2.7 to determine if both pairsets are connected to a single-signature PD, dual signature PD, or neither	PSE4P:M	Yes [ ] N/A [ ]
PSE12	Open circuit voltage and short circuit voltage during connection check	145.2.6.1	Meet the specifications in Table 145–8	PSE4P:M	Yes [ ] N/A [ ]
PSE13	Determining between single-signature and dual-signature PDs	145.2.6.1	Only for tests that result in a voltage at the PSE PI that is below V_{valid} max as defined in Table 145–8	PSE4P:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE14	Voltage on either pairset rises above V_{valid} max during connection check	145.2.6.1	Reset the PD by bringing the voltage at the PI below V_{off} max for at least T_{Reset}, before performing classification	PSE4P:M	Yes [ ] N/A [ ]
PSE15	Detecting PDs	145.2.6.2	Performed via the PSE PI	M	Yes [ ]
PSE16	PSE presents non-valid signature	145.2.6.2	As defined in Table 145–22 when probed in either polarity by another PSE	M	Yes [ ]
PSE17	Open circuit voltage and short circuit current	145.2.6.2	Meet specifications for V_{oc} and I_{sc} in Table 145–8	M	Yes [ ]
PSE18	Backdriven current	145.2.6.2	Not be damaged by up to 5 mA over the range of V_{oc}	M	Yes [ ]
PSE19	Output capacitance	145.2.6.2	C_{out} in Table 145–16	M	Yes [ ]
PSE20	Detection voltage with a valid PD signature connected	145.2.6.3	Meets V_{valid} in Table 145–8	M	Yes [ ]
PSE21	Detection voltage measurements	145.2.6.3	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE22	Control slew rate when switching detection voltages	145.2.6.3	Less than V_{slew} as defined in Table 145–8	M	Yes [ ]
PSE23	Accept as a valid signature	145.2.6.4	From a pairset with all of the characteristics specified in Table 145–9	M	Yes [ ]
PSE24	Reject as an invalid signature	145.2.6.5	From a pariset with resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min as specified in Table 145–10	M	Yes [ ]
PSE25	Applying operating voltage to both pairsets	145.2.6.7	Not until it is determined whether the attached PD is a candidate to receive power on both pairsets	PSE4P:M	Yes [ ] N/A [ ]
PSE26	4PID	145.2.6.7	A logical function of the detection state of both pairsets, the result of connection check, mutual identification, and of the Power via MDI TLV	PSE4P:M	Yes [ ] N/A [ ]
PSE27	4PID variable	145.2.6.7	Stored in pd_4pair_cand, defined in 145.2.5.4	PSE4P:M	Yes [ ] N/A [ ]
PSE28	Applying 4-pair power	145.2.6.7	Not unless a valid detection signature has been detected on both pairsets and one or more of the three conditions described in 145.2.6.7 have been met	PSE4P:M	Yes [ ] N/A [ ]
PSE29	Channel resistance considerations for $P_{Autoclass}$	145.2.7	Increase $P_{Autoclass}$ by at least P_{ac_margin}	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE30	Type 3 and Type 4 PSE successful detection	145.2.7	Subsequently perform Multiple-Event Physical Layer classification	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE31	Type 3 and Type 4 PSEs that will source 4-pair power attached to dual-signature PD	145.2.7	Perform Physical Layer classification on both pairsets	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE32	Class assignment	145.2.7	Capable of assigning the highest supported Class through Multiple-Event Physical Layer Classification	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE33	Fail to complete classification of a single-signature PD after successfully completing detection	145.2.7	Return to IDLE	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE34	Fail to completed classification of a dual-signature PD after successfully completing detection	145.2.7	Return to IDLE corresponding to the appropriate Alternative	PSET3:M PSET4:M	Yes [ ] N/A [ ]
PSE35	Type 3 PSE class and mark events	145.2.7.1	Provide a maximum of four class events and four mark events for single-signature PDs and a maximum of three class events and three mark events on each pairset for dual-signature PDs	PSET3:M	Yes [ ] N/A [ ]
PSE36	Type 4 PSE class and mark events	145.2.7.1	Provide a maximum of five class events and five mark events for single-signature PDs and a maximum of four class events and four mark events on each pairset for dual-signature PDs	PSET4:M	Yes [ ] N/A [ ]
PSE37	Number of class events issued	145.2.7.1	No more than the Class they are capable of supporting between the most recent time V_{PSE} was at V_{Reset} for at least T_{Reset} and a transition to any of the power up states	M	Yes [ ]
PSE38	Classification timing in CLASS_EV1_LCE, CLASS_EV1_AUTO, CLASS_EV1_LCE_PRI, CLASS_EV1_LCE_SEC, CLASS_EV1_LCE_4PID_PRI, or CLASS_EV1_LCE_4PID_SEC	145.2.7.1	Provide V_{Class} to the PI or pairset, subject to the T_{LCE} timing specification	M	Yes [ ]
PSE39	Measure I_{Class} in CLASS_EV1_AUTO	145.2.7.1	After T_{Class_ACS}, referenced from the application of the first class event, to determine if the PD will perform Autoclass	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE40	Classification timing in CLASS_EV2, CLASS_EV2_-PRI, CLASS_EV2_SEC, CLASS_EV3, CLASS_EV3_-PRI, CLASS_EV3_SEC, CLASS_EV4, CLASS_EV4_-PRI, CLASS_EV4_SEC, or CLASS_EV5	145.2.7.1	Provide V_{Class} to the PI or pairset, subject to the T_{CEV} timing specification	M	Yes [ ]
PSE41	Measure I_{Class} in all CLASS states except CLASS_EV1_AUTO	145.2.7.1	After T_{Class}	M	Yes [ ]
PSE42	Timing in MARK_EV1, MARK_EV1_PRI, MARK_EV1_SEC, MARK_EV2, MARK_EV2_-PRI, MARK_EV2_SEC, MARK_EV3, MARK_EV3_-PRI, MARK_EV3_SEC, or MARK_EV4	145.2.7.1	Provide V_{Mark} to the PI or pairset, subject to the T_{ME1} timing specification	M	Yes [ ]
PSE43	Timing in MARK_EV_LAST, MARK_EV_LAST_PRI, or MARK_EV_LAST_SEC	145.2.7.1	Provide V_{Mark} to the PI or pairset, subject to T_{ME2} timing specifications	M	Yes [ ]
PSE44	I_{Class} measured equal to or greater than I_{Class_LIM} min	145.2.7.1	Return to IDLE	M	Yes [ ]
PSE45	Class event currents	145.2.7.1	Limit to I_{Class_LIM}	M	Yes [ ]
PSE46	Mark event currents	145.2.7.1	Limit to I_{Mark_LIM}	M	Yes [ ]
PSE47	Class event and mark event voltages polarity	145.2.7.1	Same as defined for V_{Port_PSE-2P} in 145.2.4	M	Yes [ ]
PSE48	Transition to POWER_ON, POWER_ON_PRI, or POWER_ON_SEC after completion of Multiple-Event Physical Layer classification	145.2.7.1	Without allowing the voltage at the PI or pairset to go below V_{Mark} min, unless in CLASS_RESET, CLASS_RESET_PRI, or CLASS_RESET_SEC	M	Yes [ ]
PSE49	PSE returns to IDLE	145.2.7.1	Maintain the PI voltage in the range of V_{Reset} for a period of at least T_{Reset} min before starting new detection cycle	M	Yes [ ]
PSE50	PI or pairset voltage in CLASS_RESET, CLASS_RESET_PRI, or CLASS_RESET_SEC	145.2.7.1	Maintain in the range of V_{Reset} for a period of at least T_{Reset} min	M	Yes [ ]
PSE51	PSE connected to a dual-signature PD, implementing 4PID based on classification and is restricted to Class 3 power or less	145.2.7.1	Issue three initial class events to determine the Type of the connected PD, then transition to either CLASS_RESET_-PRI or CLASS_RESET_SEC	M	Yes [ ]
PSE52	pd_autoclass TRUE when PSE reaches POWER_ON	145.2.7.2	Measure $P_{Autoclass}$	PSEAC:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE53	Power consumption	145.2.7.2	Defined as the highest average power measured throughout the period bounded by T_{AUTO_PSE1} and T_{AUTO_PSE2}	PSEAC:M	Yes [ ] N/A [ ]
PSE54	Power supply output	145.2.8	When providing power to the PI, conform with Table 145–16	M	Yes [ ]
PSE55	Load regulation	145.2.8.1	Met with (I_{Hold} max × V_{Port_PSE-2P} min) to the maximum power per the PSE's assigned Class at a rate of change of at least 15 mA/µs	M	Yes [ ]
PSE56	Voltage transients	145.2.8.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE57	PSE that has assigned Class 5 to Class 8 to a single-signature PD	145.2.8.1	Apply power to both pairsets while in a power on state	M	Yes [ ]
PSE58	Output voltage during voltage transients lasting 30 µs to 250 µs	145.2.8.3	Maintain no less than $V_{Tran-2P}$ and meet requirements of 145.2.8.8.	M	Yes [ ]
PSE59	Voltage transients lasting more than 250 µs	145.2.8.3	Meet V_{Port_PSE-2P} specification	M	Yes [ ]
PSE60	V_{Noise}	145.2.8.4	Met for common-mode and pair-to-pair noise values at all static PSE output voltages	M	Yes [ ]
PSE61	I_{Con-2P}	145.2.8.5	As defined in Equation (145–8)	M	Yes [ ]
PSE62	$I_{Peak-2P}$	145.2.8.5	As defined in Equation (145–10) on each powered pairset while withing the operating voltage range of V_{Port_PSE-2P}, for a minimum of T_{CUT} and a duty cycle of at least 5%	M	Yes [ ]
PSE63	PI connector (jack) mated with a specified balanced cabling connector (plug)	145.2.8.5.1	Meet the requirements of 145.2.8.5.1	M	Yes [ ]
PSE64	Current source when connected to a load as shown in Figure 145-22	145.2.8.5.1	Not more than $I_{Unbalance-2P}$ on any pair using values of R_{load_min} and R_{load_max} as defined in Equation (145–14) and Equation (145–15)	M	Yes [ ]
PSE65	Reach POWER_ON on both pairsets for PSEs that have assigned Class 5 to Class 8 to a single-signature PD	145.2.8.6	Within T_{Inrush} max, starting with the first pairset transitioning into the power up state, and where the second pairset transitions to a power up state anytime within this time period	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE66	$I_{Inrush-2P}$ and I_{Inrush} limits during power up	145.2.8.6	Per the requirements of Table 145–16, with the exception of initial per pair-set transient described in Equation (145–16)	M	Yes [ ]
PSE67	Short circuit condition	145.2.8.8	Remove power from a pairset of the PSE before the pairset current exceeds the "PSE upperbound template" in Figure 145–24, or Figure 145–25	M	Yes [ ]
PSE68	Short circuit current and time	145.2.8.8	In accordance with I_{LIM-2P} and T_{LIM} in Table 145–16	M	Yes [ ]
PSE69	Short circuit power removal	145.2.8.8	Begins within T_{LIM-2P} in Table 145–16	M	Yes [ ]
PSE70	Turn off time	145.2.8.9	Applies to the discharge time from V_{Port_PSE-2P} min to V_{Off} of a pairset with a test resistor of 320 kΩ attached to the pariset.	M	Yes [ ]
PSE71	Turn off voltage	145.2.8.10	Applies to the PI voltage in IDLE	M	Yes [ ]
PSE72	PI voltage in DISABLED, IDLE, or ERROR_DELAY	145.2.8.10	Equal to or less than V_{Off}, as defined in Table 145–16	M	Yes [ ]
PSE73	Pairset voltage in IDLE_PRI, WAIT_PRI, ERROR_DELAY_PRI, IDEL_SEC, WAIT_SEC, or ERROR_DELAY_SEC	145.2.8.10	Equal to or less than V_{Off}, as defined in Table 145–16	M	Yes [ ]
PSE74	Intra-pair current unbalance	145.2.8.11	Applies to the two conductors of a power pair over the current load range as defined in Equation (145–21)	M	Yes [ ]
PSE75	Endpoint PSEs transmitting 100BASE-TX in the presence of (I_{unb} / 2)	145.2.8.11	Meet the requirements of 25.4.5	M	Yes [ ]
PSE76	Type 4 PSE source power	145.2.8.12	Not more than P_{Type} max as defined in Table 145–16 measured using a sliding window with a width of up to 4 seconds	PSET4:M	Yes [ ] N/A [ ]
PSE77	Reach POWER_ON when connected to a single-signature PD	145.2.8.13	Within T_{pon} after completing detection on the last pairset	M	Yes [ ]
PSE78	Reach respective power on state when connected to a dual-signature PD	145.2.8.13	Within T_{pon} after completing detection on the same pairset	M	Yes [ ]
PSE79	Power allocation	145.2.9	Not based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE80	PSE DC MPS component requirements	145.2.11	Use the applicable I_{Hold}, $I_{Hold-2P}$, T_{MPS}, and T_{MPDO} values as defined in Table 145–16 depending on the connected PD's assigned Class and whether it is single-signature, or dual-signature	DC:M	Yes [ ] N/A [ ]
PSE81	DC MPS component present for a PSE powering a PD over a single pairset	145.2.11	If $I_{Port-2P}$ is greater than or equal to $I_{Hold-2P}$ max continuously for at least T_{MPS}	DC:M	Yes [ ] N/A [ ]
PSE82	DC MPS component absent for a PSE powering a PD over a single pairset	145.2.11	If $I_{Port-2P}$ is less than or equal to $I_{Hold-2P}$ min	DC:M	Yes [ ] N/A [ ]
PSE83	Power removal for a PSE powering a PD over a single pairset	145.2.11	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE84	Not remove power for a PSE poweing a PD over a single pairset	145.2.11	When the DC MPS has been present within the T_{MPS} + T_{MPDO} window	DC:M	Yes [ ] N/A [ ]
PSE85	DC MPS component present for a PSE powering a single-signature PD over both pairsets	145.2.11	If $I_{Port-2P}$ of the pairset with the highest current is greater than or equal to $I_{Hold-2P}$ max and I_{Port} is greater than or equal to I_{Hold} max continuously for a minimum of T_{MPS}	DC:M	Yes [ ] N/A [ ]
PSE86	DC MPS component absent for a PSE powering a single-signature PD over both pairsets	145.2.11	If $I_{Port-2P}$ of the pairset with the highest current is less than or equal to $I_{Hold-2P}$ min and I_{Port} is less than or equal to I_{Hold} min	DC:M	Yes [ ] N/A [ ]
PSE87	Power removal for a PSE powering a single-signature PD over both pairsets	145.2.11	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE88	Not remove power for a PSE powering a single-signature PD over both pairsets	145.2.11	When the DC MPS has been present within the T_{MPS} + T_{MPDO} window	DC:M	Yes [ ] N/A [ ]
PSE89	DC MPS component for a PSE powering a dual-signature PD	145.2.11	Considered to be present or absent on each pairset independently	DC:M	Yes [ ] N/A [ ]
PSE90	DC MPS component present on a pairset for a PSE powering a dual-signature PD	145.2.11	If $I_{Port-2P}$ is greater than or equal to $I_{Hold-2P}$ max continuously for a minimum of T_{MPS}	DC:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE91	DC MPS component absent for a PSE powering a dual-signature PD	145.2.11	$I_{Port-2P}$ is less than or equal to $I_{Hold-2P}$ min	DC:M	Yes [ ] N/A [ ]
PSE92	Power removal from a pairset for a PSE powering a dual-signature PD	145.2.11	When DC MPS has been absent on that pairset for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE93	Not remove power from a pairset for a PSE powering a dual-signature PD	145.2.11	When the DC MPS has been present on both pairsets within the $T_{MPS} + T_{MPDO}$ window	DC:M	Yes [ ] N/A [ ]

145.7.3.2 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	145.3.2	In any valid 2-pair configuration and any valid 4-pair configuration as defined in Table 145–19	M	Yes [ ]
PD2	Mode polarity	145.3.2	Insensitive to the polarity of the voltage applied regardless of the polarity of the voltage applied on the other Mode	M	Yes [ ]
PD3	Operation of single-signature PDs that request Class 4 or less	145.3.2	Only if power is supplied with any valid configuration defined in Table 145–20	PDSS:M	Yes [ ] N/A [ ]
PD4	Source power	145.3.2	PDs do not source power on its PI	M	Yes [ ]
PD5	Voltage tolerance	145.3.2	Withstand 0 V to 57 V at the PI indefinitely without permanent damage when applied in any valid configuration defined in Table 145–20	M	Yes [ ]
PD6	Single-signature PD behavior	145.3.3	According to state diagram shown in Figure 145–26 and Figure 145–27	PDSS:M	Yes [ ] N/A [ ]
PD7	Dual-signature PD behavior	145.3.3	According to state diagram shown in Figure 145–28 over each pairset independently unless otherwise specified	PDDS:M	Yes [ ] N/A [ ]
PD8	Valid and non-valid detection signatures	145.3.4	Presented between positive V_{PD} and negative V_{PD} of PD Mode A and PD Mode B as defined in 145.3.2	M	Yes [ ]
PD9	Single-signature PDs powered over only one pairset	145.3.4	Present a non-valid detection signature on the unpowered pairset	PDSS:M	Yes [ ] N/A [ ]
PD10	Dual signature PDs powered over only one pairset	145.3.4	Present a valid detection signature on the unpowered pairset	PDDS:M	Yes [ ] N/A [ ]
PD11	Valid detection signature	145.3.4	Characteristics defined in Table 145–21	M	Yes [ ]
PD12	Non-valid detection signature	145.3.4	Exhibit one or both of the characteristics described in Table 145–22	M	Yes [ ]
PD13	Present valid detection signature on a given Mode for single-signature PDs	145.3.5	As defined in Table 145–21 when no voltage or current is applied to the other Mode	PDSS:M	Yes [ ] N/A [ ]
PD14	Present invalid detection signature on a given Mode for single-signature PDs	145.3.5	When any voltage between 10.1 V and 57 V is applied to the other Mode	PDSS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD15	Present valid detection signature for dual-signature PDs	145.3.5	As defined in Table 145–21 on a given Mode regardless of any voltage between 0 V and 57 V, applied to the other Mode	PDDS:M	Yes [ ] N/A [ ]
PD16	Maximum power drawn across all input voltages	145.3.6	In accordance with the requested Class in Table 145–26 and Table 145–27	M	Yes [ ]
PD17	Conform to the assigned Class	145.3.6	Regardless of its requested Class	M	Yes [ ]
PD18	Multiple-Event classification	145.3.6	Mandatory for PDs	M	Yes [ ]
PD19	Data Link Layer classification	145.3.6	Mandatory for single-signature PDs that request Class 4 or higher, and dual-signature PDs that request Class 4 or higher on at least one of its modes	PDDS:M PDSS:M	Yes [ ] N/A [ ]
PD20	PD classification behavior	145.3.6	Conforms to the state diagram in Figure 145–26, and Figure 145–28	M	Yes [ ]
PD21	PD electrical specifications	145.3.6	As defined in Table 145–24 and Table 145–25	M	Yes [ ]
PD22	Underpowered PDs	145.3.6	If PD is assigned to a lower Class than the requested Class, provide user with active indication if underpowered	M	Yes [ ]
PD23	Multiple-Event Physical Layer classification during DO_-CLASS_EVENT1 and DO_-CLASS_EVENT2	145.3.6.1	Present class_sig_A as defined in Table 145–26 and Table 145–27	M	Yes [ ]
PD24	Multiple-Event Physical Layer classification during DO_-CLASS_EVENT3, DO_-CLASS_EVENT4, DO_CLASS_EVENT5, and DO_CLASS_EVENT6	145.3.6.1	Present class_sig_B as defined in Table 145–26 and Table 145–27	M	Yes [ ]
PD25	Multiple-Event Physical Layer classification during DO_-CLASS_EVENT_AUTO for Autoclass PDs	145.3.6.1	Present class_sig_0 as defined in 145.3.6.2	PDAC:M	Yes [ ] N/A [ ]
PD26	Physical Layer class signature after entering a DO_-CLASS_EVENT state	145.3.6.1	Valid within TClass_PD as defined in Table 145–29 and remain valid for the remainder of the class event	M	Yes [ ]
PD27	Advertised class signatures for single-signature PDs	145.3.6.1	In accordance with the PD Type and PD requested Class, as defined in Table 145–26	PDSS:M	Yes [ ] N/A [ ]
PD28	Advertised class signature for dual-signature PDs	145.3.6.1	In accordance with the PD Type and PD requested Class on each pairset, as defined in Table 145–27	PDDS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD29	Dual-signature PDs powered over only one pairset	145.3.6.1	Present a valid classification signature on the unpowered pairset	PDDS:M	Yes [ ] N/A [ ]
PD30	Identifying PSEs assigned Class for single-signature PDs	145.3.6.1	As defined in Table 145–11	PDSS:M	Yes [ ] N/A [ ]
PD31	Identifying PSEs assigned Class for dual-signature PDs	145.3.6.1	As defined in Table 145–11	PDDS:M	Yes [ ] N/A [ ]
PD32	PD current draw when in a DO_MARK_EVENT state	145.3.6.1.1	I_{Mark} as defined in Table 145–25and present a non-valid detection signature as defined in Table 145–22	PDCLM:M	Yes [ ] N/A [ ]
PD33	Mark event current limits	145.3.6.1.1	Not exceed I_{Mark} when voltage at the PI enters the V_{Mark_PD} specification as defined in Table 145–25	M	Yes [ ]
PD34	Responding to first class event for Autoclass PDs	145.3.6.2	Change current to class signature 0 no earlier than T_{ACS} min and no later than T_{ACS} max, as defined in Table 145–28	PDAC:M	Yes [ ] N/A [ ]
PD35	After power up for Autoclass PDs	145.3.6.2	Draw its highest required power, $P_{Autoclass\_PD}$, subject to P_{Class_PD}, throughout the period bounded by T_{AUTO_PD1} and T_{AUTO_PD2}, measured from when V_{PD} rises above V_{Port_PD-2P} min	PDAC:M	Yes [ ] N/A [ ]
PD36	Power draw for Autoclass PDs	145.3.6.2	Not more than $P_{Autoclass\_PD}$ at any point until V_{PD} falls below V_{Reset_PD} max, unless the PD successfully negotiates a higher power level, up to the PD requested Class, through Data Link Layer classification as defined in 145.5	PDAC:M	Yes [ ] N/A [ ]
PD37	PSE Type identification	145.3.7	Set long_class_event to TRUE if the first class event is longer than T_{LCE_PD} max	M	Yes [ ]
PD38	PD operation	145.3.8	Operate within the characteristics in Table 145–29	M	Yes [ ]
PD39	PD turn on voltage	145.3.8.1	At a voltage in the range of V_{On_PD}	M	Yes [ ]
PD40	PD stay on voltage	145.3.8.1	Over the entire V_{Port_PD-2P} range	M	Yes [ ]
PD41	PD turn off voltage	145.3.8.1	At a voltage in the range of V_{Off_PD}	M	Yes [ ]
PD42	Startup oscillations	145.3.8.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD43	Power consumption of single-signature PDs that have successfully completed DLL classification	145.3.8.2	Not to exceed PDMaxPowerValue as defined in 145.5.3.4.2	PDSS:M	Yes [ ] N/A [ ]
PD44	Power consumption of dual-signature PDs that have successfully completed DLL classification	145.3.8.2	Not to exceed PDMaxPowerValue_mode(X) on Mode X as defined in 145.5.3.7.3	PDDS:M	Yes [ ] N/A [ ]
PD45	Input average power exceptions for Class 6 and Class 8single-signature PDs	145.3.8.2.1	Not to consume power greater than P_{Class} at the PSE PI and not draw a total 4-pair current in excess of 2 x I_{Cable} as defined in Table 145–1	WEXP:M	Yes [ ] N/A [ ]
PD46	Input average power exceptions for Class 5 dual-signature PDs	145.3.8.2.1	Not to consume power greater than $P_{Class-2P}$ at the PSE PI and not draw current in excess of I_{Cable} as defined in Table 145–1	WEXP:M	Yes [ ] N/A [ ]
PD47	PD input inrush current when connected to source that meets 145.2.8.6 requirements	145.3.8.3	Draw less than I_{Inrush_PD} and I_{Inrush_PD-2P} from T_{Inrush_PD} max until T_{delay} min	M	Yes [ ]
PD48	P_{Class_PD} and P_{Peak_PD} for single-signature PDs assigned to Class 1, 2, or 3	145.3.8.3	Within T_{Inrush_PD} max as defined in Table 145–29	PDSS:M	Yes [ ] N/A [ ]
PD49	P_{Class_PD-2P} and P_{Peak_PD-2P} for dual-signature PDs assigned to Class 1, 2, or 3	145.3.8.3	Within T_{Inrush_PD} max as defined in Table 145–29 on that pairset	PDDS:M	Yes [ ] N/A [ ]
PD50	Peak power for any PD operating condition, with the exception described in 145.3.8.4.1 for single-signature PDs	145.3.8.4	Not to exceed P_{Class_PD} for more than T_{CUT} min and 5% duty cycle	!WEXP*PDSS:M	Yes [ ] N/A [ ]
PD51	Peak power for any PD operating condition, with the exception described in 145.3.8.4.1 for dual-signature PDs	145.3.8.4	Not to exceed P_{Class_PD-2P} for more than T_{CUT} min and 5% duty cycle	!WEXP*PDDS:M	Yes [ ] N/A [ ]
PD52	Peak operating power exceptions for Class 6 and Class 8 single-signature, and Class 5 dual-signature PDs	145.3.8.4.1	Not to exceed P_{Port_PD} for single-signature PDs and P_{Port_PD-2P} for dual-signature PDs at the PSE PI for more than T_{CUT} min as defined in Table 145–16 and with 5% duty cycle	WEXP:M	Yes [ ] N/A [ ]
PD53	Peak operating power for Class 6 and Class 8 single-signature, and Class 5 dual-signature PDs	145.3.8.4.1	Not to exceed 1.05 x P_{Port_PD} for single-signature PDs and 1.05 x P_{Port_PD-2P} for dual-signature PDs on each pairset	WEXP:M	Yes [ ] N/A [ ]
PD54	Peak transient current for single-signature PDs	145.3.8.5	Not to change faster than $I_{Slewrate}$ in either polarity as defined in Table 145–29	PDSS:M	Yes [ ] N/A [ ]
PD55	Peak transient current for dual-signature PDs	145.3.8.5	Not to change faster than $I_{Slewrate}$in either polarity per pairset as defined in Table 145–29	PDDS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD56	Presence of transients at the PSE PI lasting longer from 30 µs to 250 µs or lasting less than 30 µs and causing the voltage at the PD PI to fall to not less than 34 V	145.3.8.6	Continue to operate without interruption	M	Yes [ ]
PD57	Transient TR1 or TR2 applied	145.3.8.6	Meet the operating power limits after $T_{Transient}$ as described in Table 145–30	M	Yes [ ]
PD58	Transient TR3 applied	145.3.8.6	PD meet operating power limits within 4 ms	M	Yes [ ]
PD59	Ripple and noise	145.3.8.7	Meet V_{Noise_PD}, as defined in Table 145–29 for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry, for all operating voltages in the range of V_{Port_PD-2P} , and over the range of input power of the device	M	Yes [ ]
PD60	Ripple and noise presence	145.3.8.7	Operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD61	Backfeed voltage	145.3.8.8	Mode A and Mode B per 145.3.8.8	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD62	PI connector (jack) mated with a specified balanced cabling connector (plug)	145.3.8.9	Meet the requirements of 145.3.8.9	M	Yes [ ]
PD63	Pair-to-pair unbalance for single-signature PDs	145.3.8.9	Not to exceed $I_{Unbalance-2P}$ for longer than T_{CUT} min and 5% duty cycle	PDSS:M	Yes [ ] N/A [ ]
PD64	Pair-to-pair unbalance for dual-signature PDs	145.3.8.9	Not to exceed I_{Con-2P} for longer than T_{CUT} min and 5 % duty cycle	PDDS:M	Yes [ ] N/A [ ]
PD65	PD that requires power from the PI	145.3.9	Provide a valid MPS at the PI	M	Yes [ ]
PD66	MPS for single-signature PDs	145.3.9	Consist of current draw equal to or above I_{Port_MPS} for a minimum duration of T_{MPS_PD}	PDSS:M	Yes [ ] N/A [ ]
PD67	MPS for dual-signature PDs	145.3.9	Consist of current draw equal to or above I_{Port_MPS-2P} on each powered pairset independently for a minimum duration of T_{MPS_PD}	PDDS:M	Yes [ ] N/A [ ]
PD68	Input impedance for PDs connected to Type 1 or Type 2 PSEs	145.3.9	With resistive and capacitive components defined in Table 145–33	M	Yes [ ]
PD69	T_{MPS_PD}	145.3.9	Met with a series resistance representing the worst case cable resistance between the measurement point and the PD PI	M	Yes [ ]
PD70	Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2	145.3.9	Remove both the current draw and impedance components of the MPS	M	Yes [ ]
PD71	Powered PDs that no longer require power and identify the PSE as Type 3 or Type 4	145.3.9	Remove the current draw component of the MPS	M	Yes [ ]

145.7.3.3 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	145.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	145.4.1	Withstand at least one of the electrical strength tests specified in 145.4.1	M	Yes [ ]
EL3	Insulation breakdown	145.4.1	No breakdown of insulation during electrical isolation tests	M	Yes [ ]
EL4	Isolation resistance	145.4.1	At least 2 MΩ, measured at 500 Vdc after electrical isolation tests	M	Yes [ ]
EL5	Isolation and grounding requirements	145.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	145.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment A requirement	145.4.1.1.1	Switch more negative conductor	M	Yes [ ]
EL8	Environment B requirements for multiple instances of PSE and/or PD	145.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL9	Environment B requirements for PSE that supports 4-pair power	145.4.1.1.2	Switch more negative conductor	PS4P:M	Yes [ ] N/A [ ]
EL10	Fault tolerance for PIs encompassed within the MDI	145.4.2	Meet requirements of the appropriate specifying Clause	!MID:M	Yes [ ] N/A [ ]
EL11	Fault tolerance for PSE PIs not encompassed within an MDI	145.4.2	Meet the requirements of 145.4.2	MID:M	Yes [ ] N/A [ ]
EL12	Common-mode fault tolerance	145.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL13	The shape of the impulse for item common-mode fault tolerance	145.4.2	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value)	M	Yes [ ]
EL14	Common-mode to differential-mode impedance balance for transmit and receive pairs	145.4.3	Exceeds value in Table 145–34 for all supported PHY speeds	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL15	Common-mode AC output voltage	145.4.4	Magnitude while transmitting data and with power applied does not exceed the values in Table 145–35 while operating at the specified speed, when measured over the specified bandwidth	M	Yes [ ]
EL16	Common-mode AC output voltage measurement	145.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL17	Noise from an operating 10/100/1000 Mb/s PSE or PD to the differential transmit and receive pairs	145.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 145.4.4	M	Yes [ ]
EL18	Noise from an operating 2.5GBASE-T, 5GBASE-T, or 10GBASE-T PSE or PD to the differential transmit and receive pairs	145.4.6	Does not exceed 10 mV peak-to-peak in the 1 MHz to 10MHz band, 1 mV peak-to-peak in the 10MHz to 100MHz band for 2.5GBASE-T, 10MHz to 250MHz band for 5GBASE-T, and 10MHz to 500MHz band for 10GBASE-T	M	Yes [ ]
EL19	Return loss requirements	145.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY, in 126.8.2.2 for a 2.5 Gb/s or 5 Gb/s PHY, and in 55.8.2.1 for a 10Gb/s PHY	M	Yes [ ]
EL20	100BASE-TX Endpoint PSE and 100BASE-TX PD unbalance	145.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ]

145.7.3.4 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	145.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current for Type 3 PSEs	145.4.2	Does not exceed $I_{PSEUT\text{-}Type3\text{-}2P}$, as defined in Equation (145–17)	PSET3: M	Yes [ ] N/A [ ]
PSEEL3	Magnitude of short circuit current for Type 4 PSEs	145.4.2	Does not exceed $I_{PSEUT\text{-}Type4\text{-}2P}$, as defined in Equation (145–18)	PSET4: M	Yes [ ] N/A [ ]
PSEEL4	Limitation of electromagnetic interference.	145.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL5	Alternative A Midspan PSEs that support 100BASE-TX	145.4.8	Enforce channel unbalance currents less than or equal to 10.5mA or meet 145.4.9.3.	MIDA: M	Yes [ ] N/A [ ]
PSEEL6	Insertion of Midspan at FD	145.4.9	Comply with the guidelines specified in 145.4.9 items a), b), and c)	MID:M	Yes [ ] N/A [ ]
PSEEL7	Resulting “channel”	145.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801-1.	MID:M	Yes [ ] N/A [ ]
PSEEL8	Configurations with Midspan PSE	145.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL9	DC continuity in power injecting pairs	145.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]
PSEEL10	Connector Midspan PSE device transmission requirements	145.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE NEXT when operating with 10/100/1000 Mb/s or 2.5GBASE-T	145.4.9.1.1	Meet values determined by Equation (145–31) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE NEXT when operating with 5GBASE-T	145.4.9.1.1	Meet the values determined by Equation (145–31) from 1 MHz to 250 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL13	Midspan PSE NEXT when opearting with 10GBASE-T	145.4.9.1.1	Meet the values determined by Equation (145–31)from 1 MHz to 500 MHz, but not greater than 75 dB	MID:M	Yes [ ] N/A [ ]
PSEEL14	Midspan PSE Insertion Loss when operating with 10/100/1000 Mb/s or 2.5GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–33) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL15	Midspan PSE Insertion Loss when operating at 5GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–33) from 1 MHz to 250 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL16	Midspan PSE Insertion Loss when operating at 10GBASE-T	145.4.9.1.2	Meet values determined by Equation (145–35) from 1 MHz to 500 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL17	Midspan PSE Return Loss	145.4.9.1.3	Meet or exceed values in Table 145–36	MID:M	Yes [ ] N/A [ ]
PSEEL18	Cord Midspan PSE	145.4.9.2	Meet the requirements of this clause and the specifications for a (jumper) cord for insertion loss, NEXT, and return loss for transmit and receive pairs, as defined in Table 145–37	MID:M	Yes [ ] N/A [ ]
PSEEL19	Midspan PSE maximum link delay	145.4.9.2.1	Not to exceed 2.5 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL20	Midspan PSE maximum link delay skew	145.4.9.2.2	Not to exceed 1.25 ns from 1 MHz to the highest referenced frequency	MID:M	Yes [ ] N/A [ ]
PSEEL21	Alternative A Midspan PSE signal path requirements	145.4.9.3	Exceed transfer function gain expressed in Equation (145–34) from 0.1 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL22	Alternative A Midspan PSE signal path requirements bias current	145.4.9.3	Met with DC bias current, I_{bias}, between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]
PSEEL23	Midspan PSE PSANEXT loss for 2.5G/5G/10GBASE-T	145.4.9.4.1	Meet or exceed the values determined using the equations shown in Table 145–38 for all specified frequencies	MID:M	Yes [ ] N/A [ ]
PSEEL24	PSANEXT loss values greater than 67 dB	145.4.9.4.1	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]
PSEEL25	Midspan PSE PSAFEXT loss for 2.5G/5G/10GBASE-T	145.4.9.4.2	Meet or exceed the values determined using the equations shown in Table 145–38 for all specified frequencies	MID:M	Yes [ ] N/A [ ]
PSEEL26	PSAFEXT loss values greater than 67 dB	145.4.9.4.2	Revert to a requirement of 67 dB minimum	MID:M	Yes [ ] N/A [ ]

145.7.3.5 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	145.4.4	The PIs that require power terminated as illustrated in Figure 145–35	M	Yes [ ]

145.7.3.6 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	145.5	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	DLCC:M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	145.5.1	Meet mandatory parts of IEEE Std 802.1AB-2016	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	145.5.1	Support the Power via MDI Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	145.5.1	Meet state diagrams defined in 145.5.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	PSE LLDPDU	145.5.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enable	DLLC:M	Yes [ ] N/A [ ]
DLL6	PD Data Link Layer classification ready	145.5.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enable	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD requested power value change	145.5.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL8	PSE allocated power value change	145.5.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–39, Figure 145–40, Figure 145–43, and Figure 145–44	DLLC:M	Yes [ ] N/A [ ]
DLL10	Single-signature PD power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–41 and Figure 145–42	DLLC*PDSS:M	Yes [ ] N/A [ ]
DLL11	Dual-signature PD power control state diagrams	145.5.3	Meet the behavior shown in Figure 145–45 and Figure 145–46	DLLC*PDDS:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
DLL12	PSEAllocatedPowerValue, PSEAllocatedPowerValue_alt(A), and PSEAllocatedPowerValue_alt(B)	145.5.4	Range defined in Table 145–41	DLLC*PSE:M	Yes [ ] N/A [ ]
DLL13	PDRequestedPowerValue, PDRequestedPowerValue_alt(A), and PDRequestedPowerValue_alt(B)	145.5.4	Range defined in Table 145–42	DLLC*PSE:M	Yes [ ] N/A [ ]
DLL14	Transition from 4-pair to 2-pair operation for PSEs connected to dual-signature PDs	145.5.6	Assign value of PSEAllocatedPowerValue_alt(X), to PSEAllocatedPowerValue	DLLC*PS4P:M	Yes [ ] N/A [ ]
DLL15	Transition from 2-pair to 4-pair operation for PSEs connected to dual-signature PDs	145.5.6	Assign value of PSEAllocatedPowerValue, to PSEAllocatedPowerValue_alt(X)	DLLC*PS4P:M	Yes [ ] N/A [ ]
DLL16	PSE receives request for Autoclass when Autoclass is enabled	145.5.7	Measure the power consumption per the requirements in 145.2.7.2	DLLC*PSE:M	Yes [ ] N/A [ ]

145.7.3.7 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	145.6.1	Conforms to IEC 60950-1 or IEC 62368-1	M	Yes [ ]
ES2	Safety	145.6.1	Comply with all applicable local and national codes	M	Yes [ ]
ES3	Telephony voltages	145.6.5	Application thereof described in 145.6.5 not to result in any safety hazard nor preclude conformance with 145.6.1 and 145.6.2	M	Yes [ ]
ES4	Limitation of electromagnetic interference	145.6.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

145.7.3.8 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	145.6.1	Limited Power Source in accordance with IEC 60950-1 or IEC 62368-1 Annex Q	M	Yes [ ]