Power Matters

Microsemi

IEEE802.3bt 4-Pair Power over Ethernet Task Force

PSE Vdiff proposal

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Rev 004

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Objectives

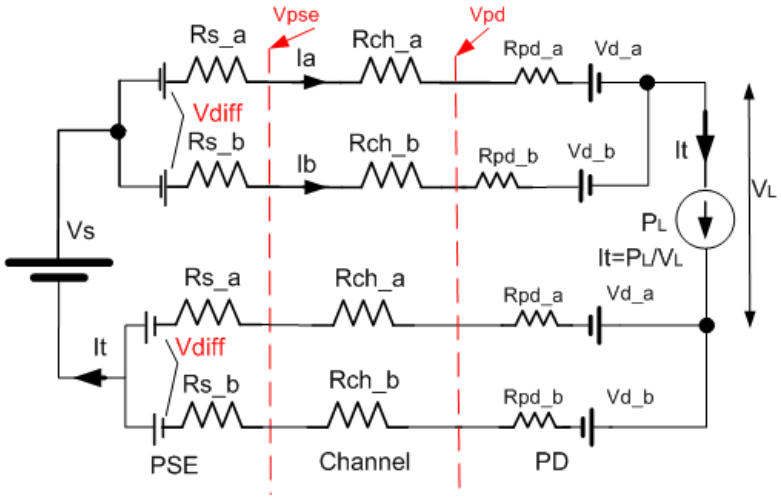
- To propose value to PSE Vdiff in IEEE802.3BT D0.2 draft:
  - See details at: http://www.ieee802.org/3/bt/public/nov14/darshan_04_1114r002.pdf

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1.1	Output voltage pair to pair difference of pairs with the same polarity in the POWER_ON state	VPort_PSE_diff	mV		TBD	3,4	Open load voltage. Test setup: TBD.

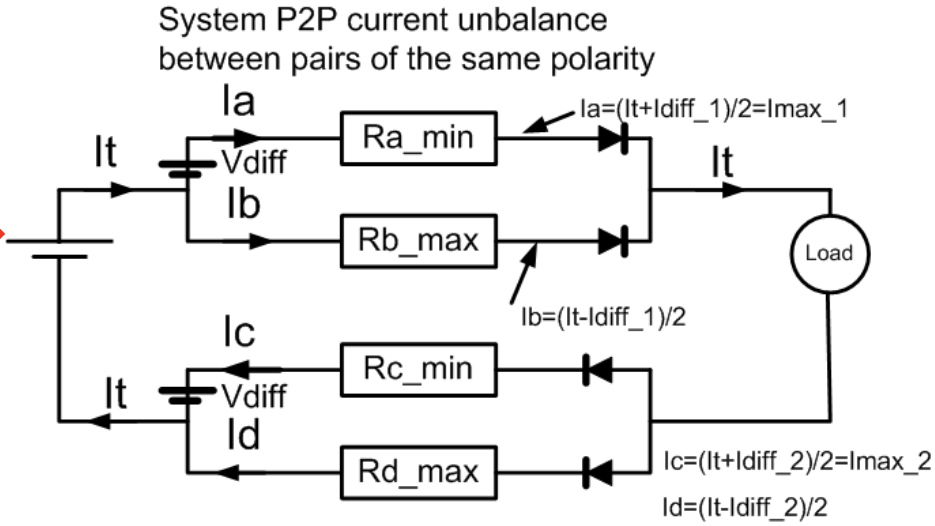
- Theoretical calculations of maximum Vdiff based on PSE PI possible maximum components resistance
  - How to address internal leakage current from positive to negative rails
- PSE Vendor Vdiff survey
- Proposal for PSE Vdiff and test conditions.
  - Background: PSE Vdiff affect system end to end unbalance. Once it is defined (and also PD Vdiff) we can calculate final system end to end channel pair to pair resistance/current unbalance based on table G1 in the adhoc material slides.
  - Then we can specify PSE and PD PI unbalance values
  - As a result, maximum pair current under unbalance conditions can be calculated.

Terms

- PSE PI pair to pair voltage difference. The voltage difference between pairs of the same polarity.
  - Pair to pair voltage difference is a major contributor for overall system unbalance especially at short channel length.
  - We have PSE Vdiff and PD Diode Vdiff. System wise the total of PSE Vdiff and PD Vdiff=Vdiff is affecting P2P_Iunb.
  - The focus of this presentation is on PSE Vdiff.



Simplified



- PD diode voltage Vd_a, Vd_b.
- PSE P2P voltage differences is described by Vdiff.

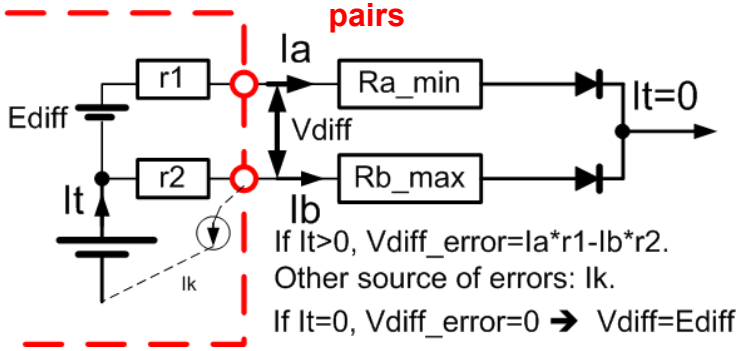
Ra,Rb, Rc and Rd are the end to end resistance

Theoretical calculations of maximum Vdiff

- Possible Maximum Min/Max values of system components.
  - For Minimum min/max values see Adhoc table G1.

Component	Min[Ω]	Max[Ω]	Rdiff[Ω]
Rsense	0.5*0.98	0.5	0.01
RDSON	0.5*0.7	0.5	0.15
Connector	0.03	0.05	0.02
Transformers	0.277	0.3	0.023

Same applies to negative pairs

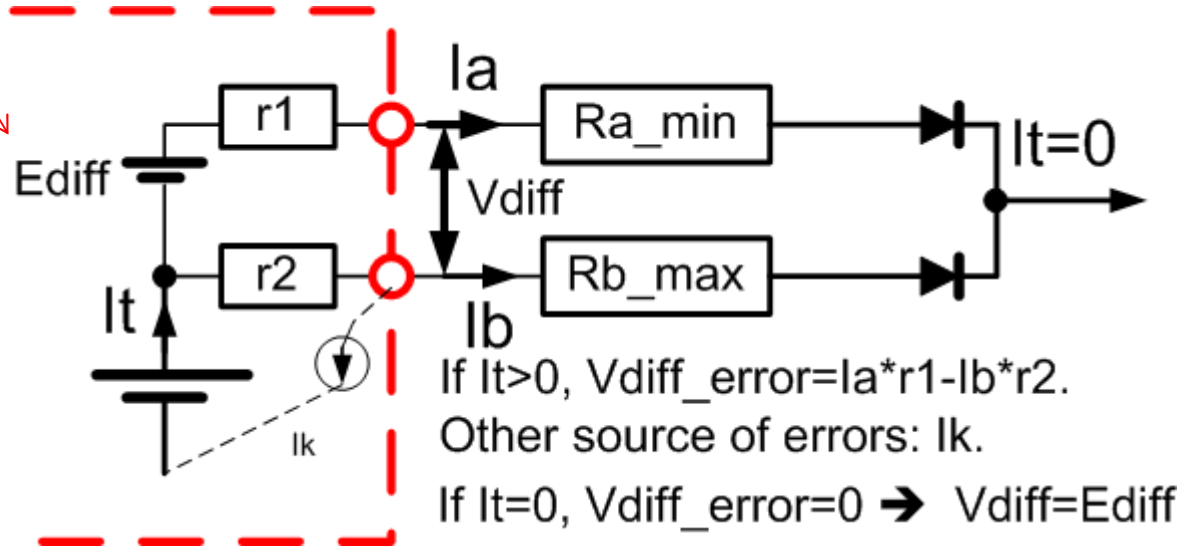


Component	Value	Units
Total Rdiff [Ω]	0.203	Ω
Possible positive to negative system **INTERNAL** Idiff[1]	1	mA
Maximum Vdiff=Idiff*Rdiff at NO external load.	**0.203**	**mV**
Adding margin ➔ Total :	1	mV
Unknowns (Results from only 4 vendors that <=2mV is OK)	1	mV
Proposal (subject to reduce to 1mV pending final survey results)	**2**	**mV**

1. PSE internal circuitry that may have current draw from positive PI wires to negative PI wires e.g. protection circuitry or other.

Proposal

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1.1	Output voltage pair to pair difference of pairs with the same polarity in the POWER_ON state	VPort_PSE_diff	mV		2	3,4	Open load voltage. Test setup: See slide 9.



Example.
Same applies to negative pairs.

Thank You

Motion

- Move to accept VPort_PSE_diff_max value per the table in slide 5 of darshan_03_0115.pdf.

- Mover: Yair Darshan
- Seconder: Dave Dwelley

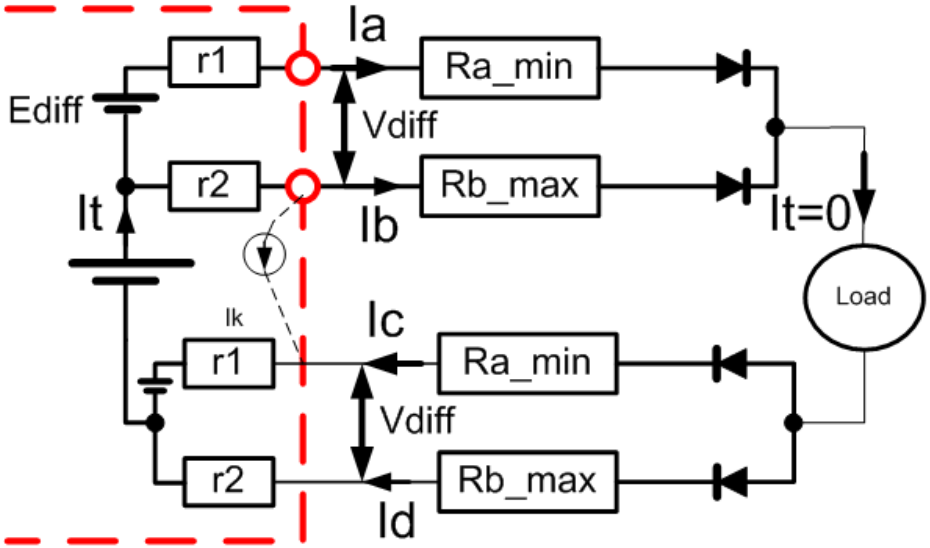
- Y: N: A:

Backup Slides

Annex A: Why Vdiff is best to be specified at No load?

- Ediff is the source for additional unbalance and not Vdiff.
- We have access only to Vdiff for measuring it.
- Only at no load, Ediff=Vdiff
  - With load, Vdiff will include error and can't be used.
    - **We need the Thevenin Vdiff equivalent.**

- Since the PSE chip and the system may have internal circuitry that draws current across the port, Vdiff can not be zero when measured for compliance, hence a minimum value need to be specified + design margin that will generate the maximum value.



If It>0, Vdiff_error=Ia*r1-Ib*r2. Other source of errors: Ik.
If It=0 and Ik=0: Vdiff_error=0 ➔ Vdiff=Ediff
If It=0, Ik>0: Vdiff_error(Ik)=Vdiff_min=I(r1)*r1-I(r2)*r2=0-Ik*r2 (example)

It =0 is achieved by the following system setup:

1. Use PSE FORCE_POWER to allow POWER_ON without a load.
2. Use MPS modulation at test at zero current.

Annex B: Why specifying Vdiff in positive pairs and negative pairs and not only on the pairs where current is measured?

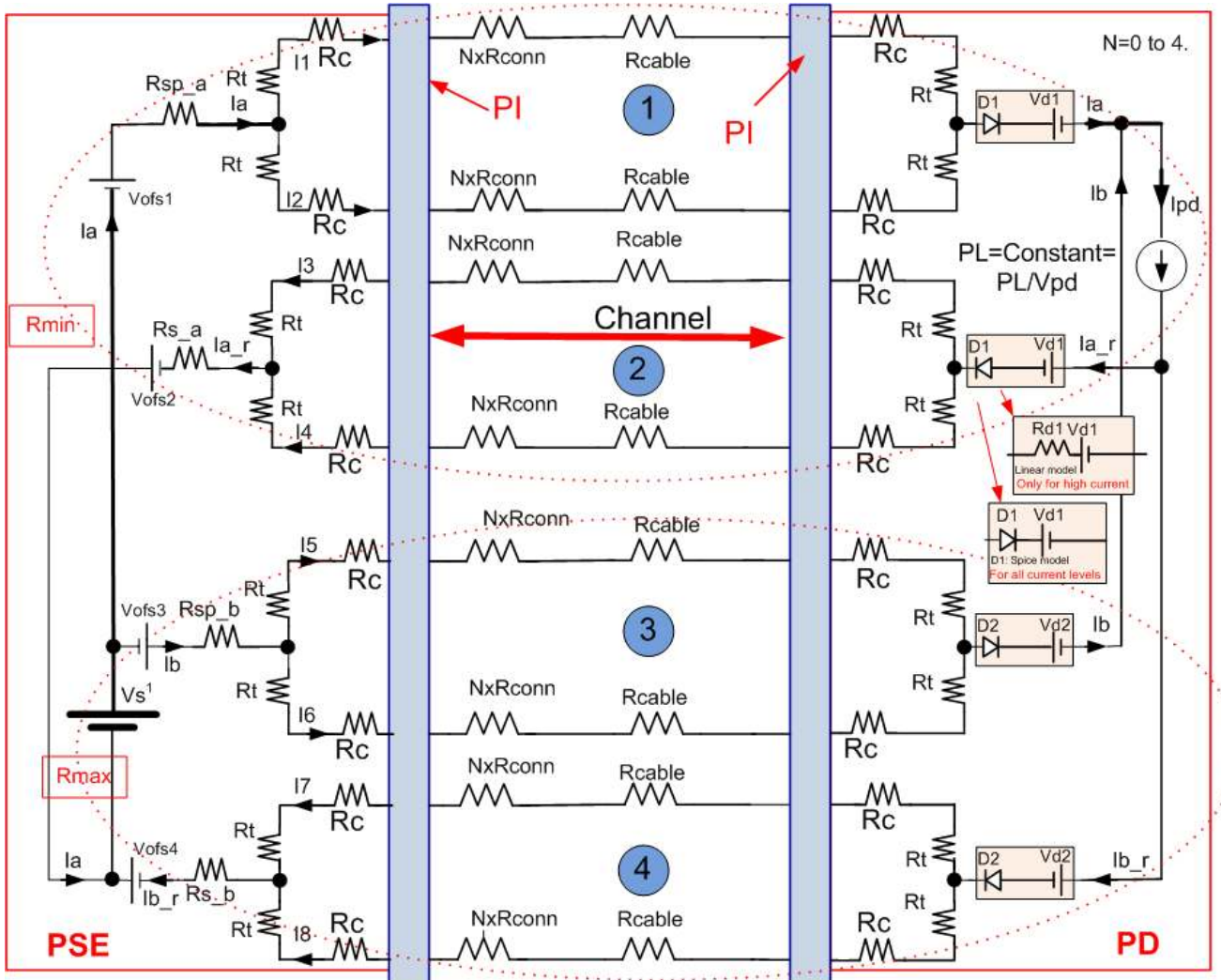
- Vdiff affects unbalance at low current at short and long cables.
- Vdiff affects unbalance at high current at short cables.
- Transformers are affected by Unbalance.
  - Transformers are located in all pairs.
- Therefor Vdiff need to be specified for all pairs of the same polarity.

Annex G1: Existing adhoc worst case data base

#	Parameter	Data set 1	Data set 2
1	Cordage resistivity[1]	0.14Ω/m	
		0.09262Ω/m for AWG#24 for worst case analysis	
2	Horizontal cable resistivity option 1[2]	11.7Ω/100m=(12.5Ω - 4*0.2Ω) / 100m which is the maximum resistance when tested with maximum Iport.	7.4Ω/100m (CAT6A, AWG23) This is to give us maximum P2PRunb
3	option 2[3]	0.098Ω/m. Maximum value per TIA etc. Can't be used for worst case analysis.	
4	Unbalance parameters	• Cable Pair resistance unbalance: 2%. Channel pair resistance unbalance: 3% • Cable P2P Resistance Unbalance: 5%. • Channel P2P Resistance Unbalance: 0.1Ω/7.5% max which ever is greater	
5	Channel use cases to check. See figure 1 for what is a channel.	A. 6 inch (0.15 m) of cordage, no connectors. B. 4 m channel with 1 m of cordage, 3 m of cable, 2 connectors C. 23 m channel with 8 m of cordage, 15 m of cable, 4 connectors D. 100m channel with 10 m of cordage, 90 m of cable, 4 connectors	
6	End to End Channel[6]	The Channel per figure 1 + the PSE and PD PIs.	
7	Transformer winding resistance	120mOhm min, 130mOhm max	
8	Connector resistance[8]	40mOhm min, 60mOhm max	30mOhm min, 50mOhm max
9	Diode bridge[9] (Discreet Diodes)	0.39V+0.25Ω*Id min; 0.53V+0.25Ω*id max. (TBD)	
10	PSE output resistance [10]	Rsense 0.25 RDSON_min=0.1 Ω RDSON_min=0.7*RDSON_max	Rsense 0.25 RDSON_min=0.05 Ω RDSON_min=0.7*RDSON_max

Annex F – System Model including PSE /PD Components

December 2014. Diode possible models details shown by splitting the general model to two models. No technical change from previous update. See note 5.



1. A single Vs was not meant to imply specific implementations and is drawn as single voltage source for simplification of the drawing. The important parameter is the pair to pair voltage difference.

Source: Yair Darshan and Christian Beia

- Notes for the general Model:

1. Total end to end channel connectors is 6 max. The formal channel is with up to 4 connectors.
2. Number of connectors can varies between 0 to 4 . See Annex G1
3. In simulations, pairs 1 and 2 components were set to minimum resistance and pairs 3 and 4 were set to maximum resistance values.
4. Vofs1/2/3 and 4 was added. Per adhoc consensus to generate PSE Vdiff (July 3,2014).
5. For low and high currents use diode in the model. Linear diode model (resistor and voltage source) can be used only for high currents. **See Adhoc slides Annex F1 for details.**

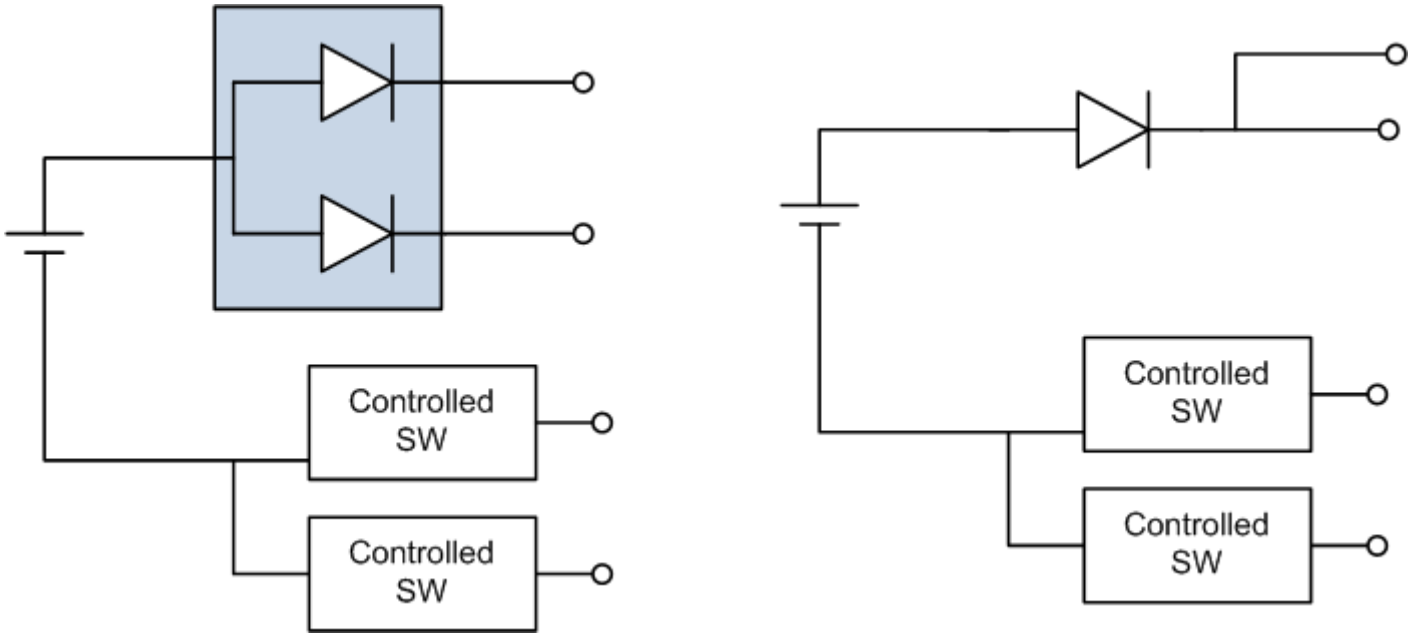
Annex G2: Worst case data base- Notes. -2

1	Per standard. It is maximum value for solid and stranded wire. The maximum value is close to AWG#26 wire resistance/meter including twist rate effects. **See annex E1.** Due to the fact that patch cords may use AWG#24 cables with stranded (for mechanical flexibility) or solid wire (for improved performance), we will use the AWG#24A for worst case analysis as well. Cordage with AWG#24 wire has 0.0842Ω/m for solid wire and with 10% twist rate it will be 0.09262 Ω/m.
2	We need both data sets (data set 1 and data set 2) to find where is the worst condition for maximum current unbalance. **See Annex B curve and data** showing that at short channel we get maximum P2PRUNB but it may has less concern to us since the current is lower. We need to do all use cases calculation to see where is the maximum current over the pair; at short channel or long channel. The CAT6A cable with AWG#23 has 0.066 Ω/m. Including 12% increase on cable length due to twist rate, the effective cable resistance per meter will be 1.12*6.6 Ω/100m= 0.074 Ω/m. (with 20% twist rate it will be 0.0792 Ω/m)
3	Standard definition per Annex E1 for maximum resistance. We will check how results will be differ when AWG#23 is used for worst case results (lower resistance than standard definition for horizontal cable which is a maximum value.
4	
5	
6	PSE PI and PD PI includes: connector, transformer, resistors. PD PI includes diode bridge.
7	
8	Connector resistance was changed since the difference (60-30) milliohm is not representing Rdiff, it is representing maximum and minimum results of connector resistance of different connectors. To correct it, we change the numbers according to inputs from connector vendors and measured data. See Annex E1-E6 for confirmation.
9	Vf and Rd are worst case numbers of discrete diode which there is no control on Vf and Rd. It needs more investigation to verify that we are not over specify. (Christian is checking it). Normally match components (e.g. matched two diode bridges) are used for 4P operation. Any how ,PD PI spec. will eventually set the requirement.
10	PSE output resistance e.g. Rs_a/b=Rsense+Rdson in addition to winding resistance. See model I Annex F for reference.

Adhoc response, June 24, 2014. Adhoc accept this table

Source: Yair Darshan and Christian Beia

PSE Vdiff with non-linear elements



- Vdiff is reduced by using single common diode or two matched diodes