

### 33.3.3.11 Type 3 and Type 4 dual-signature constants

$V_{\text{Reset}}$	Reset voltage per pairset (see Table 33–29)	1
$V_{\text{Reset\_th}}$	Reset voltage threshold per pairset (see Table 33–29)	2
$V_{\text{Mark\_th}}$	Mark event voltage threshold per pairset (see Table 33–29)	3
pd_req_class_mode(M)	A constant indicating the requested Class of the PD over Mode M	4
	Values:	5
	1: The PD requests Class 1.	6
	2: The PD requests Class 2.	7
	3: The PD requests Class 3.	8
	4: The PD requests Class 4.	9
	5: The PD requests Class 5.	10

### 33.3.3.12 Type 3 and Type 4 dual-signature variables

mdi_power_required_mode(M)	A control variable indicating that over Mode M, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.	11
	Values:	12
	FALSE:PD functionality is disabled.	13
	TRUE:PD functionality is enabled.	14
pd_dll_enabled	A variable indicating whether the Data Link Layer classification mechanism is enabled.	15
	Values:	16
	FALSE:Data Link Layer classification is not enabled.	17
	TRUE:Data Link Layer classification is enabled.	18
pd_max_power_mode(M)	A control variable indicating the max power that the PD may draw from the PSE over Mode M. See power classifications in Table 33–31.	19
	Values:	20
	0: PD may draw Class 0 power	21
	1: PD may draw Class 1 power	22
	2: PD may draw Class 2 power	23
	3: PD may draw Class 3 power	24
	4: PD may draw Class 4 power	25
	5: PD may draw Class 5 power	26
pd_reset_mode(M)	An implementation-specific control variable that unconditionally resets the PD state diagram over Mode M to the OFFLINE state.	27
	Values:	28
	FALSE:The device has not been reset (default).	29
	TRUE:The device has been reset.	30
pd_undefined_mode(M)	A control variable that indicates that the PD is in an undefined condition over Mode M. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_mode(M) variable.	31

Values:	1
FALSE:The PD is in a defined condition (default).	2
TRUE:The PD is an undefined condition.	3
power_received_mode(M)	4
An indication from the circuitry that power is present on the PD’s PI over Mode M.	5
Values:	6
FALSE:The input voltage does not meet the requirements of $V_{Port\_PD-2P}$ in Table 33–31.	7
TRUE:The input voltage meets the requirements of $V_{Port\_PD-2P}$ .	8
present_class_sig_A_mode(M)	9
Controls presenting the classification signature that is used during first two class events (see 33.3.6) by the PD over Mode M.	10
Values:	11
FALSE:The PD classification signature is not to be applied to the link.	12
TRUE:The PD classification signature is to be applied to the link.	13
present_class_sig_B_mode(M)	14
Controls presenting the classification signature that is used during the third class event and all subsequent class events (see 33.3.6) by the PD over Mode M.	15
Values:	16
FALSE:The PD classification signature is not to be applied to the link.	17
TRUE:The PD classification signature is to be applied to the link.	18
present_det_sig_mode(M)	19
Controls presenting the detection signature (see 33.3.4) by the PD over Mode M.	20
Values:	21
invalid:A non-valid PD detection signature is to be applied to the link over Mode M.	22
valid:A valid PD detection signature is to be applied to the link over Mode M.	23
either: Either a valid or non-valid PD detection signature may be applied to the link.	24
present_mark_sig_mode(M)	25
Controls presenting the mark event current and impedance (see 33.3.6.2.1) by the PD over Mode M.	26
Values:	27
FALSE:The PD does not present mark event behavior.	28
TRUE:The PD does present mark event behavior.	29
present_mps_mode(M)	30
Controls applying MPS (see 33.3.8.10) to the PD’s PI over Mode M.	31
Values:	32
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD’s PI.	33
TRUE:The MPS is to be applied to the PD’s PI.	34
pse_dll_power_level_mode(M)	35
A control variable output by the PD power control state diagram (Figure 33–49) that indicates the power level of the PSE by which the PD is being powered over Mode M.	36
Values:	37
1: The PSE has allocated Class 3 power or less (default).	38
2: The PSE has allocated Class 4 power.	39
3: The PSE has allocated Class 5 power.	40
pse_dll_power_type	41
A control variable output by the PD power control state diagram (Figure 33–49) that indicates the PSE Type connected to Mode M as 1 or 2, see 79.3.2.4.1.	42
pse_power_level_mode(M)	43
A control variable that indicates to the PD the level of power the PSE is supplying over Mode M.	44
Values:	45
3: The PSE has allocated the PD’s requested power or Class 3 power, whichever is less.	46
4: The PSE has allocated the PD’s requested power or Class 4 power, whichever is less.	47
5: The PSE has allocated the PD’s requested power or Class 5 power, whichever is less.	48
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$V_{PD\_mode}(M)$

The voltage at the PD PI measured between any positive conductor and any negative conductor of the Mode M pairs; see 33.1.4.

### 33.3.3.13 Type 3 and Type 4 dual-signature timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x\_timer” is asserted.

$tpowerdly\_timer\_mode(M)$

A timer used to prevent Class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over Mode M and Class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over Mode M during the PSE’s inrush period; see  $T_{delay-2P}$  in Table 33–31.

### 33.3.3.14 Type 3 and Type 4 dual-signature functions

$do\_class\_timing\_mode(M)$

This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over Mode M. The class event timing requirements are defined in Table 33–29. This function returns the following variable:

$short\_mps\_mode(M)$ : A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.9) the PD should use.

Values:            TRUE: The PSE uses Type 3, 4 MPS requirements.  
                      FALSE: The PSE uses Type 1, 2 MPS requirements.

### 33.3.3.15 Mode designation

PD Modes are referred to by the letter ‘A’ or ‘B’ for Mode A and Mode B respectively. Mode information is obtained by replacing the M in the desired variable or function with the letter of the Mode of interest. Modes are referred to in general as follows:

M

Generic Mode designator. When M is used in a state diagram, its value is local to that state diagram and not global to the set of state diagrams.

33.3.3.16 Type 3 and Type 4 dual-signature PD state diagrams

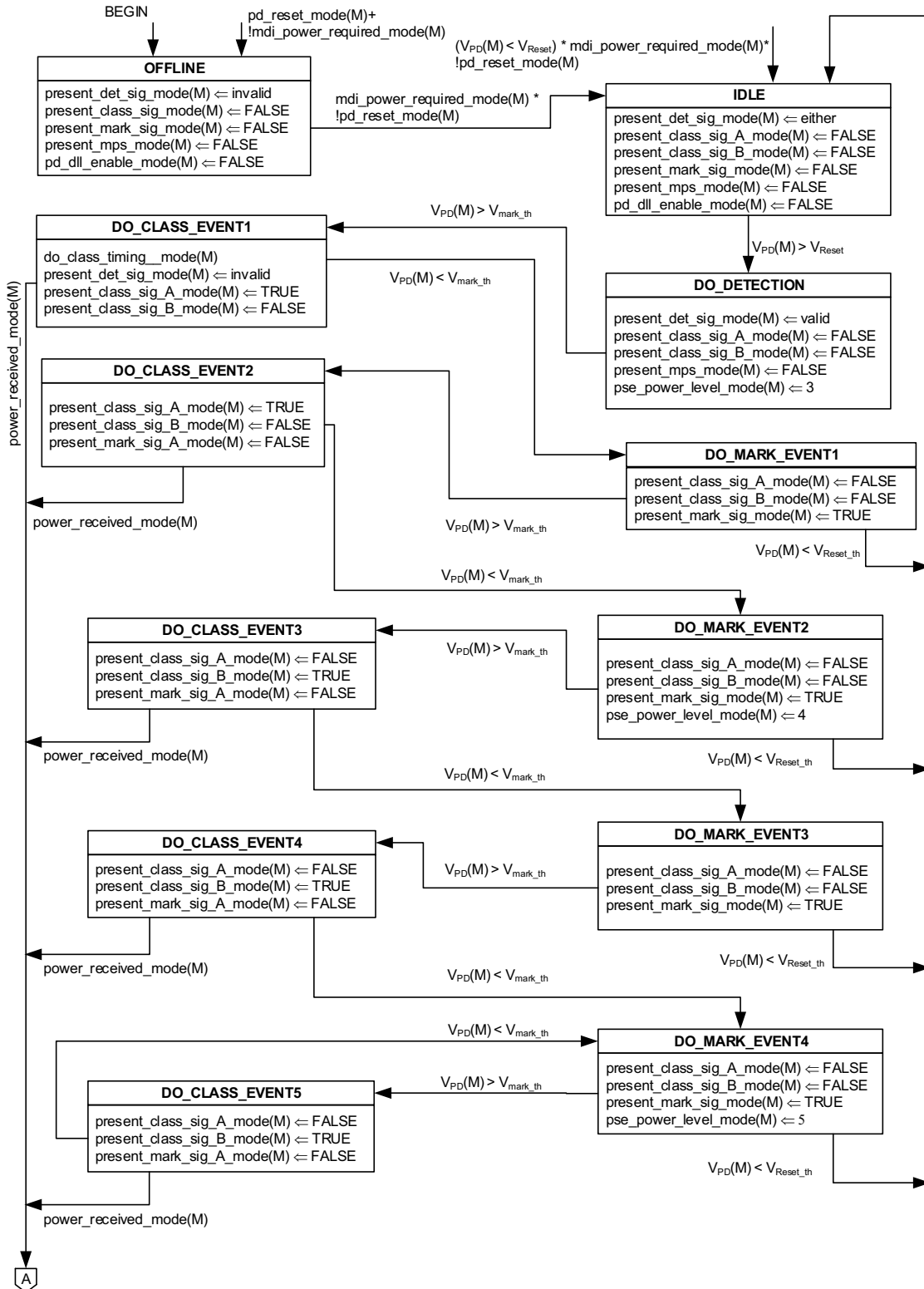


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram

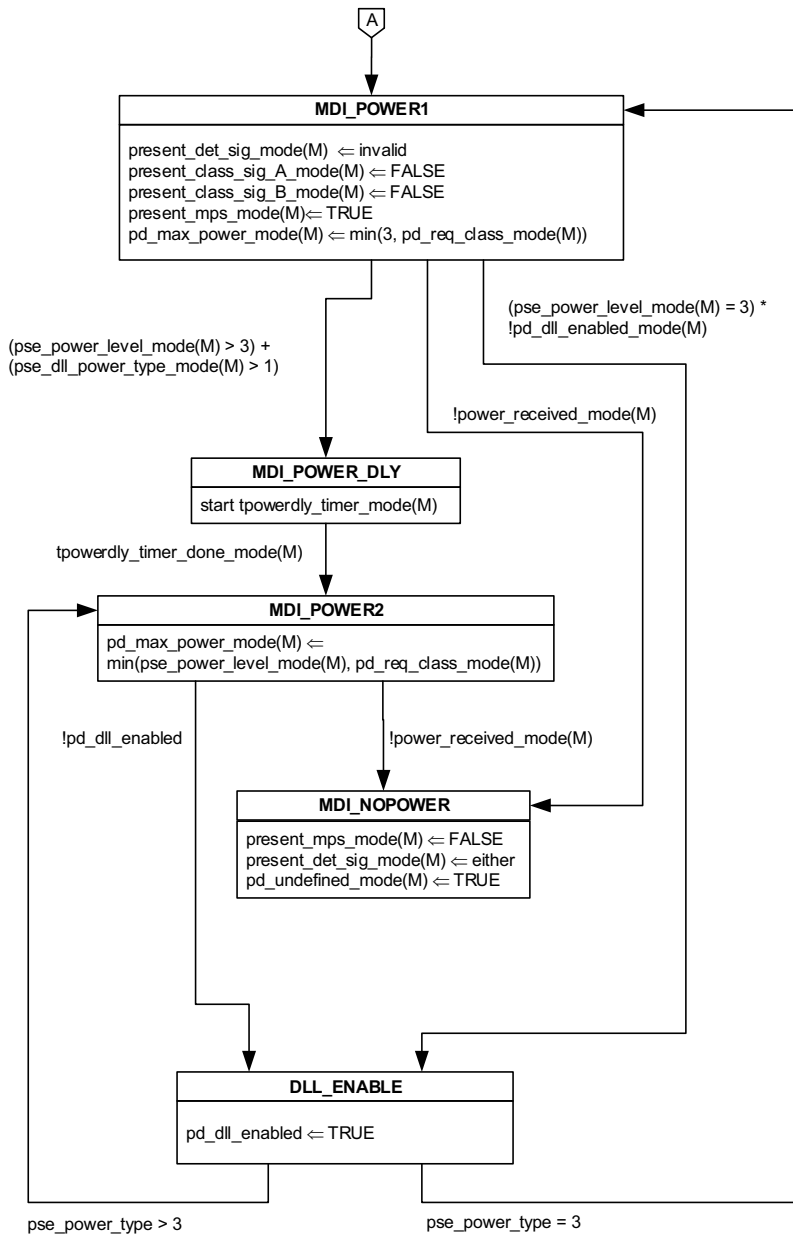


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram (continued)

### 33.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature when it is in a detection state per Figure 33–31, Figure 33–32, Figure 33–33, and Figure 33–34. See 33.3.5.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–31, Figure 33–32, Figure 33–33, and Figure 33–34.