Comment #44 (Clause 145.2.5.7)

TDL #253 D2.3 PSE Class SD for dual-signature PDs is inconsistent with recent developments in single-signature Class SD. Particularly, state CLASS_4PID4 is inconsistent with the notion that pd_req_pwr and therefore pd_cls_4pid are known after 3 (not 4) class events. Also, the "pse_allocated_pwr" paradigm is not implemented for PSE dual-signature Class SD.

TDL (Yair):

Item 1: Implement pse_allocated_pwr scheme from single-signature PSE Class SD into dual-signature PSE Class SD.

Item 2: Modify pd_cls_4pid logic such that pd_cls_4pid_* are determined out of CLASS_EV3_* states."

Discussion regarding Item 1:

Yair Darshan: Regarding Item 1: I do not see a reason to sync the concept of dual-signature state diagram with that of the single-signature. If the dual-signature sate diagram works it doesn't matter how it is implemented. The main differences start with the definition of the DO_CLASSIFICATION function.

Lennart: Same as Yair.

Jean Pickard: unless we think it's important to indicate the allocated power in the state diagram. If such change is to be done, it should be done with minimal impact on SD complexity

Discussion regarding Item 2:

Yair: I agree that state CLASS_4PID4 is inconsistent with the notion that pd_req_pwr and therefore pd_cls_4pid are known after 3 (not 4) class events. As a result, we need to move CLASS_4PID4 before MARK_EV3. Looking at the single-signature PSE Classification state diagram, PSE knows "pd_req_pwr" by CLASS_EV3, although PSE must issue 4 or 5 events to allocate this to the PD. For dual-signature, the PSE knows "pd_req_pwr" and "pd_cls_4pid_xxx" after CLASS_EV3 but PSE state diagram does not let us assign these values at that time.

Jean P.: That statement is not accurate, the 4PID block is in fact located at 2 locations, always the last block just before reaching the last Mark state (after 3 or 4 events). Why the second 4PID block after 4 events? If the 4th class is different than the 3rd, the 4PID is not set. I don't see anything to change here, really.

Yair Darshan: Jean argument make sense. 4PID states (4PID3 and 4PID4) are used in two places.

The 1st location is after doing 3 class event when (pese-avail_pwr_pri>=4) and class-sig ≠4 which ends with MARK_EV_LAST_PRI or (pese-avail_pwr_pri<4) and class-sig =4 which needs to end with CLASS_RESET_PRI and CLASS_EV1_LCE-4PID_PRI and then MARK_EV_LAST_PRI.

The 2nd location is after doing 4 class event which end with MARK_EV_LAST_PRI.

So, it is more reliable 4PID4_PRI determination to be set after CLASS_EV4_PRI when there is a chance to get false class-sig reading that is not equal to the response to CLASS_EV3_PRI.

Proposed Remedy:

Group to discuss. Meanwhile, no changes required to the spec.