# MPS Unbalance v141

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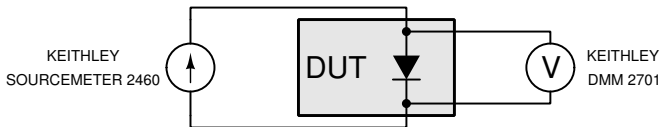
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# Overview

- ► Explore effect of diode forward voltage unbalance at low currents
- ► Temperature effect on diodes
- ► End to end MPS current unbalance
- ► Consequences for MPS design
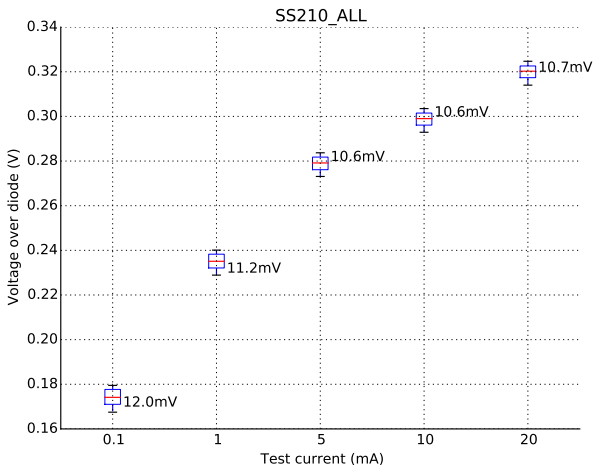- ► Proposal for MPS requirements

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## Measurement method

This presentation will explore measured difference in diode voltage over a number of different diodes at low current.

- ▶ Test currents: 100 µA, 1 mA, 5 mA, 10 mA, 20 mA
- ▶ Diodes: MBRM1H100, MBRM2H100, MBRS2H100, MBRS1100, MBRS1100T, MURS110, MURS210, NTSS2100ET1, NTSS2100T1, SS210, VSSA210E361T
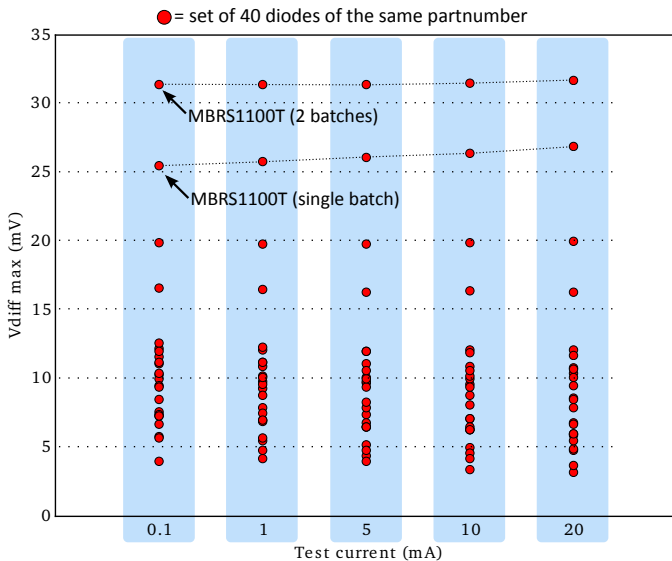- ▶ DUT at stable room temperature
- ▶ Total 720 measured diodes



KEITHLEY SOURCEMETER 2460    DUT    KEITHLEY DMM 2701

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# Example results



SS210_ALL

Voltage over diode (V)

- 10.7mV (at 20 mA, ~0.32 V)
- 10.6mV (at 10 mA, ~0.30 V)
- 10.6mV (at 5 mA, ~0.28 V)
- 11.2mV (at 1 mA, ~0.235 V)
- 12.0mV (at 0.1 mA, ~0.175 V)

Test current (mA)

Vdiff = highest measured $V_D$ - lowest measured $V_D$ at test current.

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# Vdiff overview

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# Conclusion Vdiff measurement

- Results match with ⇒darshan_02_0115.pdf
- In the current range 100 µA to 20 mA the diode voltage <u>difference</u> remains constant, but <u>absolute</u> diode voltage goes up with current
- Of all measured diodes, the maximum sample to sample difference (for the same partnumber) is 32 mV
- Comparing a batch of diodes, purchased from 1 reel, to a combination of two batches (different time, different reel) increases the maximum diode voltage different by 6 mV
- Silicon or Schottky diodes exhibit the same amount of maximum voltage difference

- … however, this is all measured at a stable constant temperature.

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# End to end MPS unbalance
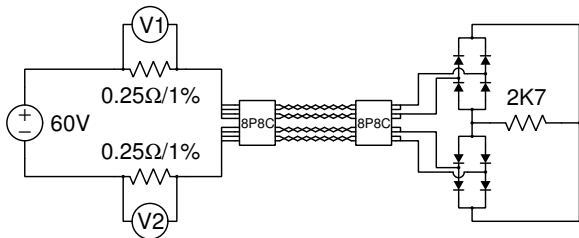


- ► Measured pair-set current over 0.25 Ω precision resistor (resistors matched better than 1%).
- ► Tested with various cable lengths (1 m, 10 m)
- ► Diode: MBRS1100T & SS210
- ► Test to fail: introduce temperature difference → can we fail MPS ?

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# Measurement results 1

- $I_{Port}$: 22 mA
- 10 meter CAT5e
- Diode: MBRS1100T
- Vdiff(max): 34 mV
- Applied 25 °C difference between diode bridges (43 °C / 68 °C)
- Current unbalance 5% → 45%



MBRS1100T, CAT5e, 10 meter, Tdiff 25C

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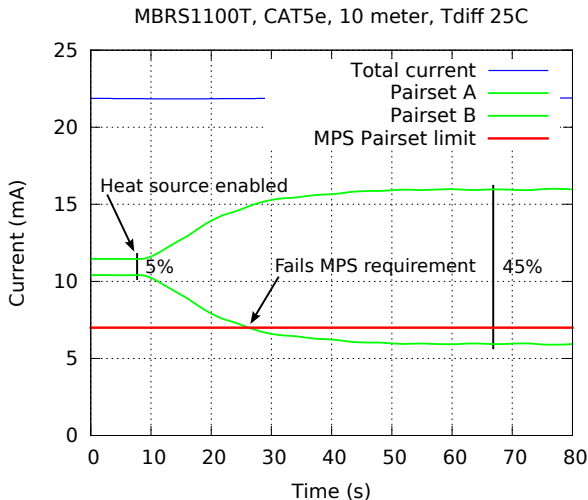
# Measurement results 2

- $I_{Port}$: 22 mA
- 10 meter CAT5e
- Diode: SS210
- Vdiff(max): 10 mV
- Applied 20 °C difference between diode bridges (40 °C / 60 °C)
- Current unbalance -2% → 28%



SS210, CAT5e, 10 meter, Tdiff 20C

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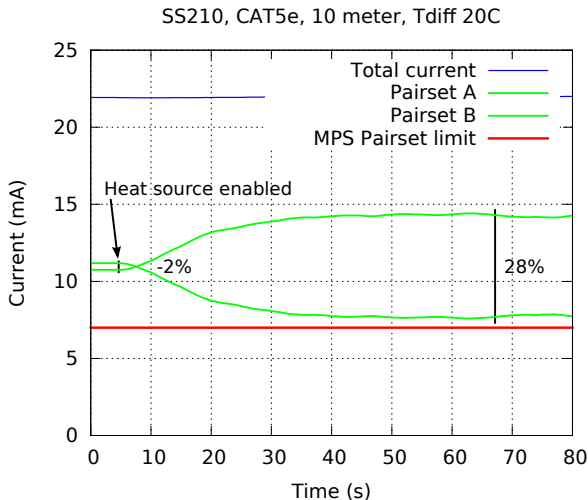
# Conclusion system measurements

System end to end low current unbalance measurements show:

- ► Initial (room-temperature) low current unbalance looks good
- ► Temperature difference between diodes creates large unbalance
- ► Temperature effect is potentially far greater than intrinsic Vdiff. Temperature coefficient $-2.0\,\text{mV/°C}$
- ► Maximum Vdiff is not a typically specified parameter in datasheets
- ► Other effects, like aging, are hard to predict

PDs will need a carefully designed input stage to control unbalance if a low power mode is needed. Use of diode rectifiers is probably not recommended if the PD must ensure a per pairset MPS.

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# MPS proposal

$I_{Hold\,2P}$      Current the PSE must see on powered pairset(s) to consider MPS OK.
$I_{Hold\,4P}$      Total current the PSE must see on both pairsets to consider MPS OK.
MPS both      PSE requires MPS to be met on both pairsets.
Sum/Max      Allowed MPS methods: sum-pairset and max-pairset
$I_{Port\_MPS\,/2P}$      Minimum current the PD must guarantee per powered pairset
$I_{Port\_MPS}$      Minimum total current the PD must guarantee
Timing      PSE or PD should follow the 'old' or 'new' timing

| PSE | PD | PSE Requirements | | | | PD Requirements | | |
|---|---|---|---|---|---|---|---|---|
| | | $I_{Hold\,2P}$ | $I_{Hold\,4P}$ | Timing | Sum/Max | $I_{Port\_MPS\,/2P}$ | $I_{Port\_MPS}$ | Timing |
| Type 1,2 | Type 1,2 | 5-10 mA | - | Old | - | - | 10 mA | Old |
| | Type 3,4 Class $\leq$ 4 | 5-10 mA | - | Old | - | - | 10 mA | Old |
| | Type 3,4 Class $\geq$ 5 | 5-10 mA | - | Old | - | - | 10 mA | Old |
| | Type 3,4 2-channel | 5-10 mA | - | Old | - | - | 10 mA | Old |
| Type 3,4 | Type 1,2 | - | 5-10 mA | New | Yes | - | 10 mA | Old |
| | Type 3,4 Class $\leq$ 4 | - | 5-10 mA | New | Yes | - | 22 mA | New |
| | Type 3,4 Class $\geq$ 5 | 2-7 mA | - | New | Yes | 7 mA | - | New |
| | Type 3,4 2-channel | 2-7 mA | - | New | No | 7 mA | - | New |

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# Type 3/4 PSE MPS Rules

- **PD Type 1, 2, 3, 4[$\leq$ Class 4]**
  - $I_{Hold}$ = 5-10 mA, total current (no balance requirement)
  - Support new MPS timings (6 ms / 354 ms)
  - MPS methods: per-pairset, sum-pairset, max-pairset

- **PD Type 3, 4 [$\geq$ Class 5]**
  - $I_{Hold}$ = 2-7 mA per pairset
  - Support new MPS timings (6 ms / 354 ms)
  - MPS methods: per-pairset, sum-pairset, max-pairset

- **PD Dual channel**
  - $I_{Hold}$ = 2-7 mA per pairset
  - Support new MPS timings (6 ms / 354 ms)
  - MPS methods: per-pairset, ~~sum-pairset, max-pairset~~

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# Type 3/4 PD MPS Rules

- **PSE Type 1, 2**
    - $I_{Port\_MPS}$ = 10 mA, total current (no balance requirement)
    - Legacy timing: 75 ms / 250 ms
- **PSE Type 3, 4 [$\leq$ 3 class events]**
    - $I_{Port\_MPS}$ = 22 mA, total current (no balance requirement)
    - New timing: 7 ms / 318 ms
- **PSE Type 3, 4 [$\geq$ 4 class events]**
    - $I_{Port\_MPS}$ = 7 mA, per pairset
    - New timing: 7 ms / 318 ms

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## Balanced flexibility

The MPS rules in the previous slide are a balance between PSE and PD flexibility and allow a further reduction in standby power.

- ► Legacy Type 1/2 PDs cannot have any requirement imposed for unbalance at MPS currents.
- ► Since a PSE cannot distinguish the Type of a PD in classes 0-4, we can apply the legacy MPS rules (amplitude & balance) also to Type 3 PDs of class 0-4, without causing (extra) complications for the PSE.
- ► Type 3/4 single channel PDs in Class 5 or higher must present $I_{Port\_MPS}$ on both pair-sets.
- ► Type 3/4 PSEs may also look at the sum of currents or the highest current of both pairsets to consider MPS satisfied.
- ► Dual channel PDs must present $I_{Port\_MPS}$ on both pairsets

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# Conclusion

- ► Measurements of 720 diodes, 11 types, reveal Vdiff(max) $< 35$ mV
- ► Parallel diodes cannot be expected to have reliable current sharing behaviour at MPS level currents
- ► PDs should be able to implement diode rectifiers and support low standby

- ► This MPS proposal offers balanced design flexibility for PSE and PD
- ► Diode bridges are possible for Class 4 and below
- ► PDs without low power modes are not impacted by this unbalance issue

Propose for .bt group to adopt MPS rules in this presentation.

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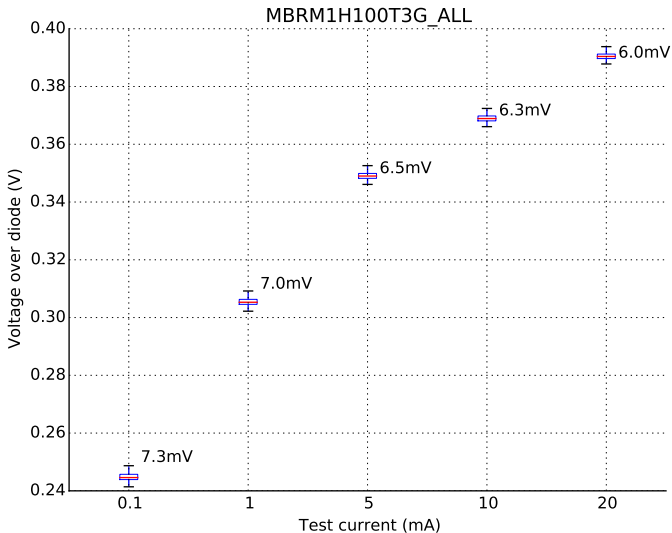# Diode equation

$$I = I_s \left( e^{\frac{qV}{nkT}} - 1 \right)$$

$$I_s = qA \frac{Dn_i^2}{LN_D} = qA \frac{D}{LN_D} BT^3 \exp\left( -\frac{E_{G0}}{kT} \right)$$

Silicon diode voltage shifts by about $-2.5$ mV/°C
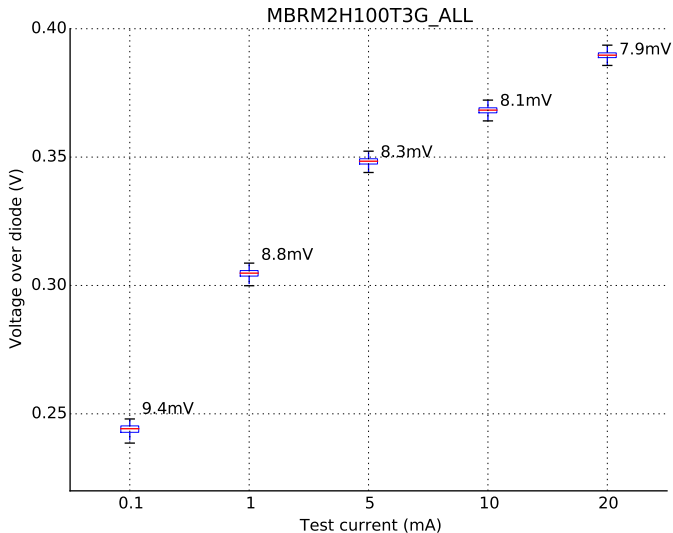Schottky diode voltage shifts by about $-2.0$ mV/°C

Reference: `http://www.pveducation.org/pvcdrom/solar-cell-operation/`
`effect-of-temperature`

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# Diode measurement results: MBRM1H100T3GALL



MBRM1H100T3G_ALL

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# Diode measurement results: MBRM2H100T3GALL

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# Diode measurement results: MBRS1100T3GALL



MBRS1100T3G_ALL

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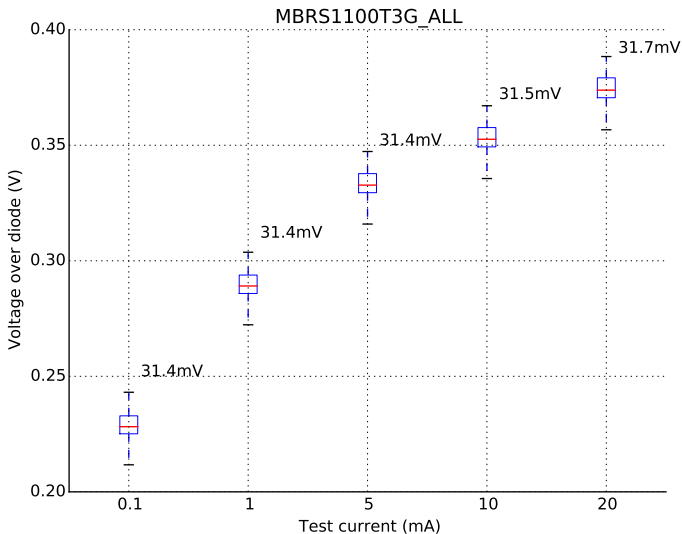
# Diode measurement results: MURS110T3GALL



MURS110T3G_ALL

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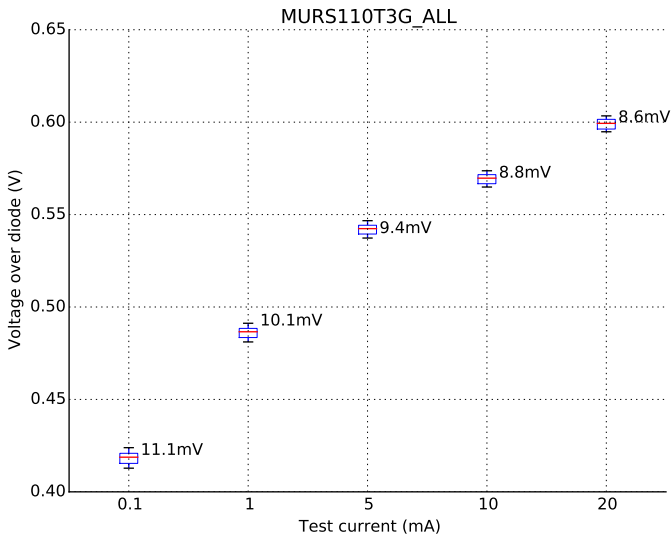
# Diode measurement results: MURS210T3GALL

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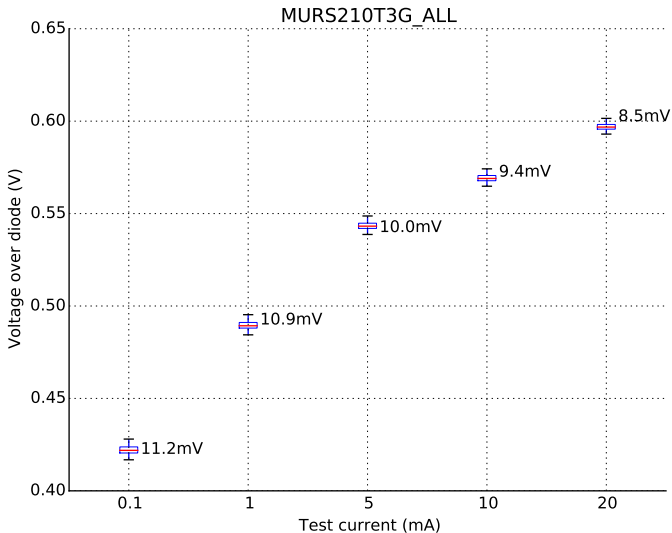
# Diode measurement results: SS210ALL

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