

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 33 SC 33.1.3 P 44 L 1 # 492
 Stover, David Linear Technology

Comment Type T Comment Status D Cabling

The text carefully distinguishes between DC loop resistance and DC pair loop resistance, stating this clause uses only DC pair loop resistance.

Furthermore the resistance is described as the path from the PSE PI to the PD PI. It is actually the round trip path.

Then the text refers to the wrong one...

"The cable references use "DC loop resistance," which refers to a single conductor. This clause uses "DC pair loop resistance," which refers to a pair of conductors in parallel. Therefore, RCh is related to, but not equivalent to, the "DC loop resistance" called out in the cable references.

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI. RChan-2P has a maximum value of RCh."

SuggestedRemedy

Change

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD. RChan has a maximum value of RCh/2 when operating in 4-pair mode. RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI. RChan-2P has a maximum value of RCh.

to

RChan is the actual DC loop pair resistance between the PI of the PSE and the PI of the PD and back to the PSE PI. RChan has a maximum value of RCh/2 when operating in 4-pair mode. RChan-2P is the actual DC loop pair resistance of a pairset from the viewpoint of the PSE PI and the PD PI. RChan-2P has a maximum value of RCh.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS LY

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD and back to the PSE PI. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI. Rchan-2P has a maximum value of RCh.

CI 33 SC 33.2.5.11 P 83 L 6 # 26
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PSE SD

Using One unique PD_4pair_cand variable can help simplify the state diagram, even if staggered detection is used for DS PD.

SuggestedRemedy

Replace "PD_4pair_cand_pri <= TRUE" with "PD_4pair_cand <= TRUE"
 Replace "PD_4pair_cand_pri <= FALSE" with "PD_4pair_cand <= FALSE"

Proposed Response Response Status W

TFTD CB

CI 33 SC 33.2.5.11 P 85 L 6 # 27
 Picard, Jean Texas Instruments

Comment Type TR Comment Status X PSE SD

Using One unique PD_4pair_cand variable can help simplify the state diagram, even if staggered detection is used for DS PD.

SuggestedRemedy

Replace "PD_4pair_cand_sec <= TRUE" with "PD_4pair_cand <= TRUE"
 Replace "PD_4pair_cand_sec <= FALSE" with "PD_4pair_cand <= FALSE"

Proposed Response Response Status W

TFTD CB

See 26

CI 33 SC 33.2.5.12 P 86 L 22 # 254
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan8

The PSE state machine part for single signature when it needs to know class code by issuing 3 finger and then doing class reset due to lake of sufficient power in which it need to generate only one finger etc. This is covered by the text but not in the state machine.

SuggestedRemedy

Add the missing state machine part in darshan_08_0916.pdf.

Proposed Response Response Status W

TFTD

WFP

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Cl 33 SC 33.2.6.7 P 94 L 28 # 290
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X 4PID

This section covers what establishes PD_4pair_cand. The state diagrams Figures 33-16, and 33-17 may do this as well, but they do not match. These diagrams do use the variable and xxx_pri and xxx_sec. The single-signature state diagram Figure 33-15 does not use PD_4pair_cand. Nothing in the state diagrams establishes pd_4pair_cand for certain.

SuggestedRemedy

See related comment marked COMMENT-3 for a solution.

Proposed Response Response Status W

TFTD CB

Need to align pd_4pair_cand with pd_4pair_cand_pri and _sec.

Cl 33 SC 33.2.7 P 96 L 43 # 407
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Yseboodt5

Unlike Type 2, Type 3 and Type 4 devices have a lot of parameters that are different depending on the Assigned Class.
 An initial assigned class is set up during Physical Layer classification.

Using DLL the PD and PSE are able to change the allocated power. It makes sense that the assigned Class 'follows' the PSEAllocatedPower variable.

SuggestedRemedy

Adopt yseboodt_05_0916_dllclasschange.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.2.7.2 P 98 L 29 # 40
 Wendt, Matthias Philips Lighting

Comment Type T Comment Status D Pres: Yseboodt7

If during autotest a PD changes its class signature to something other than '0' during TACS behavior is undefined as already pinpointed in yseboodt_03_0716_class.

It would be beneficial to define this for future use.

SuggestedRemedy

adopt yseboodt_03_0716_class

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS LY DS

Cl 33 SC 33.2.8 P 104 L 49 # 510
 Stover, David Linear Technology

Comment Type T Comment Status X Unbalance

Intra-pair current unbalance I_unb is specified as 3% I_Peak for Type 2, 3, and 4 PSEs. For higher Class PDs, this may preclude low-speed data implementations due to higher inductance requirements on those magnetics.

SuggestedRemedy

TFTD. Especially looking for opinions from magnetics vendors here.

Proposed Response Response Status W

TFTD

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Cl 33 SC 33.2.8.2 P 105 L 51 # 28
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PSE Power

To ensure acceptable steady-state operating conditions, we need to explain in which circumstances longer than 250us transients or significant voltage steps may be expected.

SuggestedRemedy

Add the following note at the end of 33.2.8.2.

"PSE should avoid causing such long duration (> 250us) transients or significant voltage steps with the exception of rare circumstances involving switchover of power supplies to ensure system robustness."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add the following note at the end of 33.2.8.2.

"PSE should avoid causing such long duration (> 250us) transients or significant voltage steps with the exception of rare circumstances such as those involving switchover of power supplies to ensure system robustness."

TFTD YD

Cl 33 SC 33.2.8.4 P 108 L 21 # 512
 Stover, David Linear Technology

Comment Type ER Comment Status D Editorial

"P_Peak_PD-2P is the total peak power... see Table 33-25". P_Peak_PD-2P is not defined anywhere (captured in another comment), but if it were, it would live in Table 33-28.

SuggestedRemedy

Correct reference to Table 33-28.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Adopt changes in darshan_16_0916.pdf

TFTD DS YD

Cl 33 SC 33.2.8.5 P 109 L 43 # 249
 Darshan, Yair Microsemi

Comment Type TR Comment Status D Pres: Darshan2

(This is identical comment to other one that I sent. Here I have updated the file to darshan_02_0916.pdf insted darshan_01_0716.pdf from July which its base line is the same. The only differences are in the Annex where "Im' was changes to "Imax" in few places to be consistent with the rest of the document.)

Equation 33-15 can be simplified per the work done in http://www.ieee802.org/3/bt/public/jul16/darshan_01_0716.pdf and was accepted according the straw poll in last meeting to be used in D2.0.

See updated version of it (baseline was not changed) in darshan_02_0916.pdf.

SuggestedRemedy

Addopt darshan_02_0916.pdf for D2.0.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY DS

WFP

Cl 33 SC 33.2.8.8 P 114 L 44 # 441
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PSE Power

"The PSE remains in the IDLE state as long as the average voltage across the pairset is below V Off max."

Or in the DISABLED state...

SuggestedRemedy

"The PSE remains in the IDLE or DISABLED state as long as the average voltage across the pairset is below V Off max."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Remove sentence.

TFTD CB

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.10 P 129 L 1 # 454
 Yseboodt, Lennart Philips

Comment Type T Comment Status X Pres: Yseboodt3

The PD inrush specification is mismatched between the text and the state diagram.
 We have now adopted accurate inrush text in 33.3.8.3, the SD should reflect this.

SuggestedRemedy

Adopt yseboodt_03_0916_pdinrushsd.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.9 P 129 L 11 # 210
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan12

The subject is: Figure 33-32 (PD single signature state diagram), dll_power_type, dll_power_level and the synch with Figure 33-50 which is currently is good only for Type 1 and Type 2.

Background:

PD Type 1/2 state machine:

In page 122 line 45 we have a definition for pse_dll_power_type that is used in PD Type 1 and 2 state machine in page 124 line 30 at the exit from MDI_PWR1.

The pse_dll_power_type is used in the PD power control state diagram (LLDP) Figure 33-50.

So far all is good.

Single Signature PD Type 3/4 state machine:

In page 127 line 11 we have a definition for pse_dll_power_level that should be used in the single-signature PD Type 3 and 4 state machine on page 129 line 11 at the exit from MDI_PWR1 but instead there is pse_dll_power_type there as was in Type 1/2 PD state machine.

The pse_dll_power_type is required in the PD power control state diagram (LLDP) Figure 33-50 but is not defined in the variable list (what is defined is only pse_dll_power_level.

The problems are:

1. For Type 3 and 4 single-signature PD: It needs to be pse_dll_power_level and not pse_dll_power_type.
2. Type 3 and 4 single-signature PD state diagram and variable list should be sync with Figure 33-50 that historically needs pse_dll_power_Type only for Type 1 and 2.
3. We need figure 33-50 to work with Legacy and new single-signature PDs.

SuggestedRemedy

Adopt darshan_12_0916.pdf if available for the meeting. If not,

To add Editor Note to page 129:

"Editor Note: (1) To make changes in Figure 33-50 so it can work with Type 1 and 2 by using the existing variables in Figure 33-50 and work with dll_power_level when it is Type 3 and Type 4 PDs. (2) Type 3 and 4 single-signature PD state diagram and variable list should be sync with Figure 33-50."

Proposed Response Response Status W

TFTD

WFP

See 296

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Cl 33 SC 33.3.3.10 P 129 L 15 # 31
 Picard, Jean Texas Instruments

Comment Type **TR** Comment Status **X** Pres: Yseboodt3

The PD behavior during inrush is not fully described in the state diagram, referring to 33.3.8.3. For example, Single-signature PDs assigned to Class 1, 2, or 3 shall conform to PClass_PD and PPeak_PD within TInrush-2P min. Another example is that it has to meet inrush requirements with the PSE behavior as defined in 33.2.8.5.

SuggestedRemedy

Add an editor's note to review the PD state diagram to cover inrush behavior.

Proposed Response Response Status **W**

TFTD

WFP

Cl 33 SC 33.3.6 P 141 L 21 # 373
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **D** Pres: Yseboodt9

"... shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer."

The 'active indication' shall is:

- untestable
- out of scope for an interoperability standard

SuggestedRemedy

"... shall conform to Type 1 PD power restrictions."

Proposed Response Response Status **W**

PROPOSED REJECT.

This is legacy text and has was debated heavily (from what I have heard).

TFTD

Cl 33 SC 33.3.8 P 146 L 44 # 524
 Stover, David Linear Technology

Comment Type **T** Comment Status **X** Pres: Darshan16

P_Peak_PD-2P (used in section 33.3.8.5, which references this table) is missing.

SuggestedRemedy

Define P_Peak_PD-2P (TFTD).

Proposed Response Response Status **W**

TFTD as requested

Cl 33 SC 33.3.8.3 P 149 L 21 # 385
 Yseboodt, Lennart Philips

Comment Type **E** Comment Status **X** Pres: Yseboodt9

"The PD shall meet the inrush requirements with the PSE behavior described in 33.2.8.5."

I guess the intent was to say "PD only needs to meet the inrush requirements if the PSE complies to 33.2.8.5".

Do we really need to say this ? The same applies to nearly every other PD parameter as well.

Also, the earlier shalls are not conditional upon this one, so it has no effect in its current form.

SuggestedRemedy

Remove "The PD shall meet the inrush requirements with the PSE behavior described in 33.2.8.5."

Proposed Response Response Status **W**

TFTD

I know that this sentence was added to make sure that PD implementers are aware of the PSE current capabilities at different voltage levels (something that has caused a great deal of issues in the field).

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Cl 33 SC 33.3.8.5 P 151 L 31 # 50
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X PD Power

Figures 33-37, 33-38, and 33-39 show PD upperbound templates. These are also described as operating masks, and a normative shall states the PDs must operate below these upperbound templates.

The figures are valid up to T_{Cut-2P} min for a single peak rising above the P_{Class_PD} power level. The figures are not valid for multiple peaks that are shorter duration than T_{Cut-2P} min (see 5% duty cycle in 33.3.8.4).

SuggestedRemedy

Change the NOTE as follows and put it under each respective template (replacing the existing notes where they appear):

NOTE - Figure 33-## applies to a single peak which exceeds the P_{Class_PD} power value.

Proposed Response Response Status W

TFTD

remove figures and associated text.

Cl 33 SC 33.3.8.5 P 151 L 32 # 51
 Bennett, Ken Sifos Technologies, In

Comment Type E Comment Status D PD Power

The templates show a second upperbound step after T_{cut-2P} min. This step is the power that a peak pulse must fall below before PSE T_{Cut} timing is reset.

After a Peak lasting T_{Cut-2P} min ends, the instantaneous power must stay below the second step for 950msecs. Peaks lasting less than T_{Cut-2P} min may exceed the second step after droppin below the P_{Class_PD} power level.

The always-valid portion of the second step is the transition at T_{Cut-2P}-min.

SuggestedRemedy

For clarity, shorten the duration of the second step in Figures 33-37, 33-38, 33-39 to 1/4 or 1/8 of their existing length.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

I believe what Ken would like is to shorten (in time) the horzontal line that extends along the P_{class_PD}(-2P) line.

If correct, make the change. If incorrect, Ken to comment.

TFTD FS LY CJ YD

Cl 33 SC 33.3.8.10 P 155 L 30 # 53
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Pres: Bennett1

Section 33.3.8.10 describes a test set-up to meet I_{con-2P} and I_{con-2P_unb}, which are necessary for interoperability.

The Normative "Shall" refers to a test set-up (derived from models) as the condition under which I_{con-2P} and I_{con-2P_unb} must be met. There are deficiencies in this approach which can result in interoperability problems.

SuggestedRemedy

See Bennett_01_0916.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.8.10 P 156 L 9 # 244
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan4

See darshan_04_0916.pdf for the correct drawing.

In figure 33-40, all Resistors are marked as R_{source_max} which is incorrect.

It should start with R_{source_min} from top, and then R_{source_max}, R_{source_min} and R_{source_max} in this order.

See darshan_04_0916.pdf for the correct drawing.

SuggestedRemedy

See darshan_04_0916.pdf for the correct drawing.

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 33 SC 33.6 P 177 L 40 # 239
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan11

Type 3 and Type 4 single signature state machine is not complete and contradicts DLL power management in clause 33.6.

The main issues are:

1. Figure 33-50 is not supporting Type 3 and Type 4 single-signature PDs. (need to support pse_dll_power_level and pse_dll_power_type)
2. Duplicate variables used in 33.6 and 33.3.3.7 (e.g pse_dll_power_level)

SuggestedRemedy

Add "Editor Note: clause 33.6 and 33.3.3.7 need to be in sync.

The following issues need to be addressed:

1. Figure 33-50 is not supporting Type 3 and Type 4 single-signature PDs. (need to support pse_dll_power_level and pse_dll_power_type)
2. Duplicate variables used in 33.6 and 33.3.3.7 (e.g pse_dll_power_level)."

Proposed Response Response Status W

TFTD

I don't think adding editor's notes pointing out technical incompleteness are a good idea at this point. We need actual solutions.

CI 33 SC 33.6 P 177 L 40 # 214
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan11

33.6 Data Link Layer classification need to be updated in order to:

1. support dual-signature PD.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, PD DLL power state maching and its variable list and figure 33-50 mainly and maybe Figure 33-49 as well.
3. In addition clause 33.6 needs to be in sync with PD single and dual signature state machines and their variable list.

SuggestedRemedy

Adopt darshan_11_0915.pdf if ready for the meeting. If not, add the following editor note to the beginning of clause 33.6:

"Editor Note: 33.6 Data Link Layer classification need to be updated in order to:

1. support dual-signature PD.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, PD DLL power state maching and its variable list and figure 33-50 mainly and maybe Figure 33-49 as well.
3. sync 33.6 with PD single and dual signature state machines and their variable list."

Proposed Response Response Status W

TFTD

WFP

CI 33 SC 33.6 P 177 L 40 # 304
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X Pres: Darshan11

A DLL subject matter expert should add text covering dual-signature PDs. A state diagram may be required and a LLDP attribute map would also then be required.

SuggestedRemedy

Add on line 40, "Editor's Note: readers are encouraged to improve the DLL to incorporate dual-signature PDs." This comment should not be considered satisfied until an acceptable solution is provided to address the comment made.

Proposed Response Response Status W

TFTD

I don't think adding editor's notes pointing out technical incompleteness are a good idea at this point. We need actual solutions.

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 33 SC 33.6.3.2 P 179 L 18 # 305
 Schindler, Fred Seen Simply, Broadco
 Comment Type **TR** Comment Status **X** Pres: Schindler
 Variable parameter_type is determined only by Type 1 and 2 function set_parameter_type, therefore it will only have values 1 and 2. Variable pd_allocated_power is not assigned anywhere and is required to determine PSE_INITIAL_VALUE.
 SuggestedRemedy
 The solution is provided in schindler_3bt_01_0916.
 Proposed Response Response Status **W**
 TFTD
 WFP

CI 33 SC 33.6.3.2 P 179 L 19 # 475
 Yseboodt, Lennart Philips
 Comment Type **T** Comment Status **X** Pres: Yseboodt2
 The constant PSE_INITIAL_VALUE needs to be initialized, but the way this is done is different for Type 1/2 and Type 3/4.
 Since we want to avoid splitting the DLL state diagrams, and this is (for now) the only variable that is causing trouble, we should initialize it differently depending on PSE Type.
 SuggestedRemedy
 Adopt yseboodt_02_0916_pseinitialvalue.pdf
 Proposed Response Response Status **W**
 TFTD
 WFP

CI 33 SC 33.6.5 P 186 L 4 # 316
 Schindler, Fred Seen Simply, Broadco
 Comment Type **TR** Comment Status **X** Pres: Yseboodt1
 An auticlass subject matter expert should add text covering this topic. A state diagram may be required and a LLDP attribute map would also then be required. This comment is related to other comments marked COMMENT-2.
 SuggestedRemedy
 Add on line 5, "Editor's Note: readers are encouraged to improve Autoclass information by adding text and state diagrams as appropriate." This comment should not be considered satisfied until an acceptable solution is provided to address the comment made.
 Proposed Response Response Status **W**
 TFTD
 WFP

CI 33 SC 33.6.5 P 186 L 4 # 476
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **X** Pres: Yseboodt1
 DLL Autoclass section is missing content.
 SuggestedRemedy
 Adopt yseboodt_01_0916_dllautoclass.pdf
 Proposed Response Response Status **W**
 TFTD
 WFP

CI 33 SC 33.6.5 P 186 L 13 # 54
 Bennett, Ken Sifos Technologies, In
 Comment Type **E** Comment Status **X** Pres: Yseboodt1
 Table 33-60 describes transactions using "LLDP Frame". All other data link classification transactions in the standard use the more specific terms: "Power via MDI TLV", "LLDPDU", or "TLV Frame".
 There isn't a formal "LLDP Frame" definition in Clause 33, whereas "TLV Frame" is specifically defined in section 33.6.1.
 SuggestedRemedy
 Change all instances of "LLDP Frame" in table 33-60 to:
 "TLV Frame" or "LLDPDU"
 Proposed Response Response Status **W**
 TFTD
 WFP

CI 79 SC 79.3.7.4 P 222 L 20 # 69
 Ran, Adeo Intel
 Comment Type **TR** Comment Status **X** **LLDP**
 Does "should" here mean it is only a recommendation? Is it OK to have more than one?
 Also applies to 79.3.2.7, although it is in the base document.
 SuggestedRemedy
 Change to "shall" unless there is no problem with having more than one.
 Proposed Response Response Status **W**
 TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33B SC 33B.1 P 237 L 8 # 118
 Hajduczenia, Marek Charter Communicatio

Comment Type ER Comment Status A Editorial

No subclause numbers

SuggestedRemedy

Please add subclause numbers in Annex 33B

Response Response Status U

ACCEPT IN PRINCIPLE.

There are annex numbers, there is just a bunch of text and a drawing before you get to the first one, 33B.1 (line 50).

Editor to renumber Annex 33B to put introductory material into 33B.1 and increment all other subclause numbers.

TFTD YD

Cl 33 SC Annex 33B P 237 L 16 # 193
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan6

(See darshan_06_0916.pdf)
 Annex 33B directs the reader to Annex 33D to find important informative data to how Rload_min/max where derived. This Annex is missing and should be added as planned.

SuggestedRemedy

See proposed remedy in darshan_06_0916.pdf for Annex D.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC Annex 33B P 237 L 16 # 250
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan6

(See darshan_06_0916.pdf)
 Annex 33B directs the reader to Annex 33D to find important informative data to how Rload_min/max where derived and other parts that are pair to pair related. This Annex is missing and should be added as planned.

Annex D is needed since all the parts of pair to pair unbalance are spread all over the spec and it is hard to see the whole picture. I find it very useful to have short summary that show the whole spec explained in short in 1.5 pages and it was planned to be there long time ago. Annex D content was reviewed many times in the original contribution (see the reference at the end) and base on it, the whole spec was built.

SuggestedRemedy

See proposed remedy in darshan_06_0916.pdf for Annex D.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33B.1 P 238 L 30 # 204
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan3

Figure 33B-2:
 1. The drawing looks like broken on the left side at the connections to Vport_pse, Vdiff1 and Vdiff2.
 2. The arrows marking the point of measuring Veff1, Veff1, Veff3 abd Veff4 are not sufficiently clear where they are pointing. Follow the original drawing darshan_03_0916.pdf for the intent.

SuggestedRemedy

Editor to:
 1. Fix the broken connection in Figure 33B-2.
 See reference in darshan_03_0916.pdf.
 2. To align the arrows to the correct position as exactly as shown in darshan_03_0916.pdf.

Proposed Response Response Status W

TFTD

WFP