Comment (#48, #49)

TDL #129, #152 D2.3: To verify that Icon-2P_unb, Ipeak-2P_unb and ILIM-2P are in sync with Table 145-17 values when resistors values are set to +/-1% tolerance.

In addition:

1. In last cycles, we have updated the 4-pair model to address the following changes:
   -PClass_PD for class 8 was changed back from 71W to 71.3W
   -Channel pair to pair resistance unbalance was set to 7%.
   -Increasing PD Vdiff for class 7-8 from 50mV to 60mV to increase design margin for extended power.
2. As a result, we have updated the values of Icon-2P_unb for class 7 and class 8.

Next step:

3. To verify that Icon-2P_unb for class 5 and 6 is updated and has sufficient margin to meet Table 145-17 load resistors accuracy of +/1%.
4. Evaluate the worst case simulated values of Ipeak-2P_unb vs the spec numbers as set by the equations and the rule: Ipeak-2P_unb_max=ILIM-2P-0.002A.

(We didn't check (some parts of items 1-4 in order to first finalize the discussion on significant bits and stabilizing the 4-pair model for all operating modes including extended power. (See Annex A in http://www.ieee802.org/3/bt/public/mar17/darshan_01_0317.pdf)

Simulations result vs. D2.4 specifications.

Evaluating Icon-2P_unb

Class	Simulated [A]	D2.4 Spec [A]	Proposed D2.5 spec [A]	Notes
5	0.547	0.55	No change	3mA margin. Meets TDL#129 objectives.
6	0.679	0.682	No change	3mA margin. Meets TDL#129 objectives.
7	0.786	0.781	No change	5mA margin. Meets TDL#129 objectives.
8	0.866	0.932	No change	Margin is significant to allow extended power with reasonable unbalance (PD Vdiff).

Evaluating Equation 145-15

Equation 145-15 was derived per simulation results. No change to spec.

Evaluating Equation 145-12and Equation 145-13 (Ipeak-2P_unb) and ILIM-2P_min

A	B	C	D	E	F	G
	Simulated	Spec D2.4 per Eq 145-12	Margin	D2.4 spec	(ILIM-2P_min In D2.4) - (Simulated Ipeak-2P_unb)	Keeping the Rule: ILIM-2P - 2mA= Spec Ipeak-2P_unb
Class	Ipeak_2P_unb_max		(Spec)-(Simulation)	ILIM-2P_min		
5	0.558	0.560	0.002	0.562	0.004	0.002
6	0.697	0.700	0.003	0.702	0.005	0.002
7	0.812	0.827	0.015	0.829	0.017	0.002
8	0.967	0.988	0.021	0.990	0.023	0.002

1. We can update Equation 145-13 to reduce margin in column D to 0. As a result, ILIM-2P_min will be reduced accordingly per column G rule, OR we can leave column C as is as a design margin in addition to the simulated worst case numbers in column B.
2. If we decide to keep the margins in column D, no changes to the spec are required.

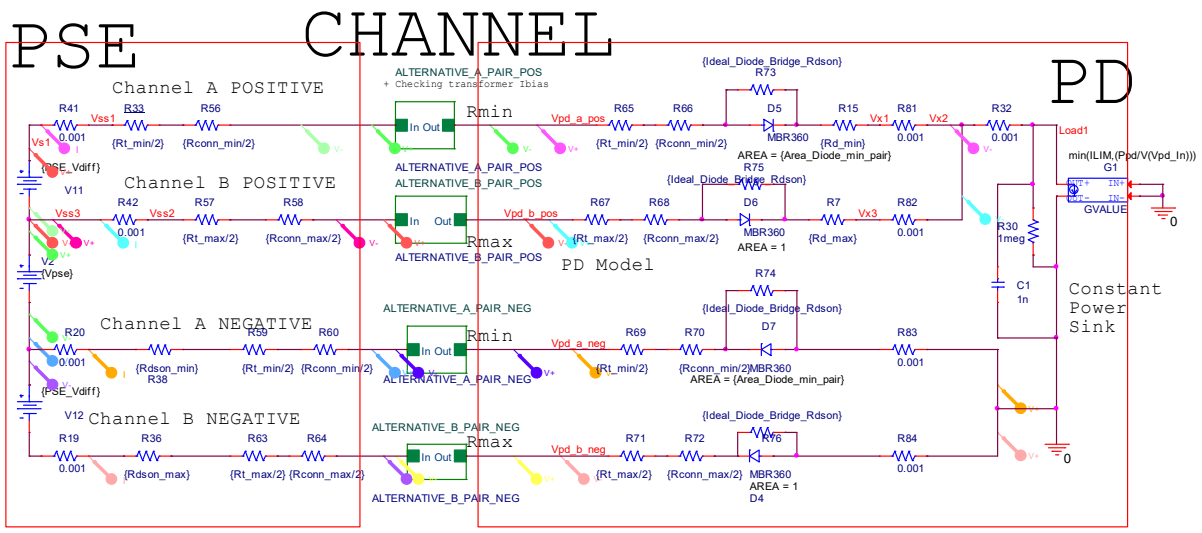
Suggested Remedy

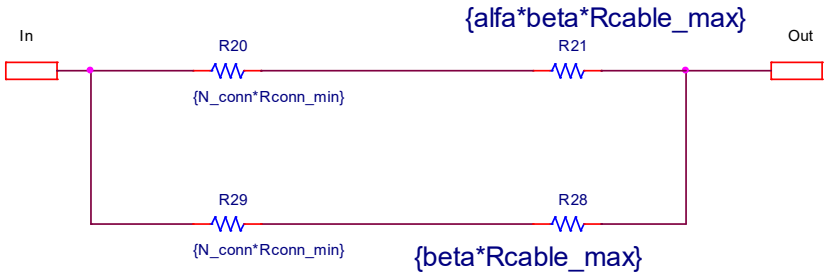
To discuss with the group. If no comments, no changes are required

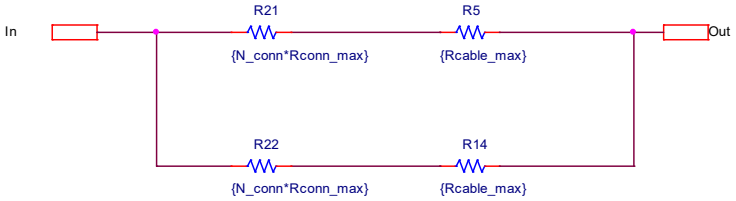
Annex A: 4-pairs Spice simulation model parameters used to specify IEEE802.3bt D2.3 and D2.4 requirements.

The following values of the 4-pair model where used to set the specification requirements of the PSE PI and the PD PI unbalance requirements as a function of the total system end to end pair to pair effective resistance/current unbalance.

#	Parameter	Units	Class 5-6		Class 7-8		Notes
			Min	Max	Min	Max	
1	Vpse	Vdc	50.31	----	52.31	----	PSE voltage source, no load voltage
2	Ppd	W	40, 51	----	62, 71.3	----	PD input power measured at the PD PI
3	Ppd extended power	W	59.7	----	89.4	----	PD input power measured at the PD PI
4	Lcable	m	2.65	100	2.65	100	Cable and cordage length.
5	Diode AREA2	-	10		10		Diode simulation parameter. Set the PD Vdiff compare to the diode in the pair with minimum resistance that is set to AREA=1. As a result, PD Vdiff is set to Vdiff=(n*K*T/q) *LN(Is2/Is1) while Is2=Is1 (same diodes only AREA parameter is changed). As a result, AREA2/AREA1 sets PD Vdiff. For AREA2=10 we will get PD Vdiff =60mV measured at IF=10mA (PD Vdiff is the pair to pair PD voltage difference caused by the forward voltage difference between two diodes on pairs of the same polarity. PD Vdiff is determined at low current (few mA range). When current increase the effect of PD Vdiff on the PD contribution to its PI unbalance and to the total system unbalance is reduced. The use of diodes with higher Vdiff, will increase the PD unbalance at high currents. Therefore, a limit of 60mV for PD Vdiff was set at 10mA.
	Diode AREA1	-	1	----	1		Diode simulation parameter set to AREA 1. This diode is located at the pair with maximum resistance.
	Cordage Resistivity	Ω/m	0.0926	----	0.0926	----	Used for short channel length with Lcacble =2.65m simulations
	Cable resistivity	Ω/m	0.074	----	0.074	----	Used for short channel length with Lcacble =2.65m simulations
	Number of connectors	-	0	----	0	----	Used for short channel length with Lcacble =2.65m simulations
	Cordage Resistivity	Ω/m	0.123	Ω	0.123	----	Used for long channel length with Lcacble =100m simulations
	Cable resistivity	Ω/m	0.123	Ω	0.123	----	Used for long channel length with Lcacble =100m simulations
	Number of connectors	-	4	----	4	----	Used for long channel length with Lcacble =100m simulations
	Minimum Channel Resistance wire 1	Ω	=α*β*Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity)+N*Rconn_min				1st wire of the pair with minimum resistance α=(1-pair_Runb)/(1+pair_Runb) =0.96. Pair_Runb=0.02. β=(1-pair2p_Runb)/(1+pair2p_Runb) =0.9. Pair2p_Runb=0.06 for IEEE802.3bt D2.3 and was changed to β=(1-pair2p_Runb)/(1+pair2p_Runb) =0.8867. Pair2p_Runb=0.06 to ensure total channel pair to pair resistance unbalance of 7% per Annex 145A.2 D2.4 Wire length is measured from PSE PI to PD PI (not round loop). Each pair of the same polarity has two wires (wire 1 and wire 2) are connected in parallel and form common mode resistance of that pair. In the positive pairs, we have two pairs with the same voltage polarity, the 1st pair is set to minimum resistance and the 2nd pair is set to maximum resistance. The same applies to the negative pairs.
	Minimum Channel Resistance wire 2	Ω	=β*Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity)) +N*Rconn_min				
	Maximum Channel Resistance wire 1 and wire 2		Lcable*(0.1*cordage_resistivity+0.9*cable_resistivity)				
	PSE Vdiff	mV	10	----	10	----	
	Rt	Ω	0.12	0.13	0.12	0.13	Transformer winding resistance
	Rconn	Ω	0.03	0.05	0.03	0.05	Connector resistance
	Rdson	Ω	0.07	0.1	0.07	0.1	
	Rsense	Ω	0.0225	0.25	0.0225	0.25	







Simulation results on the positive pairs Done for IEEE802.3bt D2.2 and D2.3 for reference.

Cable Length (m)	2.65m	100m	Spec in D2.2	Notes
Channel max common mode resistance (Ω)	0.2	12.5		It is the value of two conductors in parallel from PSE PI to PD PI and back.
Number of connectors	0	4		
PSE Vdiff (mV)	10	10		
PD Vdiff (mV)	60	60		
Pair with maximum current (mA) on (I(R41))	Imax,	Imax,	Imax=Icont_2P_unb	Positive pairs
Class 5	547.07	483.86	550(*)	Maximum current is at short cable length.
Class 6	678.65	638.83	682(*)	Maximum current is at short cable length.
Class 7	780.85	764.43	781(**)	Maximum current is at short cable length. Different from D2.1 results (maximum current was at long cable) due to different model parameters values that was updated at D2.1 meeting.
Class 8	911.62	911.61(*)	931(***)	Maximum current is at long cable length.

(*) Spec was not changed in D2.2 for class 5 and 6 due to last model changes in order to finish first the significant digit's issues.
(**) (Spec was changed in D2.2 for class 7 to update per the updated sim results.
(***) Spec was changed in D2.2 for class 8 to allow PD margin for Extended Class 8 use case. D2.1 spec was 925mA.