

1 **Baseline proposal for P2PRUNB**

2 Proposed: working flow

- 3 1. Review and clean to be technically correct
4 2. Some texts and drawings may be merged for multiple parameters for less wording
5 and clarity. This to be done during comment resolution stage
6 3. Using global parameters and moving to table 33-11 etc. can be done after steps 1 and
7 2. Now it is not worth the work since many things may be changed and it is to
8 complex now.

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10 **33.1.4.2 Type 1 and Type 2 channel Pair Resistance Unbalance requirement**

11 Type 1 and Type 2 operation requires that the resistance unbalance shall be 3 % or less. Resistance
12 unbalance is a measure of the difference between the two conductors of a twisted pair in the 100Ω
13 balanced cabling system. Resistance unbalance is defined as in Equation (33-1):

14
15 (33-1)

$$\left\{ \frac{(R_{\max} - R_{\min})}{(R_{\max} + R_{\min})} \times 100 \right\} \%$$

16
17

18 where

19 R_{\max} is the resistance of the channel conductor with the highest resistance

20 R_{\min} is the resistance of the channel conductor with the lowest resistance

21 **33.1.4.3 Type 3 and Type 4 Cable Requirement for Pair to Pair Resistance unbalance**

22 4 pair operation requires the additional specification of resistance unbalance between each two
23 pairs of the cable. The cable pair to pair resistance unbalance shall be 5% (TBD) or
24 less. Resistance unbalance between the pairs is a measure of the difference of resistance of the
25 common mode pairs of conductors used for power delivery. Cable pair to pair resistance
26 unbalance is defined by equation 33-1.1:

27
$$\left\{ \frac{(R_{cm_max} - R_{cm_min})}{(R_{cm_max} + R_{cm_min})} \times 100 \right\} \%$$
 33-1.1

28 where

29 R_{cm_max} is the pair with highest common mode resistance.

30 R_{cm_min} is the pair with lowest common mode resistance.

31 Common mode resistance is the resistance of the two wires in a pair, connected in parallel.

32

33 **33.1.4.4 Type 3 and Type 4 Channel Requirement for Pair to Pair Resistance unbalance**

34 4P pair operation requires the additional specification of resistance unbalance between each
35 two pairs of the channel. The channel pair to pair resistance unbalance shall be TBD% or
36 less. Resistance unbalance between the channel pairs is a measure of the difference of
37 resistance of the common mode pairs of conductors used for power delivery. Channel pair to
38 pair resistance unbalance is defined by equation 33-1.2:

39
$$\left\{ \frac{\left(\sum R_{cm_max} - \sum R_{cm_min} \right)}{\left(\sum R_{cm_max} + \sum R_{cm_min} \right)} \times 100 \right\} \% \quad 33-1.2$$

40 Where

41 $\sum R_{cm_max}$ is the sum of channel pair elements with highest common mode resistance.

42 $\sum R_{cm_min}$ is the sum of channel pair elements with highest common mode resistance.

43 Common mode resistance is the resistance of the two wires in a pair, connected in parallel.

44 **33.1.4.5 Type 3 and Type 4 PSE PI Pair to Pair resistance unbalance**

45 4P pair operation requires the additional specification of PSE PI resistance unbalance.

46 PSE PI pair to pair resistance unbalance shall be TBD % or less.

47 Resistance unbalance between the pairs at the PSE PI is a measure of the difference of common
48 mode DC output resistance between any two pairs used for power delivery at the PI.

49 PSE PI pair to pair resistance unbalance is defined by equation 33-1.3:

50
$$\left\{ \frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100 \right\} \% \quad 33-1.3$$

51 Where

52 R_{max} is the PSE PI common mode DC output resistance of the pair with highest common mode
53 resistance.

54 R_{min} is the PSE PI common mode DC output resistance of the pair with lowest common mode resistance.

55

56 **PSE Pair to Pair Voltage difference requirements for Environment A:** TBD% max.

57 **PSE Pair to Pair Voltage difference requirements for Environment B:** TBD% max.

58 **Test procedure/setup for compliance:** TBD

59 **33.1.4.6 Type 3 and Type 4 PD PI Pair to Pair resistance unbalance**

60 4P pair operation requires the additional specification of PD PI resistance unbalance.

61 PD PI pair to pair resistance unbalance shall be TBD % or less.

62 Resistance unbalance between the pairs at the PD PI is a measure of the difference of common
63 mode DC input resistance between any two pairs used for receiving power at the PI.

64 PD PI pair to pair resistance unbalance is defined by equation 33-1.4:

$$\left\{ \frac{(R_{\max} - R_{\min})}{(R_{\max} + R_{\min})} \times 100 \right\} \%$$

65

33-1.4

66 Where

67 R_{\max} is the PD PI common mode DC input resistance of the pair with highest common mode resistance.

68 R_{\min} is the PD PI common mode DC input resistance of the pair with lowest common mode resistance.

69

70 **PD Pair to Pair Voltage difference requirements for Environment A:** TBD% max.

71 **PD Pair to Pair Voltage difference requirements for Environment B:** TBD% max.

72 **Test procedure/setup for compliance:** TBD