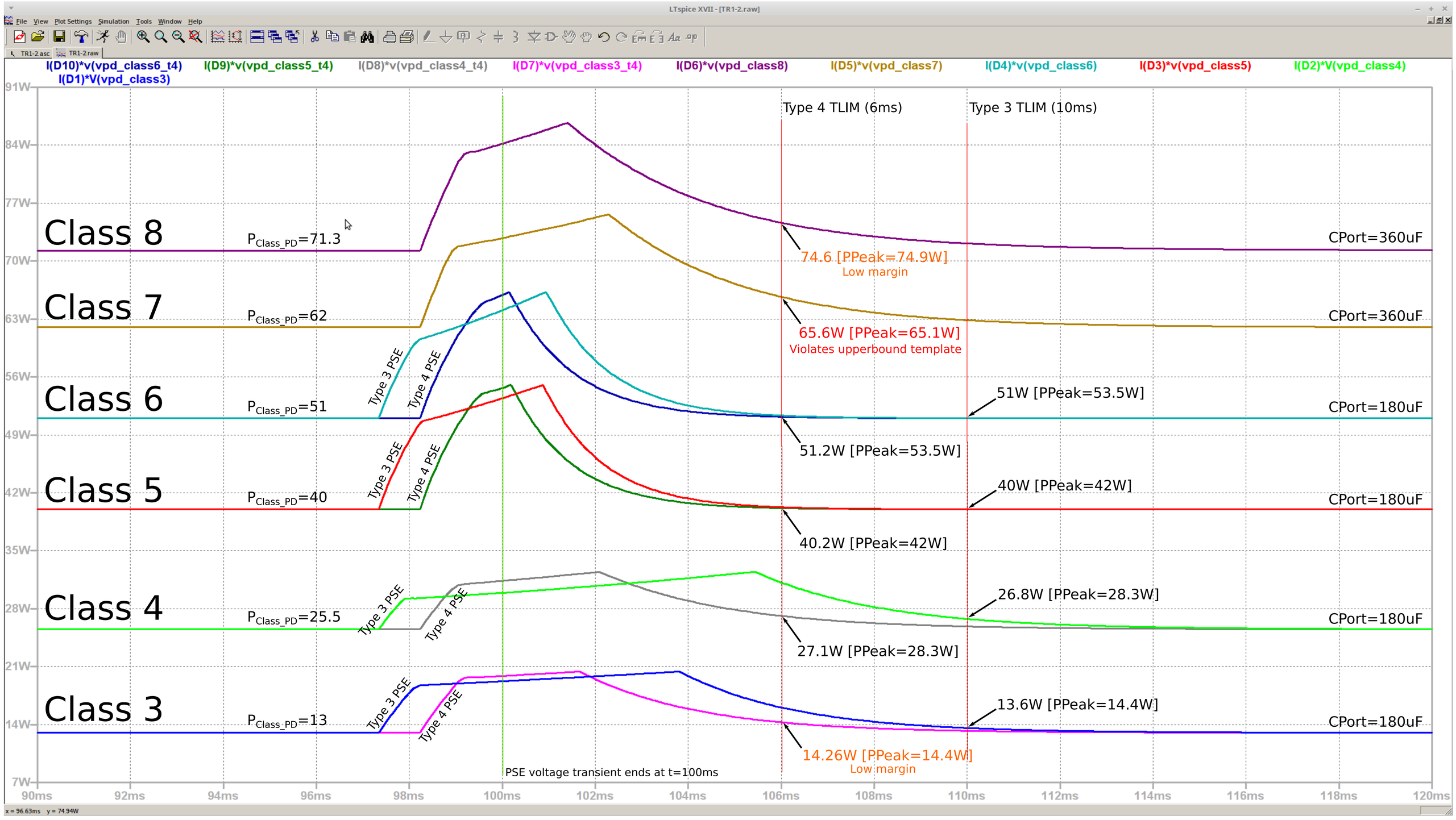
LTspice XVII - [TR1-2.raw]
File View Plot Settings Simulation Tools Window Help
TR1-2.asc
TR1-2.raw
I(D10)*v(vpd_class6_t4)
I(D1)*V(vpd_class3)
I(D9)*v(vpd_class5_t4)
I(D8)*v(vpd_class4_t4)
I(D7)*v(vpd_class3_t4)
I(D6)*v(vpd_class8)
I(D5)*v(vpd_class7)
I(D4)*v(vpd_class6)
I(D3)*v(vpd_class5)
I(D2)*V(vpd_class4)
91W
84W
77W
70W
63W
56W
49W
42W
35W
28W
21W
14W
7W
90ms
92ms
94ms
96ms
98ms
100ms
102ms
104ms
106ms
108ms
110ms
112ms
114ms
116ms
118ms
120ms
Type 4 TLIM (6ms)
Type 3 TLIM (10ms)
Class 8
P_Class_PD=71.3
CPort=360uF
74.6 [PPeak=74.9W]
Low margin
Class 7
P_Class_PD=62
CPort=360uF
65.6W [PPeak=65.1W]
Violates upperbound template
Class 6
P_Class_PD=51
CPort=180uF
51W [PPeak=53.5W]
51.2W [PPeak=53.5W]
Class 5
P_Class_PD=40
CPort=180uF
40W [PPeak=42W]
40.2W [PPeak=42W]
Class 4
P_Class_PD=25.5
CPort=180uF
26.8W [PPeak=28.3W]
27.1W [PPeak=28.3W]
Class 3
P_Class_PD=13
CPort=180uF
13.6W [PPeak=14.4W]
14.26W [PPeak=14.4W]
Low margin
Type 3 PSE
Type 4 PSE
PSE voltage transient ends at t=100ms
x = 96.63ms y = 74.94W