

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 1 SC 1.3 P 20 L 3 # 151
 Laubach, Mark Broadcom Limited
 Comment Type E Comment Status R Editorial
 Remote editor's note and subclause 1.3. Not needed if there is not content under 1.3.
 SuggestedRemedy
 As per comment.
 Response Response Status C
 REJECT.
 A normative reference is being added by comment 88.
 TFTD

Cl 30 SC 30.9.1.1.7 P 29 L 23 # 485
 Stover, David Linear Technology
 Comment Type T Comment Status D Pres: Law1
 The phrase "this will map to" is unclear. Does this mean the counter will map to or the increment will map to. Either way it is incorrect. The increment has to map to an edge event.
 SuggestedRemedy
 Change
 If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;
 to
 If a Clause 22 MII or Clause 35 GMII is present, then this counter is incremented when the Invalid Signature bit specified in 33.5.1.2.6 changes from FALSE to TRUE.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD (need an expert)
 Note: legacy text
 TFTD FS

Cl 30 SC 30.9.1.1.8 P 29 L 35 # 486
 Stover, David Linear Technology
 Comment Type T Comment Status D Pres: Law1
 The phrase "this will map to" is unclear. Does this mean the counter will map to or the increment will map to. Either way it is incorrect. The increment has to map to an edge event.
 SuggestedRemedy
 Change
 If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;
 to
 If a Clause 22 MII or Clause 35 GMII is present, then this counter is incremented when the Power Denied bit specified in 33.5.1.2.4 changes from FALSE to TRUE.;
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD (need an expert)
 Note: legacy text
 TFTD FS

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Cl 30 SC 30.9.1.1.9 P 29 L 47 # 487
 Stover, David Linear Technology

Comment Type T Comment Status D Pres: Law1

The phrase "this will map to" is unclear. Does this mean the counter will map to or the increment will map to. Either way it is incorrect. The increment has to map to an edge event.

SuggestedRemedy

Change
 If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;

to
 If a Clause 22 MII or Clause 35 GMII is present, then this counter is incremented when the Overload bit specified in 33.5.1.2.8 changes from FALSE to TRUE.;

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD (need an expert)

Note: legacy text

TFTD FS

Cl 30 SC 30.9.1.1.10 P 30 L 5 # 488
 Stover, David Linear Technology

Comment Type T Comment Status D Pres: Law1

The phrase "this will map to" is unclear. Does this mean the counter will map to or the increment will map to. Either way it is incorrect. The increment has to map to an edge event.

SuggestedRemedy

Change
 If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Short Circuit bit specified in 33.5.1.2.7.;

to
 If a Clause 22 MII or Clause 35 GMII is present, then this counter is incremented when the Short Circuit bit specified in 33.5.1.2.7 changes from FALSE to TRUE.;

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD (need an expert)

Note: legacy text

TFTD FS

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Cl 30 SC 30.9.1.1.11 P 30 L 17 # 489
 Stover, David Linear Technology

Comment Type T Comment Status D Pres: Law1

The phrase "this will map to" is unclear. Does this mean the counter will map to or the increment will map to. Either way it is incorrect. The increment has to map to an edge event.

SuggestedRemedy

Change
 If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;

to
 If a Clause 22 MII or Clause 35 GMII is present, then this counter is incremented when the MPS Absent bit specified in 33.5.1.2.9 changes from FALSE to TRUE.;

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD (need an expert)

Note: legacy text

TFTD FS

Cl 33 SC 33.1.3 P 44 L 1 # 492
 Stover, David Linear Technology

Comment Type T Comment Status D Cabling

The text carefully distinguishes between DC loop resistance and DC pair loop resistance, stating this clause uses only DC pair loop resistance.

Furthermore the resistance is described as the path from the PSE PI to the PD PI. It is actually the round trip path.

Then the text refers to the wrong one...

"The cable references use "DC loop resistance," which refers to a single conductor. This clause uses "DC pair loop resistance," which refers to a pair of conductors in parallel. Therefore, RCh is related to, but not equivalent to, the "DC loop resistance" called out in the cable references.

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI. RChan-2P has a maximum value of RCh."

SuggestedRemedy

Change

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI.

RChan-2P has a maximum value of RCh.

to

RChan is the actual DC loop pair resistance between the PI of the PSE and the PI of the PD and back to the PSE PI. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

RChan-2P is the actual DC loop pair resistance of a pairset from the viewpoint of the PSE PI and the PD PI.

RChan-2P has a maximum value of RCh.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS LY

RChan is the actual DC loop resistance between the PI of the PSE and the PI of the PD and back to the PSE PI. RChan has a maximum value of RCh/2 when operating in 4-pair mode.

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RChan-2P is the actual DC loop resistance of a pairset from the viewpoint of the PSE PI and the PD PI.
Rchan-2P has a maximum value of RCh.

Cl 33 SC 33.2.5.9 P 66 L 5 # 240

Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Yseboodt6

'class_num_events_pri' have only options of 1,2,4 events but Table 33-7 says 1,2,3 and 4. To clarify the reason for differences. (is it because class_num_events_pri is maximum values?).

Same comment for page 66 line 15 regarding 'class_num_events_sec'

SuggestedRemedy

Group to clarify.

Proposed Response Response Status W

TFTD

I believe it should include "3" as an option based on our 4PID work...right?

Cl 33 SC 33.2.5.9 P 72 L 44 # 500

Stover, David Linear Technology

Comment Type T Comment Status X Pres: Yseboodt6

The class_num_events_pri and _sec to not match the available encodings for the variable definitions.

Legal values for pri/sec are 1,2, 4

SuggestedRemedy

Change Table 33-7 Type 3 row, _pri_sec column to 1,2,4

Proposed Response Response Status W

TFTD (See 240)

Cl 33 SC 33.2.5.12 P 79 L 19 # 36

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33-15:
Issue #5 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

From the IDLE state, the branch into START_CXN_CHK and the branch into START_DETECT can be True simultaneously when CC_DET_SEQ/= 1 and mr_pse_alternative/= 'both'.
Going through connection check only makes sense when mr_pse_alternative = 'both'.

SuggestedRemedy

Change to ((CC_DET_SEQ = 0) + (CC_DET_SEQ = 3)) *(mr_pse_alternative = both) *pse_ready *(pwr_app_pri + pwr_app_sec) *(mr_pse_enable = enable).

See yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Cl 33 SC 33.2.5.12 P 80 L 31 # 37

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33-15:
Issue #6 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

From DETECT_EVAL to IDLE (label A), parenthesis are missing around "(CC_DET_SEQ = 0) + (CC_DET_SEQ = 3)".
Without these, the AND takes precedence over the OR.

SuggestedRemedy

Add parenthesis.

See yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

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CI 33 SC 33.2.5.12 P 81 L 5 # 34

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33–15:
Issue #1 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

From CLASS_EVAL to POWER_UP the condition is "pd_req_pwr < pse_avail_pwr" which has the effect that if the PSE has Class 1 available and the PD requests Class 1 the PSE will hang in CLASS_EVAL.
The same applies to Class 2.

SuggestedRemedy

Changing it to "pd_req_pwr pse_avail_pwr" fixes the issue.
See yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

CI 33 SC 33.2.5.11 P 83 L 6 # 26

Picard, Jean Texas Instruments

Comment Type TR Comment Status D PSE SD

Using One unique PD_4pair_cand variable can help simplify the state diagram, even if staggered detection is used for DS PD.

SuggestedRemedy

Replace "PD_4pair_cand_pri <= TRUE" with "PD_4pair_cand <= TRUE"
Replace "PD_4pair_cand_pri <= FALSE" with "PD_4pair_cand <= FALSE"

Proposed Response Response Status W

TFTD CB

CI 33 SC 33.2.5.11 P 85 L 6 # 27

Picard, Jean Texas Instruments

Comment Type TR Comment Status X PSE SD

Using One unique PD_4pair_cand variable can help simplify the state diagram, even if staggered detection is used for DS PD.

SuggestedRemedy

Replace "PD_4pair_cand_sec <= TRUE" with "PD_4pair_cand <= TRUE"
Replace "PD_4pair_cand_sec <= FALSE" with "PD_4pair_cand <= FALSE"

Proposed Response Response Status W

TFTD CB

See 26

CI 33 SC 33.2.5.12 P 86 L 4 # 35

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33–15:
Issues #2-4 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

From CLASS_EV1_LCE the exits to MARK_EV1 and MARK_EV_LAST forget to check the variable pse_avail_pwr.
Currently the SD would allocate more power than is available.
Same in the state CLASS_EV2.
Same in the state CLASS_EV4.

SuggestedRemedy

Changing it to check the variable pse_avail_pwr fixes the issues.

See yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY DS

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Cl 33 SC 33.2.5.12 P 86 L 6 # 38

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33-15:
Issue #7 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

The SD still uses 'tacs_timer' which has been renamed to 'tclassacs_timer'.

SuggestedRemedy

Change to 'tclassacs_timer'.

See yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Cl 33 SC 33.2.5.12 P 86 L 22 # 254

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan8

The PSE state machine part for single signature when it needs to know class code by issuing 3 finger and then doing class reset due to lake of sufficient power in which it need to generate only one finger etc.

This is covered by the text but not in the state machine.

SuggestedRemedy

Add the missing state machine part in darshan_08_0916.pdf.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.2.5.12 P 90 L 4 # 39

Wendt, Matthias Philips Lighting

Comment Type TR Comment Status D Pres: Yseboodt6

State diagram Figure 33-15:
Issue #7 as already pinpointed in yseboodt_02_0716_sdfix_baseline.pdf and yseboodt_02_0716_sdfix.pdf

Resolution to Stovers comment #122 against D1.7 has not been implemented

SuggestedRemedy

Implement Stovers comment #122 against D1.7'.

See also yseboodt_02_0716_sdfix_baseline.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 396

TFTD LY

Cl 33 SC 33.2.6.7 P 94 L 28 # 290

Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X 4PID

This section covers what establishes PD_4pair_cand. The state diagrams Figures 33-16, and 33-17 may do this as well, but they do not match. These diagrams do use the variable and xxx_pri and xxx_sec. The single-signature state diagram Figure 33-15 does not use PD_4pair_cand. Nothing in the state diagrams establishes pd_4pair_cand for certain.

SuggestedRemedy

See related comment marked COMMENT-3 for a solution.

Proposed Response Response Status W

TFTD CB

Need to align pd_4pair_cand with pd_4pair_cand_pri and _sec.

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Cl 33 SC 33.2.7 P 96 L 43 # 407
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Yseboodt5

Unlike Type 2, Type 3 and Type 4 devices have a lot of parameters that are different depending on the Assigned Class.

An initial assigned class is set up during Physical Layer classification.

Using DLL the PD and PSE are able to change the allocated power. It makes sense that the assigned Class 'follows' the PSEAllocatedPower variable.

SuggestedRemedy

Adopt yseboodt_05_0916_dllclasschange.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.2.7.2 P 98 L 29 # 40
 Wendt, Matthias Philips Lighting

Comment Type T Comment Status D Pres: Yseboodt7

If during autotclass a PD changes its class signature to something other than '0' during TACS behavior is undefined as already pinpointed in yseboodt_03_0716_class.

It would be beneficial to define this for future use.

SuggestedRemedy

adopt yseboodt_03_0716_class

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS LY DS

Cl 33 SC 33.2.8 P 104 L 49 # 510
 Stover, David Linear Technology

Comment Type T Comment Status X Unbalance

Intra-pair current unbalance I_unb is specified as 3% I_Peak for Type 2, 3, and 4 PSEs. For higher Class PDs, this may preclude low-speed data implementations due to higher inductance requirements on those magnetics.

SuggestedRemedy

TFTD. Especially looking for opinions from magnetics vendors here.

Proposed Response Response Status W

TFTD

Cl 33 SC 33.2.8.2 P 105 L 51 # 28
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PSE Power

To ensure acceptable steady-state operating conditions, we need to explain in which circumstances longer than 250us transients or significant voltage steps may be expected.

SuggestedRemedy

Add the following note at the end of 33.2.8.2.

"PSE should avoid causing such long duration (> 250us) transients or significant voltage steps with the exception of rare circumstances involving switchover of power supplies to ensure system robustness."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add the following note at the end of 33.2.8.2.

"PSE should avoid causing such long duration (> 250us) transients or significant voltage steps with the exception of rare circumstances such as those involving switchover of power supplies to ensure system robustness."

TFTD YD

Cl 33 SC 33.2.8.4 P 108 L 21 # 512
 Stover, David Linear Technology

Comment Type ER Comment Status D Editorial

"P_Peak_PD-2P is the total peak power... see Table 33-25". P_Peak_PD-2P is not defined anywhere (captured in another comment), but if it were, it would live in Table 33-28.

SuggestedRemedy

Correct reference to Table 33-28.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Adopt changes in darshan_16_0916.pdf

TFTD DS YD

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Cl 33 SC 33.2.8.4.1 P 108 L 40 # 513
 Stover, David Linear Technology

Comment Type TR Comment Status X Pres: Stover1

R_PSE min and R_PSE max place restrictions on the PSE behind the PI, precluding PSE implementations. The spirit of these variables is to define and provide a much-needed test for system unbalance requirements. However, the variables are redundant to (and, for some valid operating parameters, in conflict with) the existing unbalance ratios implicit to I_Con and I_Con-2P_unb.

SuggestedRemedy

See stover_01_0916.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.2.8.5 P 109 L 43 # 249
 Darshan, Yair Microsemi

Comment Type TR Comment Status D Pres: Darshan2

(This is identical comment to other one that I sent. Here I have updated the file to darshan_02_0916.pdf insted darshan_01_0716.pdf from July which its base line is the same. The only differences are in the Annex where "Im' was changes to "Imax" in few places to be consistent with the rest of the document.)

Equation 33-15 can be simplified per the work done in http://www.ieee802.org/3/bt/public/jul16/darshan_01_0716.pdf and was accepted according the straw poll in last meeting to be used in D2.0. See updated version of it (baseline was not changed) in darshan_02_0916.pdf.

SuggestedRemedy

Addopt darshan_02_0916.pdf for D2.0.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY DS

WFP

Cl 33 SC 33.2.8.7 P 110 L 47 # 191
 Darshan, Yair Microsemi

Comment Type TR Comment Status D PSE Power

In the following text:
 "A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template in Figure 33-27, Figure 33-28, and Figure 33-29. Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template"."

There is missing text that says that the minimum value of ILIM-2P is the PSE lowerbound template as we did for the upperbound.

SuggestedRemedy

Change from:
 "A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33-27, Figure 33-28, and Figure 33-29. Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template"."

To:
 "The minimum value of ILIM-2P is the PSE lowerbound. A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33-27, Figure 33-28, and Figure 33-29. Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template"."

Proposed Response Response Status W

PROPOSED REJECT.

The upper bound template is called out directly as the max value for ILIM. The lower bound template consists of multiple named parameters, ILIM, ICON, IPEAK. This sentence is not needed. If it was it should be above the equations for the lower bound template, not where suggested.

TFTD

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Cl 33 SC 33.2.8.7 P 111 L 28 # 435
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **D** PSE Power
 ILIMmin variable and equation are obsolete, this is not used anymore.
 In figures 33-27 to 33-29 ILIM-2P_min is used.
 SuggestedRemedy
 Remove ILIMmin equation 33-16.
 Proposed Response Response Status **W**
 PROPOSED REJECT.
 ILIM_min is used on the right axis of Figures 33-28 and 33-29.
 TFTD

Cl 33 SC 33.2.8.7 P 111 L 30 # 215
 Darshan, Yair Microsemi
 Comment Type **TR** Comment Status **D** PSE Power
 1. Equation 33-16 describes the relationship between ILIM_min and Ipeak_max and not between ILIM_min and Ipeak.
 2. Equation 33-16 address ILIM_min during TLIM-2P min time duration only.
 SuggestedRemedy
 1. Change the text "ILIM_min is defined by Equation (33-16)."
 To: "The total current at ILIM-2P_min operating point during TLIM-2P_min is ILIM_min defined by Equation (33-16)."
 2. Change Equation 33-16 from:
 ILIM_min={Ipeak+0.004}A
 To:
 ILIM_min={Ipeak_max+0.004}A
 3. in the "where" list change:
 "Ipeak is defined by Equation (33-9)
 To:
 "Ipeak_max is the maximum value of Ipeak derived from Equation (33-9)"
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.
 TFTD (needs more review)

Cl 33 SC 33.2.8.7 P 113 L 12 # 514
 Stover, David Linear Technology
 Comment Type **TR** Comment Status **D** Pres: Stover2
 I_PSEUT for Type 3, Type 4 PSEs may cause interoperability issues with Type 1, Type 2 PDs.
 SuggestedRemedy
 See stover_02_0916.pdf
 Proposed Response Response Status **Z**
 REJECT.
 This comment was WITHDRAWN by the commenter.
 TFTD
 WFP

Cl 33 SC 33.2.8.8 P 114 L 44 # 441
 Yseboodt, Lennart Philips
 Comment Type **T** Comment Status **D** PSE Power
 "The PSE remains in the IDLE state as long as the average voltage across the pairset is below V Off max."
 Or in the DISABLED state...
 SuggestedRemedy
 "The PSE remains in the IDLE or DISABLED state as long as the average voltage across the pairset is below V Off max."
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.
 TFTD DS

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Cl 33 SC 33.2.8.10 P 115 L 10 # 442
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE Power

"P Con is valid over the range of V Port_PSE-2P defined in Table 33-17. Measurement of P Con should be averaged using any sliding window with a width of 1 s."

This is the only place where Pcon is used. We can simplify it to Pclass and Pclass-2P.

SuggestedRemedy

"Pclass and Pclass-2P are valid over the range of V Port_PSE-2P defined in Table 33-17. Measurements should be averaged using any sliding window with a width of 1 s."

Proposed Response Response Status W

PROPOSED ACCEPT.

See 417

TFTD KB DS

Cl 33 SC 33.2.8.11 P 115 L 23 # 515
 Stover, David Linear Technology

Comment Type E Comment Status D Editorial

"A 100BASE-TX transmitter in a Type 2, Type 3 and Type 4 Endpoint PSEs shall meet the requirements of 25.4.5 in the presence of (l_unb / 2)." has "Type 3 and Type 4" poorly shoehorned.

SuggestedRemedy

Replace text with "A 100BASE-TX transmitter in a Type 2, Type 3, and Type 4 Endpoint PSE shall meet the requirements of 25.4.5 in the presence of (l_unb / 2)."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace text with "A 100BASE-TX transmitter in a Type 2, Type 3, or Type 4 Endpoint PSE shall meet the requirements of 25.4.5 in the presence of (l_unb / 2)."

TFTD FS

Cl 33 SC 33.2.9 P 116 L 20 # 445
 Yseboodt, Lennart Philips

Comment Type E Comment Status D Editorial

"See Annex 33C" refers to Autoclass.

SuggestedRemedy

Remove sentence.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS

Cl 33 SC 33.2.10.1.2 P 118 L 26 # 447
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PSE MPS

PSE DC MPS requirements, there are 3 "blocks" of requirements:

1. A PSE powering a PD over a single pairset
2. A Type 3 or Type 4 PSE powering a single-signature PD over both pairsets
3. A Type 3 or Type 4 PSE powering a dual-signature PD

A dual-signature PD being powered over 2P by a Type 3/4 PSE would fall both under 1 and 3.

SuggestedRemedy

Change "A Type 3 or Type 4 PSE powering a dual-signature PD" to "A Type 3 or Type 4 PSE powering a dual-signature PD over both pairsets"

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS

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Cl 33 SC 33.2.10.1.2 P 118 L 37 # 295
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status D PSE MPS

The PSE requirements on lines 37 to 39, and 52 to 54, and page 119 lines 13 to 16 are the same and appear to contradict eachother. "shall remove power from the PI when DC MPS has been absent for a duration greater than TMPDO." and "shall not remove power from the PI when DC MPS has been present within the TMPS + TMPDO window." Legacy text indicates "The PSE shall not remove power from the port when IPort is greater than or equal to IHold max continuously for at least TMPS every TMPS + TMPDO...". But it also says, "Power shall be removed from the PI when DC MPS has been absent for a duration greater than TMPDO.". The key legacy text uses "...at least TMPS ..." while the new text says "DC MPS has been present ...", which requires the reader to understand that DC MPS is TMPS, but leaves out the at least. This is comparable to = to >=.

SuggestedRemedy

Replace the called-out text, "DC MPS has been present" in all referenced lines with "DC MPS has been present for at least TMPS".

Proposed Response Response Status W

PROPOSED REJECT.

The definition of present is "Iport is greater than or equal to Ihold-2p max continuously for a minimum of TMPS.

The "minimum" takes care of your concern.

TFTD

Cl 33 SC 33.2.10.1.2 P 119 L 20 # 192
 Darshan, Yair Microsemi

Comment Type TR Comment Status X PSE MPS

In my previous work in http://www.ieee802.org/3/bt/public/may16/darshan_10_0516.pdf, I have addressed the PSE dv/dt that affects short MPS. The bottom line is: PSE dv/dt voltage transients caused by ports cross regulations, creates current transient at the amplitude and time duration of the short MPS pulse and can cancel the MPS short pulse and add to it a false current pulse which makes the short MPS operation less reliable. There are several questions resulting from this research:

1. How PSE will address false missing or addition of short MPS pulse?
 Options:
 - a) If it is missing, it should remove power and risking with false disconnect.
 - b) If the PD wants to be OFF but there is false addition of pulse, the PSE will keep the power even if it is false "don't connect power".
 - c) The PSE will decide what to do if it has the information that the distorted short MPS pulse was a result of PSE dv/dt.
2. What to require from a PD to make sure that it is generating a valid MPS pulse under PSE dv/dt conditions?
 - a) Not to require anything. The current spec. suggests using higher MPS current. The problem is that it is counter the objective of low STBY power which short MPSE was meant to achieve.
 - b) Leave it as implementation specifics and not to address it in the spec. May be just adding a note to make the reader aware of the issue?
3. How to address this issue when testing system for compliance?
 Simpler solution was suggested by Chad that is not required new definitions or requirements for PSEs nor PDs. The solution is just to test the PSE for meeting MPS rules at conditions when only single port is operated at a time so PSE dv/dt is not possible due to cross regulation. In this way the true requirements of the spec is tested and we verify that PSE or PD is not cheating... It is clear that the spec is only about a single port.. but it will be good to clarify it in case of multi-port system as we did in other cases in the spec.

SuggestedRemedy

1. Add the following text in the 1. PSE requirements:
 "In case of PSE voltage transient event that cause di/dt current transient at the PD that resultaed with distored MPS pulse, the PSE may decide what action to take (to maintain power or disconnect)if it has the information that the distorted short MPS pulse was a result of PSE dv/dt."
2. Add "Editor Note: To address what are the requirements from PSE, PD and compliance tests when PD short MPS pulse is falsely added or disappears during PSE dv/dt event."

Proposed Response Response Status W

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.5 P 124 L 54 # 452

Yseboodt, Lennart

Philips

Comment Type E Comment Status D PD SD

We used to have two notes below Figure 33-31 (the Type 1/2 PD state diagram).

SuggestedRemedy

Add the following two NOTEs after Figure 33-31:

"NOTE 1--DO_CLASS_EVENT3 creates a defined behavior for a Type 2 PD that is brought into the classification range repeatedly."

"NOTE 2--In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than TClass_PD as defined in Table 33-28."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS

Cl 33 SC 33.3.3.10 P 129 L 1 # 454

Yseboodt, Lennart

Philips

Comment Type T Comment Status X Pres: Yseboodt3

The PD inrush specification is mismatched between the text and the state diagram.

We have now adopted accurate inrush text in 33.3.8.3, the SD should reflect this.

SuggestedRemedy

Adopt yseboodt_03_0916_pdinrushsd.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.9 P 129 L 11 # 210

Darshan, Yair

Microsemi

Comment Type TR Comment Status X Pres: Darshan12

The subject is: Figure 33-32 (PD single signature state diagram), dll_power_type, dll_power_level and the synch with Figure 33-50 which is currently is good only for Type 1 and Type 2.

Background:

PD Type 1/2 state machine:

In page 122 line 45 we have a definition for pse_dll_power_type that is used in PD Type 1 and 2 state machine in page 124 line 30 at the exit from MDI_PWR1.

The pse_dll_power_type is used in the PD power control state diagram (LLDP) Figure 33-50.

So far all is good.

Single Signature PD Type 3/4 state machine:

In page 127 line 11 we have a definition for pse_dll_power_level that should be used in the single-signature PD Type 3 and 4 state machine on page 129 line 11 at the exit from MDI_PWR1 but instead there is pse_dll_power_type there as was in Type 1/2 PD state machine.

The pse_dll_power_type is required in the PD power control state diagram (LLDP) Figure 33-50 but is not defined in the variable list (what is defined is only pse_dll_power_level.

The problems are:

1. For Type 3 and 4 single-signature PD: It needs to be pse_dll_power_level and not pse_dll_power_type.
2. Type 3 and 4 single-signature PD state diagram and variable list should be sync with Figure 33-50 that historically needs pse_dll_power_Type only for Type 1 and 2.
3. We need figure 33-50 to work with Legacy and new single-signature PDs.

SuggestedRemedy

Adopt darshan_12_0916.pdf if available for the meeting. If not,

To add Editor Note to page 129:

"Editor Note: (1) To make changes in Figure 33-50 so it can work with Type 1 and 2 by using the existing variables in Figure 33-50 and work with dll_power_level when it is Type 3 and Type 4 PDs. (2) Type 3 and 4 single-signature PD state diagram and variable list should be sync with Figure 33-50."

Proposed Response Response Status W

TFTD

WFP

See 296

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.10 P 129 L 15 # 31
 Picard, Jean Texas Instruments

Comment Type TR Comment Status X Pres: Yseboodt3

The PD behavior during inrush is not fully described in the state diagram, referring to 33.3.8.3. For example, Single-signature PDs assigned to Class 1, 2, or 3 shall conform to PClass_PD and PPeak_PD within TInrush-2P min. Another example is that it has to meet inrush requirements with the PSE behavior as defined in 33.2.8.5.

SuggestedRemedy

Add an editor's note to review the PD state diagram to cover inrush behavior.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.3.12 P 130 L 24 # 251
 Darshan, Yair Microsemi

Comment Type TR Comment Status D Pres: Darshan9

(This comment corrects similiar comment with error in the file name used for the proposed remedy.)

 Dual-signature state machine need to be updated to support DLL.
 See darshan_09_0916.pdf.

SuggestedRemedy

See darshan_09_0916.pdf for proposed remedy.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.3.12 P 130 L 44 # 456
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PD SD

The Type 3/4 dual-sig state diagram has two variables pd_dll_enabled_modeA and pd_dll_enabled_modeB. Doesn't make sense, DLL can only be enabled or disabled for a complete PD, this doesn't work by Mode.

SuggestedRemedy

- Merge both into pd_dll_enabled.
- Rename all instances of pd_dll_enabled_modeA and pd_dll_enabled_modeB to pd_dll_enabled in the dual-sig state diagram.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD (needs review)

Cl 33 SC 33.3.3.12 P 132 L 32 # 457
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD SD

present_det_sig_modeA:
 Controls presenting the detection signature (see 33.3.4) by the PD over Mode A.
 invalid:A non-valid PD detection signature is to be applied to the link over Mode A regardless of any voltage above V Reset applied to Mode B.
 valid:A valid PD detection signature is to be applied to the link over each pairset over Mode A regardless of any voltage above V Reset applied to Mode B.

The detection behaviour for dual-sig PDs is already defined in 33.3.4. These descriptions duplicate that but with differing details.

SuggestedRemedy

present_det_sig_modeA:
 invalid:A non-valid PD detection signature is to be applied to the link over Mode A.
 valid:A valid PD detection signature is to be applied to the link over each pairset over Mode A.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace with:

present_det_sig_modeA:
 invalid:A non-valid PD detection signature is to be applied to the link over Mode A.
 Valid:A valid PD detection signature is to be applied to the link over Mode A.

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.12 P 132 L 40 # 458
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD SD

present_det_sig_modeB:
 Controls presenting the detection signature (see 33.3.4) by the PD over Mode B.
 invalid:A non-valid PD detection signature is to be applied to the link over Mode B
 regardless of any voltage above V Reset applied to Mode B.
 valid:A valid PD detection signature is to be applied to the link over each pairset over
 Mode B regardless of any voltage above V Reset applied to Mode B.

The detection behaviour for dual-sig PDs is already defined in 33.3.4. These descriptions
 duplicate that but with differing details.

SuggestedRemedy

present_det_sig_modeB:
 invalid:A non-valid PD detection signature is to be applied to the link over Mode B.
 valid:A valid PD detection signature is to be applied to the link over each pairset over
 Mode B.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace with:

present_det_sig_modeB:
 invalid:A non-valid PD detection signature is to be applied to the link over Mode B.
 valid:A valid PD detection signature is to be applied to the link over Mode B.

TFTD YD

Cl 33 SC 33.3.3.12 P 133 L 44 # 278
 Beia, Christian STMicroelectronics

Comment Type E Comment Status D Editorial

VPD_ModeA may be defined better

SuggestedRemedy

Replace:
 Voltage at the PD PI as defined in 1.4.425 over Mode A

with

Voltage at the PD PI as defined in 1.4.425 where the powered pair belongs to Mode A

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace:
 Voltage at the PD PI as defined in 1.4.425 over Mode A

with

Voltage at the PD PI as defined in 1.4.425 where the powered pairs belong to Mode A

TFTD LY

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.12 P 133 L 46 # 279
 Beia, Christian STMicroelectronics

Comment Type E Comment Status D Editorial

VPD_ModeB may be defined better

SuggestedRemedy

Replace:
 Voltage at the PD PI as defined in 1.4.425 over Mode B

with

Voltage at the PD PI as defined in 1.4.425 where the powered pair belongs to Mode B

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Replace:
 Voltage at the PD PI as defined in 1.4.425 over Mode B

with

Voltage at the PD PI as defined in 1.4.425 where the powered pairs belong to Mode B

TFTD LY

Cl 33 SC 33.3.3.14 P 134 L 15 # 459
 Yseboodt, Lennart Philips

Comment Type E Comment Status D PD SD

do_class_timing_modeA returns variable "short_mps".
 This needs to be handled on a per pairset basis.

SuggestedRemedy

Rename "short_mps" to "short_mps_modeA" and rename where needed in the state diagram.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Cl 33 SC 33.3.3.14 P 134 L 20 # 358
 Yseboodt, Lennart Philips

Comment Type E Comment Status D PD SD

do_class_timing_modeB returns variable "short_mps".
 This needs to be handled on a per pairset basis.

SuggestedRemedy

Rename "short_mps" to "short_mps_modeB" and rename where needed in the state diagram.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Cl 33 SC 33.3.3.15 P 135 L 5 # 29
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PD SD

VPD should refer to ModeA

SuggestedRemedy

Replace every occurrence of VPD with VPD_modeA.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Suggest Remedy applies to all of page 135.

TFTD LY

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.15 P 136 L 5 # 297
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X PD SD

The dual-signature state diagram (SD), Figures 33-33 and 33-24, should match the single-signature SD, which will make it more likely that one DLL SD can be used for both PSE versions. For example, state MDI_POWER1_modeA, "pse_dll_power_level_modeA > 1" should be "pse_dll_power_type > 1", and state DLL_ENABLE_modeA, should be "pse_power_type > 1". No differentiation for A and B is required if the power negotiated is for the PD PI total power. Many DS SD need to be fixed, which may change things that affect this remedy.

SuggestedRemedy

Make the provided changes made in the comment and replacing "pse_power_modeX" for Figure 33-33 and for Figure 33-34 where X = A or B; remove all "__modeX" in these figures, and on line 1 of each figure add, "Editor's Note: readers are encouraged to improve this section and better tie this information to section 33.6 DLL." Alternatively, only provide the Editor's note. This comment is related to other comments marked COMMENT-4. This comment should not be considered satisfied until an acceptable solution is provided to address the comment made.

Proposed Response Response Status W

TFTD

(needs review)

See PD_DS_DLL

Cl 33 SC 33.3.3.15 P 136 L 25 # 282
 Beia, Christian STMicroelectronics

Comment Type ER Comment Status X PD SD

Figure 33-33
 pd_dll_enabled is not defined for dual signature PD

SuggestedRemedy

Change:
 "!pd_dll_enabled"
 and
 "pd_dll_enabled"
 respectively to:
 "!pd_dll_enabled_modeA"
 and
 "pd_dll_enabled_modeA"

Proposed Response Response Status W

TFTD

See PD_DS_DLL

Cl 33 SC 33.3.3.15 P 136 L 35 # 359
 Yseboodt, Lennart Philips

Comment Type T Comment Status X PD SD

The dual-sig PD state diagram has states DLL_ENABLE_modeA (and modeB as well). They don't need this. DLL is mandatory for dual-signature, regardless of Class.

SuggestedRemedy

- Remove states DLL_ENABLE_modeA and DLL_ENABLE_modeB
- Add statement "pd_dll_enabled <= TRUE" to the MDI_POWER1_modeA state
- Add statement "pd_dll_enabled <= TRUE" to the MDI_POWER1_modeB state

Proposed Response Response Status W

TFTD

See PD_DS_DLL

Cl 33 SC 33.3.3.15 P 137 L 5 # 30
 Picard, Jean Texas Instruments

Comment Type TR Comment Status D PD SD

VPD should refer to ModeB

SuggestedRemedy

Replace every occurrence of VPD with VPD_modeB.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Suggest remedy applies to all of Figure 33-34.

TFTD LY YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.3.15 P 137 L 11 # 283
 Beia, Christian STMicroelectronics

Comment Type ER Comment Status D PD SD

Figure 33-34
 VPD not defined for dual signature PD

SuggestedRemedy

Change:
 "VPD"
 to:
 "VPD_modeB"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 30

TFTD YD

Cl 33 SC 33.3.3.15 P 138 L 25 # 284
 Beia, Christian STMicroelectronics

Comment Type ER Comment Status X PD SD

Figure 33-34
 pd_dll_enabled is not defined for dual signature PD

SuggestedRemedy

Change:
 "!pd_dll_enabled"
 and
 "pd_dll_enabled"
 respectively to:
 "!pd_dll_enabled_modeB"
 and
 "pd_dll_enabled_modeB"

Proposed Response Response Status W

TFTD

See PD_DS_DLL

Cl 33 SC 33.3.4 P 138 L 46 # 360
 Yseboodt, Lennart Philips

Comment Type E Comment Status D PD Detection

"A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33-32."

At the very least we need to add references to the other state machines.
 What is "a state where it accepts power via the PI" ? I can only imagine this being mdi_power_required.

If so this statement is wrong:

- not required to do valid detect when in IDLE
- not possible to do valid detect when in CLASS
- not allowed to do valid detect when in MARK

SuggestedRemedy

"A PD presents a valid detection signature when it is the DO_DETECTION state as defined in Figure 33-31, Figure 33-32, Figure 33-33, Figure 33-34."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD DS

Cl 33 SC 33.3.4 P 139 L 7 # 363
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Detection

"A PD may indicate the ability to accept power on both pairsets using TLV variable PD 4PID in Table 79-6b or by presenting a valid detection signature on the unpowered pairset, when it is powered over only one pairset."

The last part of the sentence is a hint at Type 1 and Type 2 dual-signature PDs, something we have left out of scope.

It is also in direct conflict with the paragraph above it.

See item b in 33.2.6.7, PSEs are allowed to power such a device on 4P.

SuggestedRemedy

"A PD may indicate the ability to accept power on both pairsets using TLV variable PD 4PID in Table 79-6b."

Proposed Response Response Status W

PROPOSED REJECT.

I believe the intent of the last part of the sentence is to include Type 3 and Type 4 PDs that do this. Type 1 and Type 2 PDs are strictly forbidden from presenting a valid detection signature on one pairset when powered from the other pairset.

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 33 SC 33.3.4 P 139 L 13 # 18
 Jones, Chad Cisco

Comment Type E Comment Status D PD Detection

"The detection signature is a resistance calculated from two voltage/current measurements made during the detection process". Didn't this used to say 'at least two measurements'?

SuggestedRemedy

change: "calculated from two voltage/current measurements"
 to: "calculated from at least two voltage/current measurements"

Proposed Response Response Status Z

REJECT.

This comment was WITHDRAWN by the commenter.

No, it always said "two". The equation only uses two points.

TFTD

CI 33 SC 33.3.6 P 141 L 21 # 373
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Class

"... shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer."

The 'active indication' shall is:

- untestable
- out of scope for an interoperability standard

SuggestedRemedy

"... shall conform to Type 1 PD power restrictions."

Proposed Response Response Status W

PROPOSED REJECT.

This is legacy text and has been debated heavily (from what I have heard).

TFTD

CI 33 SC 33.3.6.2 P 142 L 43 # 519
 Stover, David Linear Technology

Comment Type T Comment Status X PDClass

For Class 8 PDs, P_Class as defined in Table 33-12 does not match P_Class as calculated by Equation 33-2. Specifically, P_Class in 33-2 is ~89.5W with V_Port_PSE (min), R_Chans (max), and P_Class_PD (min).

SuggestedRemedy

In Table 33-24, increase P_Class_PD for single-signature Class 8 PDs from 71.0W to 71.3W.

Proposed Response Response Status W

TFTD

It was 71.3W at one point and we decided to just round it off to 71W. Does anyone object to going back to 71.3W?

CI 33 SC 33.3.6.2 P 143 L 1 # 520
 Stover, David Linear Technology

Comment Type T Comment Status X PD Power

For dual-signature Class 5 PDs, P_Class as defined in Table 33-12 does not match P_Class as calculated by Equation 33-2. Specifically, P_Class in 33-2 is ~44.8W with V_Port_PSE (min), R_Chans (max), and P_Class_PD (min).

SuggestedRemedy

In Table 33-25, increase P_Class_PD for dual-signature Class 5 PDs from 35.5W to 35.6W.

Proposed Response Response Status W

TFTD

CI 33 SC 33.3.6.2 P 143 L 29 # 298
 Schindler, Fred Seen Simply, Broadco

Comment Type ER Comment Status D Editorial

Existing text, "If it chooses to implement short MPS, a PD may set short_mps to ..." may be improved. This change reduces the amount of thinking required to determine if "it" is the PSE or the PD.

SuggestedRemedy

Replace the called-out text with, "If a PD chooses to implement short MPS, it may set short_mps to ..."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.7 P 145 L 1 # 376
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **X** Pres: Yseboodt4
 The section on PSE Type identification has two problems:
 - It is only valid for Type 3 and Type 4, we lost the legacy text
 SuggestedRemedy
 Adopt yseboodt_04_0916_psetypeid.pdf
 Proposed Response Response Status **W**
 TFTD
 WFP

Cl 33 SC 33.3.7 P 145 L 1 # 301
 Schindler, Fred Seen Simply, Broadco
 Comment Type **TR** Comment Status **X** Pres: Yseboodt4
 The description for pse_power_level is not correct or incomplete. The existing text is, "The default value of pse_power_level is 3. After a successful Multiple-Event Physical Layer classification has completed the pse_power_level is set to either 3, 4, 6, or 8. After a successful Data Link Layer classification has completed, the pse_power_level is set to either 3, 4, 6 or 8. The PD resets the pse_power_level to '1' when the PD enters the DO_DETECTION state.". This text only applies to Type 3 and 4 PDs. The first sentence contradicts the last sentence. DLL does not affect the variable and Physical layer always sets it. Dual-signature state diagrams may remove the appending of _modeA or _modeB to pse_power_level, so it is better to address DS using an Editor's note. This comment is related to comments marked COMMENT-4 and COMMENT-5.

SuggestedRemedy
 Replace "The default value of pse_power_level is 3." with "Type 3 and 4 PDs provide a default value of 3 for pse_power_level in the DO_DETECTION state." Delete the sentence, "After a successful Data Link Layer classification has completed, the pse_power_level is set to either 3, 4, 6 or 8. " A comment marked COMMENT-4 already provides a related Editor's Note. Strike the sentence "The PD resets the pse_power_level to '1' when the PD enters the DO_DETECTION state."

Proposed Response Response Status **W**
 TFTD
 WFP

Cl 33 SC 33.3.7 P 145 L 5 # 377
 Yseboodt, Lennart Philips
 Comment Type **T** Comment Status **X** Pres: Yseboodt4
 "The PD resets the pse_power_level to '1' when the PD enters the DO_DETECTION state."
 Wrong. Should be 3.
 SuggestedRemedy
 "The PD resets the pse_power_level to '3' when the PD enters the DO_DETECTION state."
 Possible OBE by yseboodt_04_0916_psetypeid.pdf
 Proposed Response Response Status **W**
 TFTD
 WFP

Cl 33 SC 33.3.7 P 145 L 5 # 521
 Stover, David Linear Technology
 Comment Type **TR** Comment Status **X** Pres: Yseboodt4
 "The PD resets the pse_power_level to '1' when the PD enters the DO_DETECTION state." False. The Type 3 and Type 4 PD reset pse_power_level to 3 in DO_DETECTION. Type 2 PDs do not have a defined variable named pse_power_type, which IS set to 1 in DO_DETECTION. Also (TFTD) why do we have two pse_power_xxx variables?
 SuggestedRemedy
 Replace text with "Type 1 and Type 2 PDs reset the pse_power_type to '1' when the PD enters the DO_DETECTION state. Type 3 and Type 4 PDs reset the pse_power_level to '3' when the PD enters the DO_DETECTION state."
 Proposed Response Response Status **W**
 TFTD
 WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8 P 145 L 41 # 379
 Yseboodt, Lennart Philips
 Comment Type **TR** Comment Status **D** PD Power
 Table 33-28 has an incorrect value for Type 4 overload.
 At Class 8 worst case we have $P_{class_pd-2P} = 1.05 * 71W = 74.55W$, with current = 1.841A.
 The resulting PD voltage is $52 - 6.25 * 1.841 = 40.5V$
 SuggestedRemedy
 Change Table 33-28, item 3, Type 4 value from 39.5 to 40.5
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.
 TFTD YD

Cl 33 SC 33.3.8 P 146 L 8 # 522
 Stover, David Linear Technology
 Comment Type **E** Comment Status **D** PD Types
 "PD Type" for Single-signature PD, Class 0 to 6 is "All"; Type 4 PDs can only be Class 7 or Class 8.
 SuggestedRemedy
 Replace "All" in PD Type column for Single-signature PD, Class 0 to 6 with "1, 2, 3"
 Proposed Response Response Status **W**
 PROPOSED ACCEPT.
 TFTD LY

Cl 33 SC 33.3.8 P 146 L 25 # 523
 Stover, David Linear Technology
 Comment Type **ER** Comment Status **D** PD Power
 PD Type column for dual-signature entries in I_Inrush_PD-2P is incorrect.
 SuggestedRemedy
 Replace PD Type column for "Dual-signature PD, Class 1 to 4" with "3" (is 4); for "Dual-signature PD, Class 5" with "4" (is blank).
 Proposed Response Response Status **W**
 PROPOSED ACCEPT IN PRINCIPLE.
 Replace PD Type column for "Dual-signature PD, Class 1 to 4" with "3" (is 4); for "Dual-signature PD, Class 5" with "4" (is blank).
 Also, replace PD Type column for "Single-signature PD, Class 7 to 8" with "4" (is 3, 4).
 TFTD LY

Cl 33 SC 33.3.8 P 146 L 44 # 524
 Stover, David Linear Technology
 Comment Type **T** Comment Status **X** PD Power
 P_Peak_PD-2P (used in section 33.3.8.5, which references this table) is missing.
 SuggestedRemedy
 Define P_Peak_PD-2P (TFTD).
 Proposed Response Response Status **W**
 TFTD as requested

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8.1 P 148 L 15 # 381
 Yseboodt, Lennart Philips

Comment Type T Comment Status X PD SD

"The behavior of a PD at a voltage outside of V Port_PD-2P is undefined once the PD reaches MDI_POWER1, until V PD falls below V Reset."

Now that we have this text, we can do away with the inelegant MDI_NOPOWER state in the state diagram.

SuggestedRemedy

- From 33.3.3.7 remove variable 'pd_undefined'
- From Figure 33-32 remove state MDI_NOPOWER
- From 33.3.3.12 remove variables 'pd_undefined_modeA' and _modeB
- From Figure 33-33 remove state MDI_NOPOWER_modeA
- From Figure 33-34 remove state MDI_NOPOWER_modeB

Proposed Response Response Status W

TFTD

Cl 33 SC 33.3.8.2.1 P 148 L 37 # 47
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Extended Power

This section states:

"...the PD may consume greater than PClass_PD but shall not consume greater than PClass at the PSE PI."

Problem: Equation 33-2 defines Pclass by Rchan and Pclass_PD. If a PD consumes more than Pclass_PD, it will by definition cause Pclass in equation 33-2 to be exceeded.

SuggestedRemedy

Append the following text to the end of the statement:

..., where PClass is the lesser of: a) the PSEs PClass allocation; and b) the overmargined PClass value in table 33-12."

Proposed Response Response Status W

TFTD

Ken and Lennart to align before meeting.

Cl 33 SC 33.3.8.2.2 P 148 L 47 # 383
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Power

In the section "System stability test conditions during startup and steady state operation" we find:

"When a Type 1, Type 2, single-signature Type 3, or single-signature Type 4 PD is supplied with V Port_PSE-2P min to V Port_PSE-2P max with R Ch (as defined in Table 33-1) in series, it shall operate at PPort_PD , as defined in Table 33-28, with the ripple and noise content as defined in Table 33-28, and with the DC input operating voltage range as defined by Table 33-28."

and

"When a dual-signature PD is supplied with V Port_PSE -2P min to V Port_PSE-2P max with R Ch (as defined in Table 33-1) in series, it shall operate at PPort_PD-2P , as defined in Table 33-28, with the ripple and noise content as defined in Table 33-28, and with the DC input operating voltage range as defined by Table 33-28."

All of this repeats requirements already in Table 33-28, a Table that has a shall associated with it.

Also this doesn't belong in this section anyway.

SuggestedRemedy

Remove both paragraphs from this section.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8.4 P 149 L 17 # 221
 Darshan, Yair Microsemi

Comment Type TR Comment Status X PD Power

The dual-signature part of Figure 33-36 is presenting a dual signature with two completely isolated circuits (loads) connected to mode A and mode B and showing total capacitance Cx+Cy as seen by the PSE.
 However dual signature PDs may be implemented in different ways e.g. using single load at POWER_ON state which result with lower than Cx+Cy value.

SuggestedRemedy

Add the following note below Figure 33-36:
 "The dual-signature part of Figure 33-36 is presenting a dual signature with two completely isolated circuits (loads) connected to mode A and mode B and showing total capacitance Cx+Cy as seen by the PSE.
 However dual signature PDs may be implemented in different ways e.g. using single load at POWER_ON state which result with lower than Cx+Cy value."

Proposed Response Response Status W
 TFTD

Cl 33 SC 33.3.8.3 P 149 L 21 # 385
 Yseboodt, Lennart Philips

Comment Type E Comment Status X PD Power

"The PD shall meet the inrush requirements with the PSE behavior described in 33.2.8.5."

I guess the intent was to say "PD only needs to meet the inrush requirements if the PSE complies to 33.2.8.5".
 Do we really need to say this ? The same applies to nearly every other PD parameter as well.
 Also, the earlier shalls are not conditional upon this one, so it has no effect in its current form.

SuggestedRemedy

Remove "The PD shall meet the inrush requirements with the PSE behavior described in 33.2.8.5."

Proposed Response Response Status W
 TFTD

I know that this sentence was added to make sure that PD implementers are aware of the PSE current capabilities at different voltage levels (something that has caused a great deal of issues in the field).

Cl 33 SC 33.3.8.3 P 149 L 23 # 386
 Yseboodt, Lennart Philips

Comment Type E Comment Status D Editorial

"Editor's Note: These paragraphs have changed as a result of MR1277 and further work. Do not change this paragraph without consulting the request of MR1277."

This whole section has been revamped and the concern of MR1277 has been addressed.

SuggestedRemedy

Remove note.

Proposed Response Response Status W
 PROPOSED ACCEPT.

TFTD (Chad, are you OK with this?)

Cl 33 SC 33.3.8.3 P 149 L 30 # 460
 Yseboodt, Lennart Philips

Comment Type TR Comment Status D PD Power

"If a PD has a larger C Port or C Port-2P value, then the PD shall limit the input inrush current such that I Inrush_PD max and I Inrush_PD-2P max, as defined in Table 33-28, are met."

Very true, but also redundant to the requirement a few paragraphs above:
 "PDs shall draw less than I Inrush_PD and I Inrush_PD-2P from T Inrush-2P min until T delay-2P min."

SuggestedRemedy

Remove the "If a PD has a larger..." sentence.

Proposed Response Response Status W
 PROPOSED ACCEPT.

TFTD

The PD actually needs to limit inrush current so that Pclass_PD is met after Tinrush_min (50ms).

The inrush requirements were written to make sure this is true.

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 33 SC 33.3.8.4.1 P 151 L 2 # 48
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Extended Power

The statement:

"...the peak power shall not exceed PClass at the PSE PI for more than TCUT-2P min, as defined in Table 33-17 and with 5% duty cycle."

Needs clarification of PClass. Three interpretations are possible: Equation 33-2, Table 33-12, or the PClass level provided by the connected PSE.

SuggestedRemedy

Append the following to the end of the statement:

", where PClass is the lesser of: a) the PSE's PClass allocation; and b) the overmargined PClass value in table 33-12."

Proposed Response Response Status W

TFTD

Ken and Lennart to align before meeting.

CI 33 SC 33.3.8.4.1 P 151 L 2 # 49
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Extended Power

This section addresses peak power for Class 6 and 8 extended power. It mirrors section 33.3.8.4, however it is missing a Peak Power value.

The average power (Pport_PD) in extended mode is limited to PClass at the PSE. Ppeak_PD limits use a fixed multiplier (1.05 x PClass_PD). Ppeak_PD is a fixed limit at the PD and is variable with respect to PClass at the PSE (due to changes in channel loss). For interoperability and clarity, the Peak Power limit should remain at the same factor of 1.05, referenced to the PD PI.

SuggestedRemedy

Append the text below to the paragraph ending on Pg 151, Ln 2.

Peak operating power shall not exceed 1.05 x Port_PD max.

Proposed Response Response Status W

TFTD

Ken and Lennart to align before meeting.

CI 33 SC 33.3.8.5 P 151 L 31 # 50
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X PD Power

Figures 33-37, 33-38, and 33-39 show PD upperbound templates. These are also described as operating masks, and a normative shall states the PDs must operate below these upperbound templates.

The figures are valid up to TCut-2P min for a single peak rising above the PClass_PD power level. The figures are not valid for multiple peaks that are shorter duration than TCut-2P min (see 5% duty cycle in 33.3.8.4).

SuggestedRemedy

Change the NOTE as follows and put it under each respective template (replacing the existing notes where they appear):

NOTE - Figure 33-## applies to a single peak which exceeds the PClass_PD power value.

Proposed Response Response Status W

TFTD (needs review)

CI 33 SC 33.3.8.5 P 151 L 32 # 51
 Bennett, Ken Sifos Technologies, In

Comment Type E Comment Status D PD Power

The templates show a second upperbound step after Tcut-2P min. This step is the power that a peak pulse must fall below before PSE TCut timing is reset.

After a Peak lasting TCut-2P min ends, the instantaneous power must stay below the second step for 950msecs. Peaks lasting less than TCut-2P min may exceed the second step after droppin below the PClass_PD power level.

The always-valid portion of the second step is the transition at TCut-2P-min.

SuggestedRemedy

For clarity, shorten the duration of the second step in Figures 33-37, 33-38, 33-39 to 1/4 or 1/8 of their existing length.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

I believe what Ken would like is to shorten (in time) the horizontal line that extends along the Pclass_PD(-2P) line.

If correct, make the change. If incorrect, Ken to comment.

TFTD FS LY CJ YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8.5 P 153 L 3 # 52
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Extended Power

The Class 6 and 8 extended template and Equation 33-30 impose peak power values of $I_{peak} \cdot V_{pse}$.

PDs are not required to "know" V_{pse} : without V_{pse} , this is an unknown limit.

Another submitted comment suggested "1.05 x $P_{port_PD\ max}$ " as a P_{peak} limit for extended mode. If it was accepted, it should appear here as well.

SuggestedRemedy

Replace $I_{peak} \cdot V_{pse}$ with "1.05 x $P_{port_PD\ max}$ ".

Proposed Response Response Status W

TFTD

Ken and Lennart to align before meeting.

Cl 33 SC 33.3.8.9 P 155 L 24 # 467
 Yseboodt, Lennart Philips

Comment Type T Comment Status D PD Power

"When $V_{Port_PD-2P\ max}$ is applied across the PI at either polarity specified on the conductors of either Mode A or Mode B according to Table 33-19, the voltage measured across the PI for the other Mode with a 100 kOhm load resistor connected shall not exceed $V_{bfd\ max}$ as specified in Table 33-28."

Note: legacy text!

This 'shall' only applies when precisely 57.0V is applied. In essence, the shall does not exist.

SuggestedRemedy

TFTD

"When any voltage between 0V and $V_{Port_PD-2P\ max}$ is applied across the PI at either polarity specified..."

or

"When V_{Port_PD-2P} is applied across the PI at either polarity specified..."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD

Cl 33 SC 33.3.8.10 P 155 L 30 # 53
 Bennett, Ken Sifos Technologies, In

Comment Type T Comment Status X Pres: Bennett1

Section 33.3.8.10 describes a test set-up to meet Icon-2P and Icon-2P_unb, which are necessary for interoperability.

The Normative "Shall" refers to a test set-up (derived from models) as the condition under which Icon-2P and Icon-2P_unb must be met. There are deficiencies in this approach which can result in interoperability problems.

SuggestedRemedy

See Bennett_01_0916.pdf

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.8.10 P 155 L 34 # 213
 Darshan, Yair Microsemi

Comment Type T Comment Status X Pres: Darshan7

This comment is marked "PDPI_P2P"
 33.3.8.10 needs some updates. All my comments related to 33.3.8.10 are shown with editing marks on page 2 in darshan_07_0916.pdf.

SuggestedRemedy

All my comments related to 33.3.8.10 are shown with editing marks on page 2 in darshan_07_0916.pdf.

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8.10 P 155 L 40 # 242
 Darshan, Yair Microsemi
 Comment Type E Comment Status D Editorial
 Error in the link to Figure 33-39. Need to be 33-40.
 SuggestedRemedy
 Change from "Figure 33-39"
 To: "Figure 33-40".
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD CJ

Cl 33 SC 33.3.8.10 P 155 L 42 # 243
 Darshan, Yair Microsemi
 Comment Type T Comment Status X Pres: Darshan7
 In the text:
 "Rsource_min and Rsource_max represent the Vin source common mode effective resistance that consists of the PSE PI components (RPSE_min and RPSE_max as specified in 33.2.8.4.1, VPort_PSE_diff as specified in Table 33-17 and the channel resistance). Common mode effective resistance is the resistance of two conductors of the same pair and their other components connected in parallel including the effect of VPort_PSE_diff. IA and IB are the pair currents of pairs with the same polarity. See Annex 33A.5 for design guide lines for meeting the above requirements."
 There is some missing information that clarifies the text and some redundant information.

SuggestedRemedy
 Change from:
 "Rsource_min and Rsource_max represent the Vin source common mode effective resistance that consists of the PSE PI components (RPSE_min and RPSE_max as specified in 33.2.8.4.1, VPort_PSE_diff as specified in Table 33-17 and the channel resistance). Common mode effective resistance is the resistance of two conductors of the same pair and their other components connected in parallel including the effect of VPort_PSE_diff. IA and IB are the pair currents of pairs with the same polarity. See Annex 33A.5 for design guide lines for meeting the above requirements."
 TO:
 "Rsource_min and Rsource_max represent the Vin source common mode effective resistance that consists of the PSE PI components (RPSE_min and RPSE_max as specified in 33.2.8.4.1, VPort_PSE_diff as specified in Table 33-17, channel resistance and RPAIR_PD_min , RPAIR_PD_max specified in 33A.5. See Annex D for derivation of Rsource_min and Rsource_max. Common mode effective resistance is the resistance of two conductors of the same pair and their other components (that are forming Rsource) connected in parallel including the effect of the system total pair to pair voltage difference. IA and IB are the pair currents of pairs with the same polarity."

Proposed Response Response Status W
 TFTD
 WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.3.8.10 P 155 L 46 # 222

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan7

(See darshan_07_0916.pdf page 4 for editing marks on 33A.5.)

Annex 33A.5 needs updates:

1. Equation 33A-4 was not implemented correctly. It was written in reverse order.
2. Some text clarification was missing.
3. Figure 33A-4 was update for editorials and missing information.

SuggestedRemedy

See page 4 in darshan_07_0916.pdf for proposed remedy.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.8.10 P 156 L 9 # 244

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan4

See darshan_04_0916.pdf for the correct drawing.

In figure 33-40, all Resistors are marked as Rsource_max which is incorrect.

It should start with Rsource_min from top, and then Rsource_max, Rsource_min and Rsource_max in this order.

See darshan_04_0916.pdf for the correct drawing.

SuggestedRemedy

See darshan_04_0916.pdf for the correct drawing.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.3.9 P 157 L 16 # 470

Yseboodt, Lennart Philips

Comment Type TR Comment Status X PD MPS

There is a interoperability issue for dual-signature PDs connected to Type 1/2 PSEs.

The Iport_mps-2P is 8mA (min) for the PD, but can be up to 10mA for the PSE.

SuggestedRemedy

Two options.

Simple: Change Table 33-30, IPort_MPS-2P to 0.010 A

Complex: Change Table 33-30, such that depending on short_mps_modeA and short_mps_modeB the current is 8mA or 10mA

Proposed Response Response Status W

TFTD

my vote: change to 10mA

Cl 33 SC 33.3.9 P 157 L 29 # 302

Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status D PD MPS

The existing table note can be improved to make PD designers aware of other concerns that may affect PDs using low-MPS. PSEs have a noise allowance covered in Table 33-17 item 4, that permit 0.5Vpp at 500 Hz, which could null the PD MPS current. The PSE noise value is only around 0.7% of the PI voltage so the noise allowance is not likely to be lowered.

SuggestedRemedy

Replace the legacy note text "resistance RCh)" with "resistance RCh) or the PSE power feeding ripple and noise covered in Table 33-17".

Proposed Response Response Status W

PROPOSED REJECT.

The note there already gives guidance to PD designers that other factors need to be taken in consideration when using MPS pulsing. I believe the new note only confuses the manner more.

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.4.5 P 163 L 48 # 529
 Stover, David Linear Technology
 Comment Type ER Comment Status D Editorial
 "This AC voltage can be ripple from the power supply (Table 33-17, item 3)". Actually, item 4.
 SuggestedRemedy
 Correct reference to item 4.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD FS LY

Cl 33 SC 33.4.9.1 P 168 L 9 # 536
 Flatman, Alan LAN Technologies
 Comment Type E Comment Status D Editorial
 ISO/IEC 11801: 2002 does not include cabling for 10GBASE-T which is listed as an MDI type in this subclause. Cabling for 10GBASE-T is included in ISO/IEC 11801: Edition 2.1 2008 and will be contained in ISO/IEC 11801: Edition 3 which is currently at DIS stage.
 SuggestedRemedy
 change reference to ISO/IEC 11801: Edition 2.1 2008 or ISO/IEC 11801: Edition 3.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD CJ

Cl 33 SC 33.4.9.1.4 P 170 L 22 # 537
 Flatman, Alan LAN Technologies
 Comment Type E Comment Status D Editorial
 ISO/IEC 11801: 2002 does not include 10GBASE-T cords which are listed in this subclause. 10GBASE-T cords are included in ISO/IEC 11801: Edition 2.1 2008 and will be contained in ISO/IEC 11801: Edition 3 which is currently at DIS stage.
 SuggestedRemedy
 change reference to ISO/IEC 11801: Edition 2.1 2008 or ISO/IEC 11801: Edition 3.
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD CJ

Cl 33 SC 33.5 P 172 L 26 # 211
 Darshan, Yair Microsemi
 Comment Type TR Comment Status X Pres: Law1
 Clause 33.5 Management function requirements is missing many of type 3 and Type 4 registers. It is a problem to add the missing registers to 33.5 due to used up address space. It is suggested to:
 1.rename clause 33.5 title in line 21 to "33.5 Type 1 and Type 2 Management function requirements"
 2. Add new sub clause: "33.X Type 3 and Type 4 Management function requirements"
 3.Add minimum control and status register set for Type 3 and 4 features that will be equitant management capability to the MDIO and will have future expansion capabilities as well. The protocol will be implementation specific since MDIO is not practical and the spec allows equivalent way to do it. See page 172 lines 29-32.
 SuggestedRemedy
 1.Rename clause 33.5 title in line 21 to "33.5 Type 1 and Type 2 Management function requirements"
 2. Add new sub clause: "33.X Type 3 and Type 4 Management function requirements"
 3.Adopt darshan_09_0916.pdf if available for the meeting. If not ready for the meeting add to the new clause 33.X the following Editor Note:
 "Editor Note: "Editor Note: Add minimum control and status register set for Type 3 and 4 features that will be equitant management capability to the MDIO and will have future expansion capabilities as well. The protocol will be implementation specific since MDIO is not practical and the spec allows equivalent way to do it."
 Proposed Response Response Status W
 TFTD
 WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.5 P 172 L 26 # 335
 Law, David HPE

Comment Type TR Comment Status X Pres: Law1

As acknowledged in subclause 33.1.2, as an optional non-data entity, DTE Power via MDI does not appear in the seven layer model. Regardless, as illustrated in Figures 33-1 and 33-2, it interfaces to the medium at the same point as the PHY, and these figures also show the PSE and PD function adjoining the PHY. Perhaps because of this, or perhaps for other reasons, Clause 33 has provided the option for the PSE functions to be 'below' the optional xMII, as for PHYs. This is through the optional support of the MDIO interface, and associated registers, defined in subclause 33.5.

It seems however that implementations of PSE functions don't ever implement the MDIO interface and instead use other approaches. From the perspective of an implementer it doesn't matter if IEEE 802.3 specifies registers in subclause 33.5 since they are only mandatory if '...the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO) ...'. Hence if the MDIO interface isn't implemented on the PSE function, the registers don't need to be implemented, only something equivalent.

But there would seem to be no point specifying these registers moving forward if they are never used, as that would just be unnecessary work. And there would appear to be an additional work for IEEE P802.3bt as there is no space left in the Clause 22 register space, hence we'd have to look at how to use the Clause 45 register space instead.

So far in IEEE 802.3 we've only defined an optional compatibility interface, in this case the xMII (see subclause 1.1.3.2), for access to the status and control information to the PHY. We've not defined one for the MAC, MAC Control and upper sublayers, instead only abstract services interfaces. Hence access to control and status in these sublayers has always been in an implementation specific way. Maybe it is time to add DTE Power via MDI to this list.

SuggestedRemedy

Consider either deprecating, or even removing, subclause 33.5 'Management function requirements'. For all DTE Power via MDI attributes in Clause 30 remove the 'If a Clause 22 MII or Clause 35 GMII is present, then this will map to ...' text so that the attributes behaviours will then only make reference to subclause, state diagrams and functions as is the case for all MAC, MAC Control and other upper sublayers related attributes. State diagram variables with 'mr_' prefixes should have the text related to register bits removed and should be renamed by removing the text 'mr_'.

I have requested presentation time at the 2016 September interim to make a presentation in support of this comment.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.5.1.2 P 175 L 32 # 98
 Zimmerman, George CME Consulting, Aqua

Comment Type TR Comment Status X Pres: Law1

Need to specify new classes (5-8 and Autoclass) in PD class bits.

SuggestedRemedy

Change 1 0 1 to Invalid Class or Type 4 PD, Change 1 1 0 to Class 5, and 1 1 1 to Class 6. Change last sentence of 33.5.1.2.10 to read "The combination "1 0 1" indicates that either an invalid class was read, or the PD is a Type 4 PD, with Class 7, 8 or autoclass has been determined (see 45.2.7b.4)." Add Clause 45 into the draft, and allocate a new PSE status register in clause 45 space at 45.2.7b.4, after 45.2.7b.3, as inserted by IEEE P802.3bu-201x, to include 2 bits (0:1) for 00 = PD Class 1-6, 01 = PD Class 7, 10 = PD Class 8, and 11 = Autoclass, and the rest reserved.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.5.1.2 P 175 L 50 # 143
 Grow, Robert RMG Consulting

Comment Type TR Comment Status X Pres: Law1

The Editor's note highlights a technical incompleteness that should have disqualified the draft from progressing to WG ballot. While it is admirable to highlight input being needed from WG members, this should have been done prior to ballot.

SuggestedRemedy

Unfortunately, I don't think I have a solution for you, but you need one prior to the next recirculation. All that occurs to me is to deprecate the use of Clause 22 registers, require the use of Clause 45 registers (possibly including the mapped Clause 22 registers, and get the extra registers and bits in the Clause 45 register space.

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.5.1.2 P 175 L 51 # 209
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Law1

The Editor note need to be updated as for the list of features we need to support.

SuggestedRemedy

Change from:

"Editor's Note: Table 33-22 requires new fields to support new Types and features. Reviewers are encouraged to provide the required definitions. Status register bits are used up, and clause 22 address space is used up as well. Contributions requested as to how to expand status, at a minimum to report Class 8 PD and Autoclass."

To:

"Editor's Note: Table 33-22 requires new fields to support new Types and features. Reviewers are encouraged to provide the required definitions. Status register bits are used up, and clause 22 address space is used up as well. Contributions requested as to how to expand status, at a minimum to report Class 5-8 PDs, dual/single-signature PD detected, PSE is using Type 3 or 4 electrical parameters and Autoclass."

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.5.1.2 P 175 L 51 # 1
 McDermott, Thomas Fujitsu

Comment Type TR Comment Status X Pres: Law1

The editor's note refers to TABLE 33-22. This appears to be the wrong table for defining additional Types and Features. Should it refer to TABLE 33-39? It is not clear whether the draft, as written, can operate properly without these additional fields being defined. If it cannot, then the fields and mechanisms need to be defined before the draft can be approved.

SuggestedRemedy

Define method and fields before progressing the draft further if the draft is inoperable as currently written.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.6 P 177 L 40 # 304
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X DLL

A DLL subject matter expert should add text covering dual-signature PDs. A state diagram may be required and a LLDP attribute map would also then be required.

SuggestedRemedy

Add on line 40, "Editor's Note: readers are encouraged to improve the DLL to incorporate dual-signature PDs." This comment should not be considered satisfied until an acceptable solution is provided to address the comment made.

Proposed Response Response Status W

TFTD

I don't think adding editor's notes pointing out technical incompleteness are a good idea at this point. We need actual solutions.

Cl 33 SC 33.6 P 177 L 40 # 214
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan11

33.6 Data Link Layer classification need to be updated in order to:

1. support dual-signature PD.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, PD DLL power state maching and its variable list and figure 33-50 mainly and maybe Figure 33-49 as well.
3. In addition clause 33.6 needs to be in sync with PD single and dual signature state machines and their variable list.

SuggestedRemedy

Adopt darshan_11_0915.pdf if ready for the meeting. If not, add the following editor note to the begining of clause 33.6:

"Editor Note: 33.6 Data Link Layer classification need to be updated in order to:

1. support dual-signature PD.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, PD DLL power state maching and its variable list and figure 33-50 mainly and maybe Figure 33-49 as well.
3. sync 33.6 with PD single and dual signature state machines and their variable list."

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.6 P 177 L 40 # 239
 Darshan, Yair Microsemi

Comment Type **TR** Comment Status **X** DLL

Type 3 and Type 4 single signature state machine is not complete and contradicts DLL power management in clause 33.6.

The main issues are:

1. Figure 33-50 is not supporting Type 3 and Type 4 single-signature PDs. (need to support pse_dll_power_level and pse_dll_power_type)
2. Duplicate variables used in 33.6 and 33.3.3.7 (e.g pse_dll_power_level)

SuggestedRemedy

Add "Editor Note: clause 33.6 and 33.3.3.7 need to be in sync.

The following issues need to be addressed:

1. Figure 33-50 is not supporting Type 3 and Type 4 single-signature PDs. (need to support pse_dll_power_level and pse_dll_power_type)
2. Duplicate variables used in 33.6 and 33.3.3.7 (e.g pse_dll_power_level)."

Proposed Response Response Status **W**

TFTD

I don't think adding editor's notes pointing out technical incompleteness are a good idea at this point. We need actual solutions.

Cl 33 SC 33.6.3.2 P 179 L 18 # 305
 Schindler, Fred Seen Simply, Broadco

Comment Type **TR** Comment Status **X** Pres: Schindler

Variable parameter_type is determined only by Type 1 and 2 function set_parameter_type, therefore it will only have values 1 and 2. Variable pd_allocated_power is not assigned anywhere and is required to determine PSE_INITIAL_VALUE.

SuggestedRemedy

The solution is provided in schindler_3bt_01_0916.

Proposed Response Response Status **W**

TFTD

WFP

Cl 33 SC 33.6.3.2 P 179 L 19 # 475
 Yseboodt, Lennart Philips

Comment Type **T** Comment Status **X** Pres: Yseboodt2

The constant PSE_INITIAL_VALUE needs to be initialized, but the way this is done is different for Type 1/2 and Type 3/4.

Since we want to avoid splitting the DLL state diagrams, and this is (for now) the only variable that is causing trouble, we should initialize it differently depending on PSE Type.

SuggestedRemedy

Adopt yseboodt_02_0916_pseinitialvalue.pdf

Proposed Response Response Status **W**

TFTD

WFP

Cl 33 SC 33.6.3.3 P 180 L 43 # 309
 Schindler, Fred Seen Simply, Broadco

Comment Type **TR** Comment Status **D** DLL

Variable parameter_type is determined only by Type 1 and 2 function set_parameter_type, therefore it will only have values 1 and 2. The value of this variable is not used by the Type 3 and 4 PSE state diagram (it is a don't care).

SuggestedRemedy

Delete text for values 3 and 4.
 Modify legacy sentence,

"A control variable output by the PSE state diagram (Figure 33-13) used by a Type 2, Type 3, or Type 4 PSE to choose operation with Type 1, Type 2, Type 3, or Type 4 PSE output PI electrical requirement parameter values defined in Table 33-17."

to read

"A control variable output by the Type 1 and 2 PSE state diagram (Figure 33-13) used by a Type 2 PSE to choose operation with Type 1 or Type 2 PSE output PI electrical requirement parameter values defined in Table 33-17."

Proposed Response Response Status **W**

PROPOSED ACCEPT.

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.6.3.3 P 181 L 41 # 311
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status D

The values are missing from variable pse_power_level.

SuggestedRemedy

Add "

Values:

3: The PSE has allocated Class 3 power (default).

4: The PSE has allocated Class 4 power.

5: The PSE has allocated Class 5 power.

6: The PSE has allocated Class 6 power.

7: The PSE has allocated Class 7 power.

8: The PSE has allocated Class 8 power."

Note that the phrase "or less is not used for class 3 because PSE are required to provide at least class 3 power before DLL is operational.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 312

TFTD YD

Cl 33 SC 33.6.3.5 P 183 L 33 # 56
 Tremblay, David Hewlett Packard Enter

Comment Type E Comment Status D DLL

The PSE power control state diagram makes use of setting local_system_change as a condition when transitioning from the RUNNING to the PSE POWER REVIEW state; however, the condition never gets reset. For clarity, the local_system_change condition should be reset when exiting the MIRROR UPDATE state.

SuggestedRemedy

Replace the UCT condition exiting the MIRROR UPDATE state between lines 33 and 34 with !local_system_change.

Proposed Response Response Status W

PROPOSED REJECT.

The UCT is the logic that defines when to transition from MIRROR UPDATE to RUNNING. It cannot be used to reset a variable, that must be done inside a state.

TFTD

Cl 33 SC 33.6.5 P 186 L 4 # 316
 Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X Pres: Yseboodt1

An autoclass subject matter expert should add text covering this topic. A state diagram may be required and a LLDP attribute map would also then be required. This comment is related to other comments marked COMMENT-2.

SuggestedRemedy

Add on line 5, "Editor's Note: readers are encouraged to improve Autoclass information by adding text and state diagrams as appropriate." This comment should not be considered satisfied until an acceptable solution is provided to address the comment made.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.6.5 P 186 L 4 # 476
 Yseboodt, Lennart Philips

Comment Type TR Comment Status X Pres: Yseboodt1

DLL Autoclass section is missing content.

SuggestedRemedy

Adopt yseboodt_01_0916_dllautoclass.pdf

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33.6.5 P 186 L 13 # 54
 Bennett, Ken Sifos Technologies, In

Comment Type E Comment Status X Pres: Yseboodt1

Table 33-60 describes transactions using "LLDP Frame". All other data link classification transactions in the standard use the more specific terms: "Power via MDI TLV", "LLDPDU", or "TLV Frame".

There isn't a formal "LLDP Frame" definition in Clause 33, whereas "TLV Frame" is specifically defined in section 33.6.1.

SuggestedRemedy

Change all instances of "LLDP Frame" in table 33-60 to:

"TLV Frame" or "LLDPDU"

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.7 P 186 L 24 # 538
 Goergen, Joel Cisco

Comment Type T Comment Status X Environmental

See George Zimmerman comments - needs environmental and safety section

SuggestedRemedy

See George Zimmerman comments - needs environmental and safety section

Proposed Response Response Status W

TFTD

I do not see any comments from George that cover this. Is there a presentation?

Cl 33 SC 33.8.2 P 189 L 1 # 158
 Abramson, David Texas Instruments

Comment Type TR Comment Status D PICS

The PICS section of the draft has not been updated to include Type 3 and Type 4.

SuggestedRemedy

Update PICS section to include all new requirements.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Has anyone volunteered for PICS duty for BT? Craig?

TFTD

Cl 33 SC 33.8.2.4 P 190 L 13 # 183
 Anslow, Pete Ciena

Comment Type T Comment Status X PICS

The status of item *MIDA is "MID:O:2".

The meaning of the colon is given in 21.6.2:

<item>: simple-predicate condition, dependent on the support marked for <item>

So, the "MID:O" part means optional for a midspan PSE.

The ":2" part seems to violate the syntax. When there is a number (as per 1 or 3) there have to be at least two rows containing that number.

SuggestedRemedy

Please explain the meaning of "MID:O:2" or correct it.

Proposed Response Response Status W

TFTD (needs review/expert)

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79 P 208 L 1 # 157
 Laubach, Mark Broadcom Limited

Comment Type T Comment Status D Editorial

I see scattered editing instruction and a lot of unchanged text. Similar to previous comment on Clause 30: Clause 79 of .3bt should only contain the subclauses and associated text for what is being changed in existing Clause 79 Section 6. If nothing is being changed, it doesn't need to be in this draft. Only the first subclause headers for each level leading up to the new/changed subclauses, the subclause header of interest, the editing instructions, and the added/changed text for the specific sections.

SuggestedRemedy

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 124

TFTD YD

Cl 79 SC 79 P 208 L 1 # 4
 Carlson, Steven HSD/Robert Bosch

Comment Type ER Comment Status D Editorial

It appears the entire subclause from the base document has been copied into Clause 79. It is difficult to follow the change instructions and to determine what has actually changed.

SuggestedRemedy

Follow the 802.3 editorial guidelines for changes.
http://grouper.ieee.org/groups/802/3/WG_tools/editorial/requirements/words.html

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 124

TFTD YD

Cl 79 SC 79 P 208 L 1 # 124
 Hajduczenia, Marek Charter Communicatio

Comment Type ER Comment Status D Editorial

Clause 79 already exists in 802.3-2015 and only modified (edited) portions should be presented, including Table 79-1, Table 79-4, etc. The unchanged text should be removed

SuggestedRemedy

Per comment. Remove all unchanged text and subclauses from Clause 79 and leave only changed text / tables / content with appropriate editorial comments for such changes

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Cl 33 SC 79 P 208 L 2 # 237
 Darshan, Yair Microsemi

Comment Type TR Comment Status D LLDP

If PSE issues only single class event due to power limitations, it can't know what is the PD physical advertised class.

At this point nobody has this information.

Now if PSE has the power budget, and PD wants for more through DLL to increase power, he can't do it since DLL do not have the physical PD class.

As a result, we need to add to TLVs information, the PD physical class requirements.

SuggestedRemedy

Add in clause 79: "Editor Note: If TLVs doesnt contain information regarding the PD physical advertized class, to add it."

Proposed Response Response Status W

PROPOSED REJECT.

We need to stop adding Editor's notes that show technical incompleteness. They will just draw more ire from the WG. Please submit actual remedies for this.

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.1 P 208 L 5 # 542
McClellan, Brett Marvel

Comment Type ER Comment Status D Editorial

Clause 79 contains sections unchanged from the base standard. They should not be included within this amendment.

SuggestedRemedy

Remove sections 79.1 to 79.2. Section 73.1 remove the unchanged text and unchanged rows in Table 79-1. Remove sections 79.3.1 to 79.3.1.4. Section 79.3.2 remove the unchanged text. Section 79.3.2.1 remove the unchanged text and unchanged rows in Table 79-3 and insert editing instructions for 79-3. In section 79.3.2.2 provide editing instructions. Remove sections 79.3.2.3, 79.3.2.4 and Table 79-4. Remove sections 79.3.2.4.2 to 79.3.2.4.3. Sections 79.3.2.5 and 79.3.2.6 remove the unchanged text. Remove 79.3.2.7.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 124

TFTD YD

Cl 33 SC 79 P 211 L 1 # 195
Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan13

Clause 79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements, need to be updated with more TLV information needed for the current spec and optional features to support dual-signature PDs.

SuggestedRemedy

Adopt recommendations of darshan_13_0916.pdf if available for the meeting. If not ready, add to clause 79: "Editor Note: To verify if TLVs contain all the information required to DLL to support dual-signature DLL state machine in Figure 33-50 including optional information for future needs."

Proposed Response Response Status W

TFTD

WFP

Cl 79 SC 79.3.2.6 P 214 L 40 # 318
Schindler, Fred Seen Simply, Broadco

Comment Type TR Comment Status X LLDP

Draft 1.4, comment 160 resulted in using the same starting value for power values. Previously, DLL values were permitted to start a 0 while LLDP values were required to start at 1. The change made all values start at 1. Reserved TLV fields are normally zero but this value is allowed for values that have meaning. Using zero rather than one for all starting references would have them all start at the same value and permit a means for the PD to signal to the PSE that power should be removed. If other believe this change is acceptable (discussion are in progress now) then 79.3.2.6e Request power down could be eliminated in the TLV.

SuggestedRemedy

Replace all one (1) values with zero (0).
page 214, line 15, and 40.
page 179, line 47.
page 180 lines 3, 10, 20, 27, 31,
Delete section 79.3.2.6e on page 217.
On page 211 correct the TLV, delete the "Power down" value and adjust TLV information string length from 18 to 17. This comment is related to other comments marked COMMENT-1.

Proposed Response Response Status W

TFTD (needs review)

Cl 79 SC 79.3.2.6a P 215 L 6 # 125
Hajduczenia, Marek Charter Communicatio

Comment Type E Comment Status D Editorial

If Table 79-6a is a new table, there is no need to use any underline in the table to indicate inserted text

SuggestedRemedy

Remove all underline from Table 79-6a. The same applies for Table 79-6b

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

CI 79 SC 79 P 216 L 29 # 248

Darshan, Yair Microsemi

Comment Type TR Comment Status D LLDP

Comment

Table 79-6b System setup value field bit 0, value/meaning:

1 = PD requested power applies to Mode A pairset

0 = PD requested power applies to Mode B pairset

The problems are:

1. System wise we need to know WITHIN single transaction what is the PD requested power for Mode A pairset and for Mode B pairset simultaneously.

1.1 It looks that this bit covers operation on 2-pairs only.

1.2 Currently it says that "PD requested power applies to Mode A pairset or Mode B pairset but no information about what both pairsets requested power are.

1.3 4-pairs operation is not covered

SuggestedRemedy

1. Add additional bit/s to indicate dual-signature PD or Single-signature PD. Use bits 7:4 reserved bits to indicate:

-Dual-signature Type 3 (use reserved codes "1011").

-Dual-signature Type 4 (use reserved codes "1010").

-The other Type 3 and 4 PDs in bits 7:4: add the "single-signature Type x PD"

2. Split Table 79-5 to Mode A and Mode B and A+B. when Mode A and B are used, Total value is set to zero.

3. Update Figure 79-3, PD requested power value for the final number of octets .

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change bits for Power Type as follows:

1 0 1 1 = Type 4 dual-signature PD

1 0 1 0 = Type 4 single-signature PD

1 0 0 1 = Type 4 PSE

1 0 0 0 = Type 3 dual-signature PD

0 1 1 1 = Type 3 single-signature PD

0 1 1 0 = Type 3 PSE

The rest of the changes are TFTD.

TFTD FS

CI 79 SC 79.3.2.6b.2 P 216 L 34 # 477

Yseboodt, Lennart Philips

Comment Type T Comment Status D LLDP

The PD 4PID bit allows a PD to indicate if it supports powering over both Modes simultaneous or not.

To be consistent with 33.2.6.7 we should indicate the specific cases where the PD may actually set this.

SuggestedRemedy

Append:

"This field shall be set to '1' when the power type is Type 3 PD or Type 4 PD."

after:

"This field shall be set to 0 when the power type is PSE."

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS CJ DS

CI 79 SC 79.3.2.6b.3 P 216 L 37 # 478

Yseboodt, Lennart Philips

Comment Type T Comment Status D LLDP

The PD PI bit in the System setup field is not in line with the classification scheme we have.

For single-signature PDs, the communicated Class is for the entire PD.

For dual-signature PDs, the communicated Class on a pairset is for that pairset.

This bit seems to indicate that choice is possible when it is not.

SuggestedRemedy

TFTD.

Unless we can give meaning to this bit, we should remove it.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 320

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.3.2.6b.3 P 216 L 37 # 320
Schindler, Fred Seen Simply, Broadco

Comment Type T Comment Status D LLDP

The System setup value field "PD PI" is no longer required because a dual-signature classification mechanism was added--see PD Mode selection. The solution provided should be discussed as recent changes to dual-signature text could require this bit with some minor text modifications.

SuggestedRemedy

Replace Table 79-6b bit- 2 function and value/meaning fields with, "Reserved" and "Transmit as zero. Ignore on receive.", respectively. Delete section 79.3.2.6b.3.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS YD

Cl 33 SC 79.3.2.6d P 217 L 19 # 232
Darshan, Yair Microsemi

Comment Type TR Comment Status D LLDP

The text says:
"Using the Autoclass field to trigger a new Autoclass measurement allows a PD to change maximum power consumption."
In addition Table 796d tries to specify some "handshake" parameters.

I believe the definitions are incomplete and may cause issues.

- a)It is not clear who is initiating the request for new Autoclass measurement?
- b)What is the timing sequence?
- c)When to raise power?
- d)When to measure?
- e)Where is the final Acknowledge?
- F)The flow is missing.

SuggestedRemedy

Add "Editor Note: The timing and state flow is missing for the case when triggering new Autoclass measurements.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Remove "Annex 33C" from autoclass description (line 19)

Cl 33 SC 79.3.7.1 P 220 L 5 # 233
Darshan, Yair Microsemi

Comment Type TR Comment Status X LLDP

Table 79-6f - PD measurements
All measurements need to be for pairset A and B separately for accurate measurement. Example: dual-signature dual load will have different voltages at the PD input over the modes.
Same for currents, energy, accuracy etc.

SuggestedRemedy

Add "Editor Note: Split Table 79-6f to Mode A and Mode B to have separate field."

Proposed Response Response Status W

TFTD

Cl 79 SC 79.3.7.1 P 220 L 6 # 63
Ran, Adee Intel

Comment Type T Comment Status X LLDP

"(decimal value of bits)" is meaningless here. A bit field that carries a value typically encodes that value to a binary representation unless stated otherwise. The number is not decimal or binary, the base only affects the text representation.

Also applies to the next two bit fields.

SuggestedRemedy

Either delete "(decimal value of bits)" or change it to "(encoded as unsigned binary)", in all occurrences

Proposed Response Response Status W

TFTD (needs review)

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.3.7.1 P 220 L 16 # 64
 Ran, Adee Intel

Comment Type T Comment Status X LLDP

"VPort_PD-2P = (decimal value of bits) mV" is an awkward way of describing the value or meaning of this bits. Also, a voltage value is not "decimal", only the text representation has a base.

I assume the measured value is rounded down or to the nearest mV and the result is encoded.

This applies to many other occurrences of "decimal value of bits" in this amendment. I am aware of two occurrences in the base document, but this amendment adds a lot more.

SuggestedRemedy

Change this one to
 "VPort_PD-2P / 1 mV, rounded down and encoded as unsigned binary"
 or
 "VPort_PD-2P in mV units, rounded down and encoded as unsigned binary"

(or rounded up or whatever is intended)

Change other occurrences in a similar style (with appropriate units and resolution).

Proposed Response Response Status W

TFTD (needs review)

Cl 79 SC 79.3.7.3 P 222 L 3 # 68
 Ran, Adee Intel

Comment Type TR Comment Status X LLDP

It is not clear from this description how this value should be set or interpreted. Is it a completely implementation dependent field? Does a number lower than 1000 indicate power is cheap (and if so, what should be done)? Does a very high number mean power is about to go out?

SuggestedRemedy

Clarify the intent. If meaning of this field is implementation dependent please state it.

Proposed Response Response Status W

TFTD

Cl 79 SC 79.3.7.3 P 222 L 14 # 67
 Ran, Adee Intel

Comment Type E Comment Status X LLDP

"= decimal value of bits" does not add any clarity here

SuggestedRemedy

delete these words

Proposed Response Response Status W

TFTD

Cl 79 SC 79.3.7.4 P 222 L 20 # 69
 Ran, Adee Intel

Comment Type TR Comment Status X LLDP

Does "should" here mean it is only a recommendation? Is it OK to have more than one?

Also applies to 79.3.2.7, although it is in the base document.

SuggestedRemedy

Change to "shall" unless there is no problem with having more than one.

Proposed Response Response Status W

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.4.2 P 224 L 35 # 345
 Law, David HPE

Comment Type TR Comment Status D LLDP

Table 79-8 'IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references' lists a number of new attributes in the 'LLDP Local System Group managed object class attribute' column for the 'Power via MDI' TLV that have not been defined in Clause 30.

SuggestedRemedy

Add the following attributes to the 'LLDP Power via MDI Local Package (conditional)' package in Table 30-7 as well as definitions for each attribute as subclauses of subclause 30.12.2.1 'LLDP Local System Group attributes'.

- aLldpXdot3LocPowerClassx
- aLldpXdot3LocPowerTypex
- aLldpXdot3Loc4PID
- aLldpXdot3LocPDPI
- aLldpXdot3LocPSEMaxAvailPower
- aLldpXdot3LocPSEAutoclassSupport
- aLldpXdot3LocAutoclassCompleted
- aLldpXdot3LocAutoclassRequest
- aLldpXdot3LocPowerDownRequest

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Definitions are needed.

TFTD

Cl 79 SC 79.4.2 P 225 L 23 # 346
 Law, David HPE

Comment Type TR Comment Status D LLDP

Table 79-8 'IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references' lists a number of new attributes in the 'LLDP Local System Group managed object class attribute' column for the 'Power via MDI Measurements' TLV that have not been defined in Clause 30.

SuggestedRemedy

[1] Add a new 'LLDP Power via MDI measurement Local Package (conditional)' package to Table 30-7.

[2] Add the following attributes to the new 'LLDP Power via MDI measurement Local Package (conditional)' package.

[3] Add definitions for each of the following attribute as subclauses of subclause 30.12.3.1 'LLDP Local System Group attributes'.

- aLldpXdot3LocPDMeasVoltageSupport
- aLldpXdot3LocPDMeasCurrentSupport
- aLldpXdot3LocPDMeasEnergySupport
- aLldpXdot3LocPDMeasurementSource
- aLldpXdot3LocPDMeasurementVoltage
- aLldpXdot3LocPDMeasurementCurrent
- aLldpXdot3LocPDMeasurementEnergy
- aLldpXdot3LocPSEMeasVoltageSupport
- aLldpXdot3LocPSEMeasCurrentSupport
- aLldpXdot3LocPSEMeasEnergySupport
- aLldpXdot3LocPSEMeasurementSource
- aLldpXdot3LocPSEMeasurementVoltage
- aLldpXdot3LocPSEMeasurementVoltage
- aLldpXdot3LocPSEMeasurementCurrent
- aLldpXdot3LocPSEMeasurementEnergy
- aLldpXdot3LocPSEPowerPriceIndex

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Definitions are needed.

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.4.2 P 226 L 32 # 347
 Law, David HPE

Comment Type TR Comment Status D LLDP

Table 79-9 'IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references' lists a number of new attributes in the 'LLDP Remote System Group managed object class attribute' column for the 'Power via MDI' TLV that have not been defined in Clause 30.

SuggestedRemedy

Add the following attributes to the 'LLDP Power via MDI Remote Package (conditional)' package in Table 30-7 as well as definitions for each attribute as subclauses of subclause 30.12.3.1 'LLDP Remote System Group attributes'.

- aLldpXdot3RemPowerClassx
- aLldpXdot3RemPowerTypex
- aLldpXdot3Rem4PID
- aLldpXdot3RemPDPI
- aLldpXdot3RemPSEMaxAvailPower
- aLldpXdot3RemPSEAutoclassSupport
- aLldpXdot3RemAutoclassCompleted
- aLldpXdot3RemAutoclassRequest
- aLldpXdot3RemPowerDownRequest

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Definitions are needed.

TFTD

Cl 79 SC 79.4.2 P 227 L 23 # 348
 Law, David HPE

Comment Type TR Comment Status D LLDP

Table 79-9 'IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references' lists a number of new attributes in the 'LLDP Remote System Group managed object class attribute' column for the 'Power via MDI Measurements' TLV that have not been defined in Clause 30.

SuggestedRemedy

- [1] Add a new 'LLDP Power via MDI measurement Remote Package (conditional)' package to Table 30-7
- [2] Add the following attributes to the new 'LLDP Power via MDI measurement Remote Package (conditional)' package.
- [3] Add definitions for each of the following attribute as subclauses of subclause 30.12.3.1 'LLDP Remote System Group attributes'.

- aLldpXdot3RemPDMeasVoltageSupport
- aLldpXdot3RemPDMeasCurrentSupport
- aLldpXdot3RemPDMeasEnergySupport
- aLldpXdot3RemPDMeasurementSource
- aLldpXdot3RemPDMeasurementVoltage
- aLldpXdot3RemPDMeasurementCurrent
- aLldpXdot3RemPDMeasurementEnergy
- aLldpXdot3RemPSEMeasVoltageSupport
- aLldpXdot3RemPSEMeasCurrentSupport
- aLldpXdot3RemPSEMeasEnergySupport
- aLldpXdot3RemPSEMeasurementSource
- aLldpXdot3RemPSEMeasurementVoltage
- aLldpXdot3RemPSEMeasurementVoltage
- aLldpXdot3RemPSEMeasurementCurrent
- aLldpXdot3RemPSEMeasurementEnergy

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Definitions are needed.

TFTD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 79 SC 79.5.2.1 P 228 L 15 # 127
 Hajduczenia, Marek Charter Communicatio
 Comment Type ER Comment Status D Editorial
 Changes to 79.5.2.1 are not really marked in any way at this time - it is not clear what was added / deleted.
 SuggestedRemedy
 Please update 79.5 (PICS for Clause 79) to show only changes (additions / deletions) and not show all PICS for Clause 79 with unmarked changes
 Proposed Response Response Status W
 PROPOSED ACCEPT.
 TFTD LY

Cl 33A SC 33A.3 P 233 L 14 # 114
 Hajduczenia, Marek Charter Communicatio
 Comment Type E Comment Status D Editorial
 Seems that subclause numbering is off by 2
 SuggestedRemedy
 Change 33A.3 to 33A.1 and propagate through Annex 33A
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 33A.1 is in the base document. Editor to renumber Annex 33A correctly.
 Does 33A.2 exist somewhere?
 TFTD LY

Cl 33A SC 33A.3 P 233 L 16 # 71
 Ran, Adeo Intel
 Comment Type TR Comment Status D Annex
 Seems like a normative requirement in an informative annex. Also in other subclauses of 33A.
 SuggestedRemedy
 Make this annex normative?
 Proposed Response Response Status W
 PROPOSED REJECT.
 These are cabling requirements and this annex was written in a way to not include normative requirements (no shalls).
 This may be able to be done in a better way.
 TFTD

Cl 33A SC 33A.3 P 233 L 16 # 113
 Hajduczenia, Marek Charter Communicatio
 Comment Type TR Comment Status D Annex
 The term "Types" is not defined
 SuggestedRemedy
 Please consider specyfing what the particular meaning of "Types" is indended - PSE-D types or something altogether different
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Change "Types" to "PSE Types"
 TFTD LY

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33A.3 P 233 L 26 # 324

Shariff, Masood

CommScope

Comment Type TR Comment Status D Annex

Incorrect definition of resistance unbalance within a pair.

SuggestedRemedy

Change:

Rmax is the resistance of the channel conductor with the highest resistance
Rmin is the resistance of the channel conductor with the lowest resistance

To:

Rmax is the resistance of the pair conductor with the highest resistance
Rmin is the resistance of the pair conductor with the lowest resistance

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD FS YD

Cl 33A SC 33A.5 P 234 L 11 # 75

Ran, Adee

Intel

Comment Type TR Comment Status D Annex

Inconsistent units. $1,750 \times R_{Pair_PD_min} + 0,080$, all quantified later as Ohms, but $R_{Pair_PD_min}$ is already in Ohms.

SuggestedRemedy

Change all equations to include Ohm units for the constants, remove the Ohm subscript.

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD LY

Cl 33A SC 33A.5 P 234 L 11 # 76

Ran, Adee

Intel

Comment Type E Comment Status D Editorial

It would be clearer if the class-dependent numbers were placed in a table, and the inline equation that appears below (line 18) used instead.

SuggestedRemedy

Use alpha and beta in the equation, add a table for alpha and beta per class.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Editor is very fond of tables, he would be glad to implement.

TFTD LY

Cl 33 SC 33A.5 P 234 L 11 # 205

Darshan, Yair

Microsemi

Comment Type TR Comment Status X Pres: Darshan7

(See page 4 in darshan_07_0916.pdf)

Equation 33A-4 was implemented wrongly since Catania meeting.
the 4 equations appears in revers order.

The classes appears in the correct order.

It should be according to:

http://www.ieee802.org/3/bt/public/oct15/darshan_01_1015_Rev001.pdf
(Variable names in D2.0 are correct, DO NOT CHANGE IT)

SuggestedRemedy

(See corrected equation in page 4 in darshan_07_0916.pdf.)

Change only the Equations order as follows:

$R_{pair_PD_max} = 2.200 * R_{pair_PD_min} + 0.125$ For PD Type 3 class 5

$R_{pair_PD_max} = 2.010 * R_{pair_PD_min} + 0.105$ For PD Type 3 class 6

$R_{pair_PD_max} = 1.800 * R_{pair_PD_min} + 0.080$ For PD Type 4 class 7

$R_{pair_PD_max} = 1.750 * R_{pair_PD_min} + 0.080$ For PD Type 4 class 8

Proposed Response Response Status W

TFTD

WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33A **SC 33A.5** **P 234** **L 17** # **117**
 Hajduczenia, Marek Charter Communicatio
Comment Type ER **Comment Status D** *Editorial*
 Incorrect use of "will" in "stringent requirement will be needed"
SuggestedRemedy
 Change to "stringent requirement is needed"
 Please review the use of key words in the whole draft, includign "will", "must", etc. - see Style Manual
Proposed Response **Response Status W**
 PROPOSED ACCEPT.
 TFTD LY CJ

Cl 33 **SC 33A.5** **P 234** **L 21** # **229**
 Darshan, Yair Microsemi
Comment Type TR **Comment Status X** *Pres: Darshan7*
 (See page 4 in darshan_07_0916.pdf for editing marks)
 In the following text:
 "RPair_PD_max and RPair_PD_min represent PD common mode input effective impedance of pairs of the same polarity. The effective resistance Rn is the measured voltage Veff_pd_n, divided by the current through the path as described below and as shown in the example in Figure 33A-4, where n is the pair number."
 1. Mixed use of "resistance" and "impedance". Use only resistance for contintency.
 2. The common mode effective resistance is not sufficiently defined as done for Rsource (PSE) in 33.3.8.10 . Only how to measure it is defined.
SuggestedRemedy
 (See page 4 in darshan_07_0916.pdf for editing marks)
 Chane lines 21-24 from:
 "RPair_PD_max and RPair_PD_min represent PD common mode input effective impedance of pairs of the same polarity. The effective resistance Rn is the measured voltage Veff_pd_n, divided by the current through the path as described below and as shown in the example in Figure 33A-4, where n is the pair number."
 To:
 "RPair_PD_max and RPair_PD_min represent PD common mode input effective resistance of pairs of the same polarity. Common mode effective resistance is the resistance of two conductors of the same pair and their other components connected in parallel including the effect of PD pair-to-pair voltage difference of pairs with the same polarity (e.g. Veff_pd1-Veff_pd3 as shown in Figure 33A-4). The common mode effective resistance Rn is the measured voltage Veff_pd_n, divided by the current through the path as described below and as shown in the example in Figure 33A-4, where n is the pair number."
Proposed Response **Response Status W**
 TFTD
 WFP

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33A.5 P 234 L 28 # 228
 Darshan, Yair Microsemi

Comment Type E Comment Status X Pres: Darshan7

(See page 4 in darshan_07_0916.pdf for editing marks)
 Figure 33A-4 in Annex 33A.5 contains the resistors R1, R2, R3 and R4 that their index numbers should be subscripted as in their equations in page 235 lines 3-7.

SuggestedRemedy

(See page 4 in darshan_07_0916.pdf for editing marks)
 In Figure 33A-4, subscript the index number of R1, R2, R3 and R4.

Proposed Response Response Status W

TFTD

WFP

Cl 33A SC 33A.4 P 234 L 36 # 531
 Stover, David Linear Technology

Comment Type ER Comment Status D Editorial

Figure 33A-4 labels for "R_pair_PD_max" and "R_pair_PD_min" are jumbled.

SuggestedRemedy

Relabel R2 to "R_pair_PD_min" and R3 to "R_pair_PD_max".

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

Cl 33B SC 33B P 237 L 2 # 79
 Ran, Adee Intel

Comment Type TR Comment Status D PICS

Normative annex, but no PICS?

SuggestedRemedy

Add PICS listing the normative requirements

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Need PICS editor...

TFTD LY

Cl 33B SC 33B.1 P 237 L 8 # 118
 Hajduczenia, Marek Charter Communicatio

Comment Type ER Comment Status D Editorial

No subclause numbers

SuggestedRemedy

Please add subclause numbers in Annex 33B

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

There are annex numbers, there is just a bunch of text and a drawing before you get to the first one, 33B.1 (line 50).

Editor to renumber Annex 33B to put introductory material into 33B.1 and increment all other subclause numbers.

TFTD YD

Cl 33B SC 33B P 237 L 15 # 532
 Stover, David Linear Technology

Comment Type T Comment Status X Pres: Stover1

"The details for derivation of R_load_max and R_load_min, which are composed of compliant channel and PD effective resistances, can be found in Annex 33D." This draft does not include an Annex 33D.

SuggestedRemedy

May be OBE by stover_01. If not, TFTD what to do with Annex 33D.

Proposed Response Response Status W

TFTD as requested

WFP

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC Annex 33B P 237 L 16 # 250
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan6

(See darshan_06_0916.pdf)

Annex 33B directs the reader to Annex 33D to find important informative data to how Rload_min/max where derived and other parts that are pair to pair related. This Annex is missing and should be added as planned.

Annex D is needed since all the parts of pair to pair unbalance are spread all over the spec and it is hard to see the whole picture. I find it very useful to have short summary that show the whole spec explained in short in 1.5 pages and it was planned to be there long time ago. Annex D content was reviewed many times in the original contribution (see the reference at the end) and base on it, the whole spec was built.

SuggestedRemedy

See proposed remedy in darshan_06_0916.pdf for Annex D.

Proposed Response Response Status W

TFTD

WFP

Cl 33B SC 33B P 237 L 16 # 77
 Ran, Adeel Intel

Comment Type TR Comment Status D

Annex 33D doesn't seem to exist.

SuggestedRemedy

Add the required details here or conjure the missing annex...

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 532

TFTD YD

Cl 33 SC Annex 33B P 237 L 16 # 193
 Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan6

(See darshan_06_0916.pdf)

Annex 33B directs the reader to Annex 33D to find important informative data to how Rload_min/max where derived. This Annex is missing and should be added as planned.

SuggestedRemedy

See proposed remedy in darshan_06_0916.pdf for Annex D.

Proposed Response Response Status W

TFTD

WFP

Cl 33B SC 33B.1 P 237 L 16 # 119
 Hajduczenia, Marek Charter Communicatio

Comment Type TR Comment Status D

"can be found in Annex 33D" - said Annex does not exist

SuggestedRemedy

Either add the missing Annex or revise the text to eliminate reference to non-existing Annex

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

OBE by 532

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC ANNEX 33B P 237 L 18 # 201

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan7

(See editing marks on page 5 in darshan_07_0916.pdf)
 In the text "A compliant unbalanced load, Rload, consists of the channel (cables and connectors) and the PD effective resistances."

Rload is actually Rload_min and Rload_max as discussed in Annex 33B.
 In addition for improved clarity, to tie Rload with Rchan and RPair_PD.

SuggestedRemedy

(See editing marks on page 5 in darshan_07_0916.pdf)

Change:
 "A compliant unbalanced load, Rload, consists of the channel (cables and connectors) and the PD effective resistances."

To:

"A compliant unbalanced load, Rload_min and Rload_max consists of the channel (cables and connectors), PD effective resistances and PSE PI effective resistance. See Annex D.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC Annex B P 237 L 18 # 253

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan7

Annex B needs some updates.
 See darshan_07_0916.pdf pages 5-8 for editing marked document.

SuggestedRemedy

See proposed updates in darshan_07_0916.pdf pages 5-8 for editing marked document.

Proposed Response Response Status W

TFTD

WFP

Cl 33B SC 33B P 237 L 22 # 78

Ran, Adeo Intel

Comment Type E Comment Status X Pres: Darshan7

Equation 33-14 defines R_PSE_max. The sentence is not clear.

The next paragraph seems to repeat the same idea.

SuggestedRemedy

Change
 "the relationship between PSE PI Equation (33-14) and Rload_min and Rload_max"
 to
 "the relationship between effective resistances at the PSE PI (Equation (33-14)) and Rload_min and Rload_max"

Consider merging the first sentence of the next paragraph into this one.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33.B.1 P 238 L 30 # 44

Trowbridge, Steve Nokia

Comment Type E Comment Status D Editorial

Several sloppy elements in Figure 33B-2 - the vertical lines at the left between Vdiff1 and Vport_PSE and between Vport_PSE and Vdiff2 are composed of multiple line segments that don't line up. Several of the lines that are supposed to meet in the figure cross over

SuggestedRemedy

Zoom in close and tidy up the figure

Proposed Response Response Status W

PROPOSED ACCEPT.

TFTD YD

IEEE P802.3bt D2.0 4-Pair PoE Initial Working Group ballot comments

Cl 33 SC 33B.1 P 238 L 30 # 204

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan3

Figure 33B-2:

1. The drawing looks like broken on the left side at the connections to Vport_pse, Vdiff1 and Vdiff2.
2. The arrows marking the point of measuring Veff1, Veff1, Veff3 and Veff4 are not sufficiently clear where they are pointing. Follow the original drawing darshan_03_0916.pdf for the intent.

SuggestedRemedy

Editor to:

1. Fix the broken connection in Figure 33B-2. See reference in darshan_03_0916.pdf.
2. To align the arrows to the correct position as exactly as shown in darshan_03_0916.pdf.

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC 33B.4 P 240 L 37 # 252

Darshan, Yair Microsemi

Comment Type TR Comment Status X Pres: Darshan7

(This comment is identical to other comment in which only file name was corrected.)

(see editing marks on page 8 in darshan_07_0916.pdf)

"ICon_2P_unb and Equation (33-14) are specified for total channel common mode pair resistance from 0.1 ohm to 12.5 ohm and worst case unbalance contribution by a PD. When the PSE is tested for channel common mode resistance less than 0.1 ohm, i.e. 0 ohm < Rchan < 0.1 ohm, the PSE shall be tested with (Rload_min - Rchan) and (Rload_max - Rchan) to meet ICon-2P-unb requirements and RPSE_min and RPSE_max conformance to Equation (33-14)."

In the above text it is about Rchan-2P which range from 0.2 ohm to 12.5 ohm.

SuggestedRemedy

(See editing marks on page 8 in darshan_07_0916.pdf)

In 33B.4:

1. Replace all "0.1 ohm" with "0.2 ohm".
2. Replace "Rchan" with "Rchan-2P".

Proposed Response Response Status W

TFTD

WFP

Cl 33 SC Annex 33C P 241 L 14 # 231

Darshan, Yair Microsemi

Comment Type TR Comment Status X Annex

Annex 33c objective is to supply informative data regarding the timing relationships between detection and connection check as function of CC_DET_SEQ variable options. After reviewing it, it seems to supply also information regarding if classification must be done in parallel when dual-signature PD is detected and Class_4PID_mult_events_sec is TRUE which is not necessarily correct. Staggered classification can be done regardless if it is single or dual signature PD and staggered classification can be done regardless if it is Class_4PID_mult_events_sec is TRUE or FALSE.

In addition, in all drawings, PWRUP starts at the same time while in dual-signature or even single signature, PWR_UP can be done in different times.

SuggestedRemedy

Update drawing to address the following points:

- a) In dual-signature classification can be done in parallel or in staggered way. See example in figure 33C-2, 33C-5 that classification is in parallel and can be also staggered. Or add note saying "The drawing show one option to classification and POWER_ON timing. Staggered classification and POWER_ON can be done."
- b) Scan all drawing in Annex 33C and repeat the fix if required.

Proposed Response Response Status W

TFTD

Yair and Miklos, please work offline before the meeting to fix this. We can present your solution when we get to this comment.