Interoperability vs Inrush and C_{Port}

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Problem Statement
802.3bt D1.6 Inrush Requirements

- Conflicting PSE/PD POWER_UP requirements…
  - Do not address complexities of simultaneous, staggered POWER_UP (2P inrush vs 4P inrush)
  - Include *informative* combinations of PD inrush cap and load current that…
    - –Exceed PSE guaranteed minimum inrush requirements
    - –Are unnecessarily narrow in scope
  - **Are not interoperable**
- Is there a better way to describe inrush?

Charge is the Currency of Inrush

7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	See 33.2.8.5, max value definition in Figure 33–26
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			0.800	0.900	4	See 33.2.8.5, max value definition in Figure 33–26. See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.
9	Inrush time per pairset	$T_{Inrush-2P}$	s	0.050	0.075	All	See 33.2.8.5.

- Current is Charge (Q) per Time:
  - $I = Q / T$
- Since I_{Inrush} and T_{Inrush} are defined, Q_{Inrush} is also defined.
  - $Q_{Inrush} = I_{Inrush} * T_{inrush}$
- Therefore, the PD is guaranteed a minimum amount of **total charge** during inrush.
  - The PD may store it in a bulk cap:
    - $Qcap = (C_{port} * V_{PSE})$
  - Or it may be used by the load:
    - $Qload = (I_{load} * T_{inrush})$

$$\mathbf{Q_{Inrush} > (C_{port} * V_{PSE}) + (I_{load} * T_{inrush})}$$

PSE Minimum Guaranteed *Total* Charge during POWER_UP SS PD Class 0 – 4 (Type 1, Type 2 PD)

From 802.3-2012:

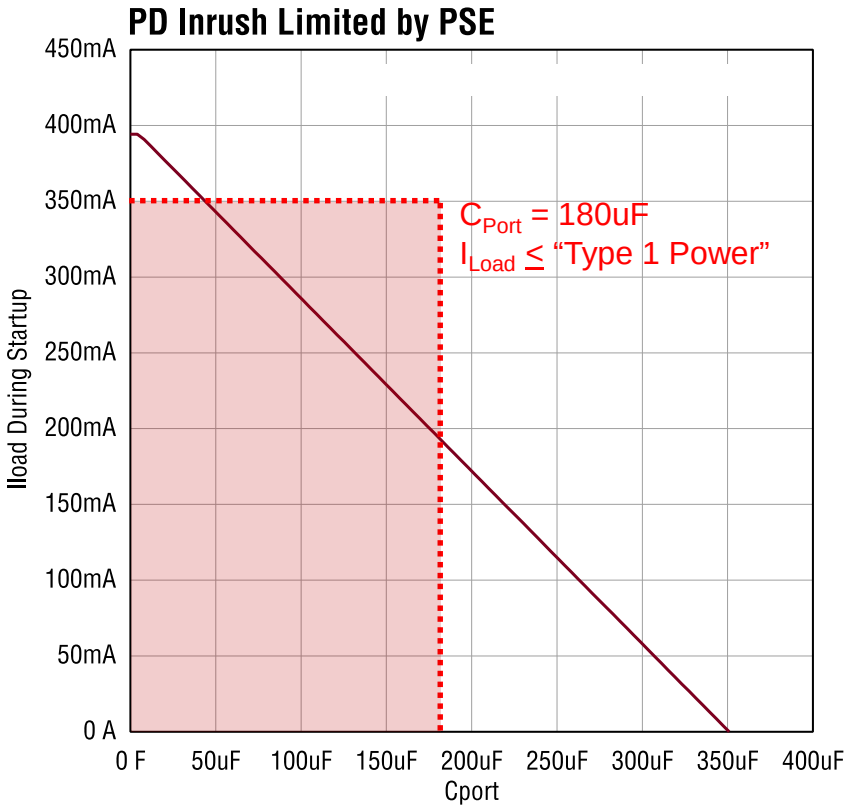
33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99 % of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180\ \mu F$, as specified in Table 33–11.

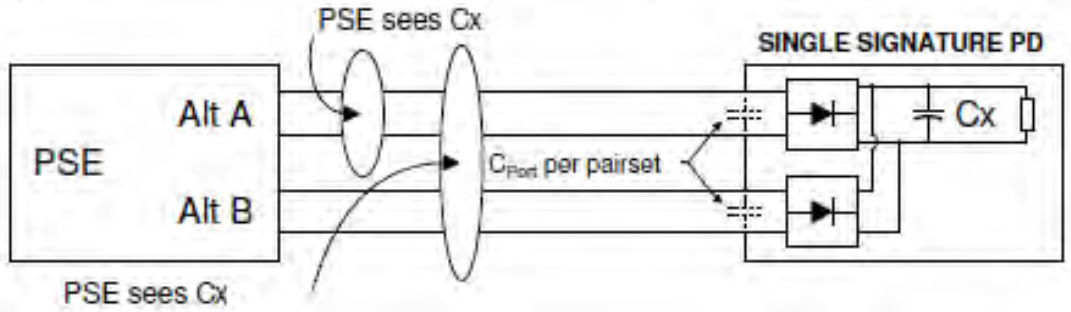
If $C_{Port} \geq 180\ \mu F$, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.



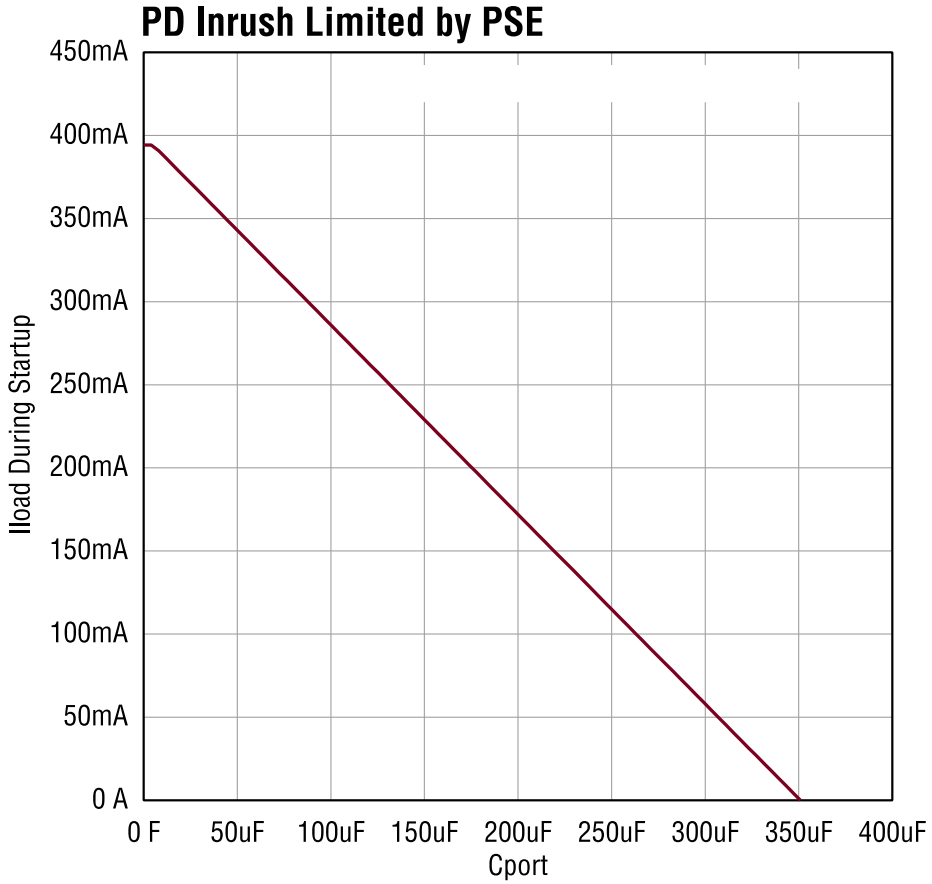
- Type 1 and Type 2 PDs do not follow a simple "PSE minimum guaranteed charge" model
- **Do not change legacy behavior**
- **Maintain text of 802.3-2012 for Type 1 and Type 2 inrush requirements**

PSE Minimum Guaranteed *Total* Charge during POWER_UP SS PD Class 5 - 6

7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class					
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	See 33.2.8.5, max value definition in Figure 33–26
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			0.800	0.900	4	See 33.2.8.5, max value definition in Figure 33–26. See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.



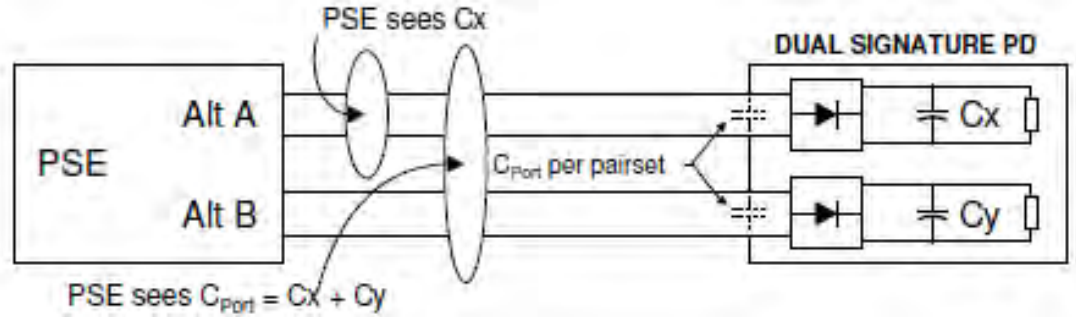
$I_{Inrush,min}$	$T_{inrush-2p,min}$	$Q_{Inrush,min}$	$V_{PSE,max}$
400mA	50ms	20mC	57V



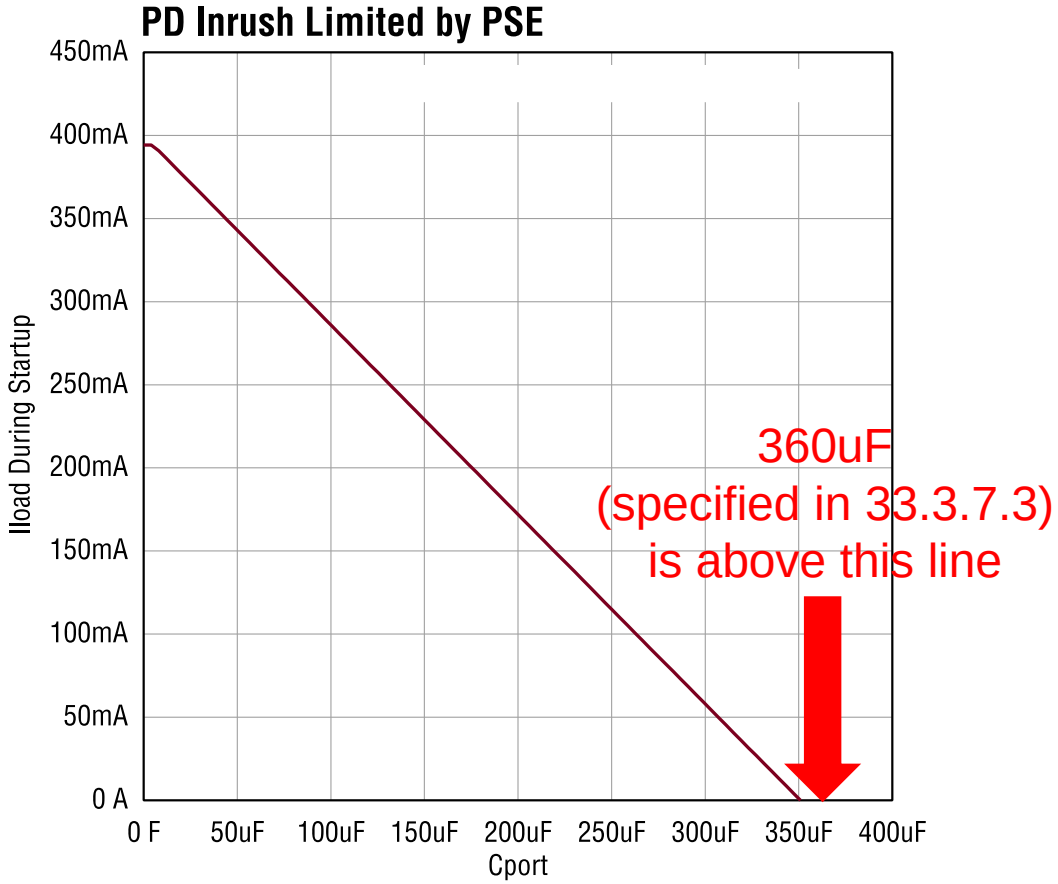
$$I_{load} < [20mC - (C_{port} * 57V)\ ]/\ 50ms$$

PSE Minimum Guaranteed *Total* Charge during POWER_UP
DS PD Class 1 - 4

7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	See 33.2.8.5, max value definition in Figure 33–26
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			0.800	0.900	4	See 33.2.8.5, max value definition in Figure 33–26. See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.



$I_{Inrush,min}$	$T_{inrush-2p,min}$	$Q_{Inrush,min}$	$V_{PSE,max}$
400mA	50ms	**20mC**	57V



$$I_{load} < [20mC - (C_{port} * 57V)] / 50ms$$

PSE Minimum Guaranteed *Total* Charge during POWER_UP
SS PD Class 7 - 8, DS PD Class 5

33.2.8.5.1 $I_{Inrush-2P}$ minimum and I_{Inrush} minimum requirements

A Type 4 PSE, when connected to a single signature PD with assigned Class 7 or Class 8, may optionally implement a minimum $I_{Inrush-2P}$ and I_{Inrush} lower than defined in Table 33–17, but not less than 0.15A and 0.4A respectively. When a Type 4 PSE is connected to a single-signature PD with assigned Class 7 or Class 8 and uses a lower $I_{Inrush-2P}$ and I_{Inrush} than those defined in Table 33–17, it shall successfully power up a single-signature PD comprised of a parallel combination of C_{Port} per pairset as defined in 33.3.7.3 and a Class 2 load within $T_{Inrush-2p}$ min without startup oscillations during the POWER_UP period, when connected to the PD through channel resistance of 0.1Ω to 12.5Ω per pairset.

Derivation of PSE Minimum Guaranteed Total Inrush from 33.2.8.5.1:

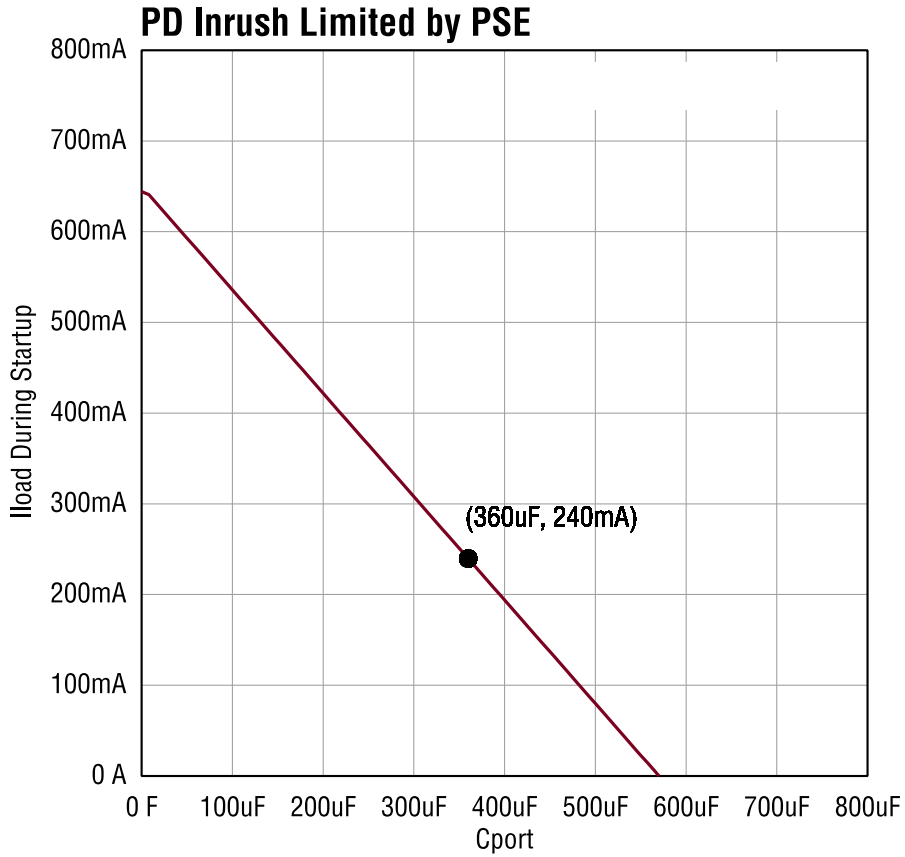
$I_{CLASS\_2\ max}$ = 240mA

C_{Port} = 360uF

240mA < [Q_{Inrush} – (360uF * 57V)] / 50ms

Q_{Inrush} > 32.5mC

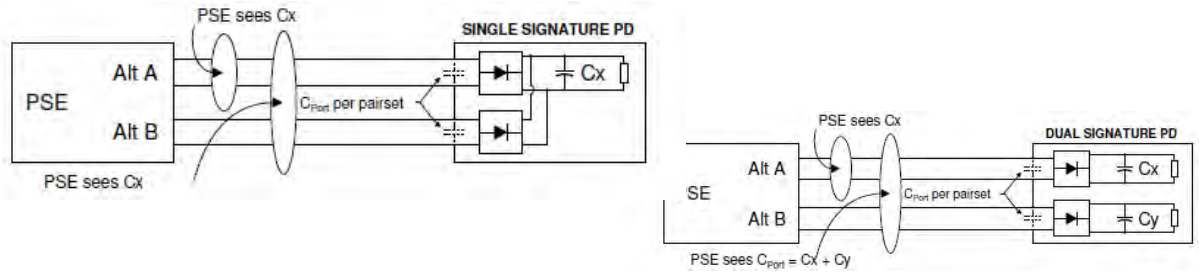
$I_{Inrush,min}$	$T_{inrush-2p,min}$	$Q_{Inrush,min}$	$V_{PSE,max}$
650mA	50ms	32.5mC	57V



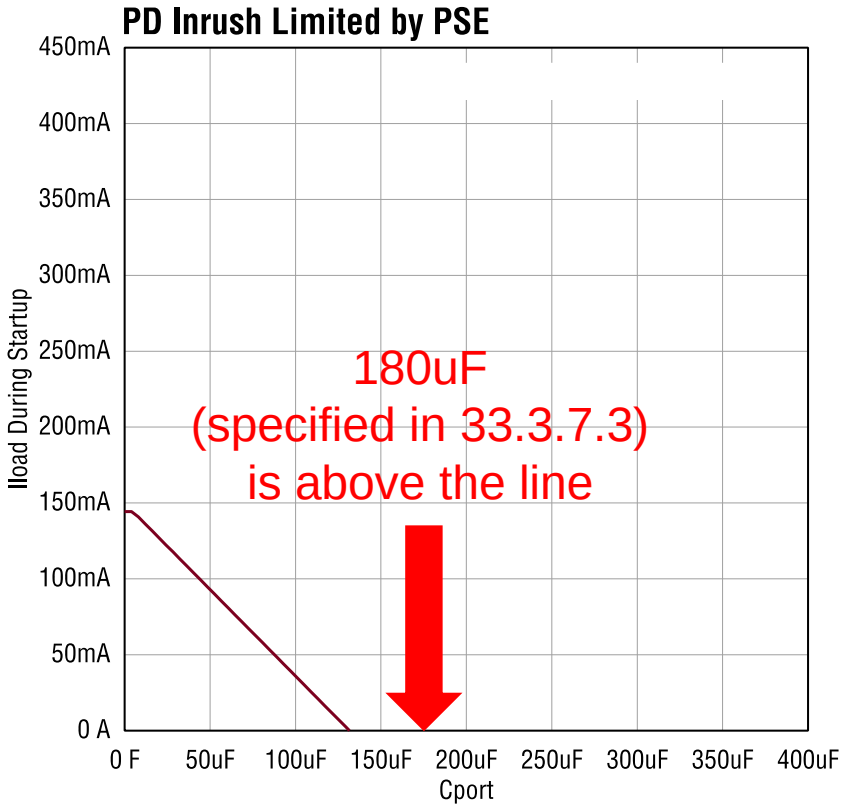
$$I_{load} < [32.5mC – (C_{port} * 57V)\ ]/\ 50ms$$

PSE Minimum Guaranteed *Per-Pairset* Charge during POWER_UP
SS PD Class 5 – 6, DS PD Class 1 - 4

8	Output current per pairset in the POWER_UP state as function of the assigned Class					
	Dual-signature PD Class 0 to 4	$I_{Inrush-2P}$	A	0.400	0.450	3, 4	See 33.2.8.5, max value definition in Figure 33–26
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.150	0.600	3, 4	
	Single-signature PD Class 7to 8 Dual-signature PD Class 5			0.400	0.600	4	See 33.2.8.5, max value definition in Figure 33–26. See 33.2.8.5.1 for conditions to use lower than $I_{Inrush-2P}$ min current values.



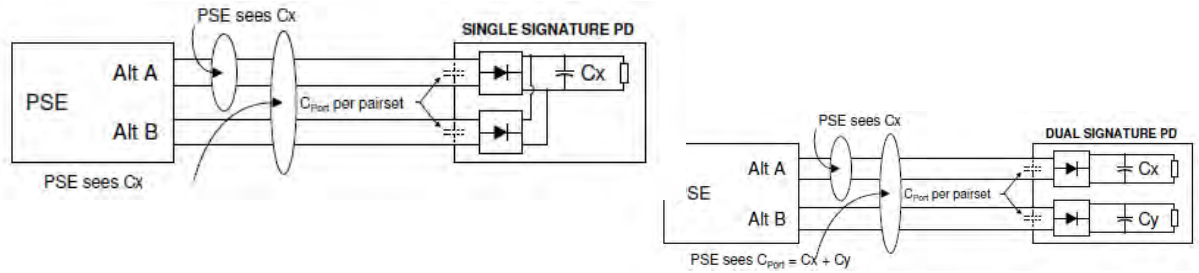
$I_{inrush-2p}$ min	$T_{inrush-2p}$ min	$Q_{Inrush-2p}$ min	$V_{PSE,max}$
150mA	50ms	7.5mC	57V



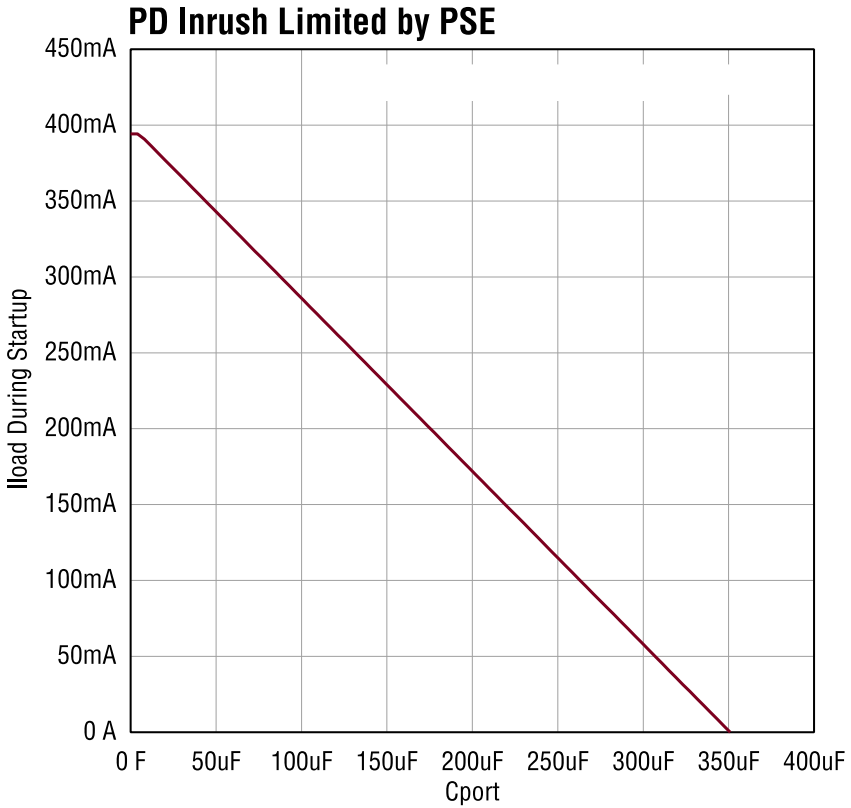
$$I_{load} < [7.5mC - (C_{port} * 57V)] / 50ms$$

PSE Minimum Guaranteed *Per-Pairset* Charge during POWER_UP
SS PD Class 7 – 8, DS PD Class 5

8	Output current per pairset in the POWER_UP state as function of the assigned Class					
	Dual-signature PD Class 0 to 4	$I_{Inrush-2P}$	A	0.400	0.450	3, 4	See 33.2.8.5, max value definition in Figure 33–26
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.150	0.600	3, 4	
	Single-signature PD Class 7to 8 Dual-signature PD Class 5			0.400	0.600	4	See 33.2.8.5, max value definition in Figure 33–26. See 33.2.8.5.1 for conditions to use lower than $I_{Inrush-2P}$ min current values.



$I_{inrush-2p\ min}$	$T_{inrush-2p\ min}$	$Q_{Inrush-2p\ min}$	$V_{PSE,max}$
400mA	50ms	20mC	57V



$$I_{load} < [20mC - (C_{port} * 57V)\ ]/\ 50ms$$

Proposed solution

- No change to Type 1, Type 2 behavior
- Type 3 PSE minimum inrush requirement remains 20mC
  - PSEs opting to simultaneously POWER_UP both pairsets of PDs Type 3 and below shall guarantee 20mC total charge
  - PSEs opting to stagger POWER_UP to PDs Type 3 and below shall guarantee 20mC charge per-pairset
- Type 4 PSE minimum inrush requirement remains 32.5mC
  - PSEs opting to simultaneously POWER_UP Type 4 PDs must be able to guarantee 32.5mC total charge
  - PSEs opting to stagger POWER_UP Type 4 DS PDs must be able to guarantee 16.75mC charge per-pairset

Baseline Text

- Modify Tables 33–17 and 33–28 as follows:

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	Applies to all Type 1 and 2 PSEs. Applies to Type 3 and 4 PSEs when both pairsets are in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			~~0.800~~ 0.650	0.900	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~
8	Output current per pairset in the POWER_UP state as function of the assigned Class						
	Single-signature PD Class 0 to 4 Dual-signature PD Class 1 to 4	$I_{Inrush-2P}$	A	0.400	0.450	3, 4	Applies to Type 3 and 4 PSEs when only one pairset is in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	~~Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4~~			~~0.150~~	~~0.600~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5			~~0.400~~ 0.325	0.600	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~

Table 33–17

6	Input inrush current						
	Single-signature PD Class 0 to 6 Dual-signature PD Class 1 to 4	I_{Inrush_PD}	A		0.400	All	Peak value—See 33.3.7.3
	Single-signature PD Class 7to 8 Dual-signature PD Class 5				~~0.800~~ 0.650	4	
7	Input inrush current per pairset						
	Dual-signature PD Class 1 to 4	I_{Inrush_PD-2P}	A		0.400	3	Peak value—See 33.3.7.3
	~~Single-signature PD Class 5 to 6 Dual-signature PD~~				~~0.300/ TBD~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5				~~0.600~~ 0.325	4	

Table 33–28

Baseline Text, cont'd

- Redefine PSE minimum inrush in terms of 4-Pair simultaneous and 2-Pair staggered output currents

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	Applies to all Type 1 and 2 PSEs. Applies to Type 3 and 4 PSEs when both pairsets are in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	0.900	3, 4	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			~~0.800~~ 0.650	0.900	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~
8	Output current per pairset in the POWER_UP state as function of the assigned Class						
	Single-signature PD Class 0 to 4 Dual-signature PD Class 1 to 4	$I_{Inrush-2P}$	A	0.400	0.450	3, 4	Applies to Type 3 and 4 PSEs when only one pairset is in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	~~Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4~~			~~0.150~~	~~0.600~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5			~~0.400~~ 0.325	0.600	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~

Table 33–17

6	Input inrush current						
	Single-signature PD Class 0 to 6 Dual-signature PD Class 1 to 4	I_{Inrush_PD}	A		0.400	All	Peak value—See 33.3.7.3
	Single-signature PD Class 7to 8 Dual-signature PD Class 5				~~0.800~~ 0.650	4	
7	Input inrush current per pairset						
	Dual-signature PD Class 1 to 4	I_{Inrush_PD-2P}	A		0.400	3	Peak value—See 33.3.7.3
	~~Single-signature PD Class 5 to 6 Dual-signature PD~~				~~0.300/ TBD~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5				~~0.600~~ 0.325	4	

Table 33–28

Baseline Text, cont'd

- Guaranteed interoperability

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
7	Total output current of both pairsets of the same polarity in the POWER_UP state as function of assigned Class						
	Single-signature PD Class 0 to 4	I_{Inrush}	A	0.400	0.450	All	Applies to all Type 1 and 2 PSEs. Applies to Type 3 and 4 PSEs when both pairsets are in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26. ~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~
	Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4			0.400	~~0.900~~	~~3, 4~~	
	Single-signature PD Class 7 to 8 Dual-signature PD Class 5			~~0.800~~ 0.650	0.900	4	
8	Output current per pairset in the POWER_UP state as function of the assigned Class						
	Single-signature PD Class 0 to 4 Dual-signature PD Class 1 to 4	$I_{Inrush-2P}$	A	0.400	~~0.450~~	~~3, 4~~	Applies to Type 3 and 4 PSEs when only one pairset is in POWER_UP state. See 33.2.8.5, max value definition in Figure 33-26.
	~~Single-signature PD Class 5 to 6 Dual-signature PD Class 1 to 4~~			~~0.150~~	~~0.600~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5			~~0.400~~ 0.325	0.600	4	~~See 33.2.8.5.1 for conditions to use lower than I_{Inrush} min current values.~~

Table 33–17

6	Input inrush current						
	Single-signature PD Class 0 to 6 Dual-signature PD Class 1 to 4	I_{Inrush_PD}	A		0.400	All	Peak value—See 33.3.7.3
	Single-signature PD Class 7to 8 Dual-signature PD Class 5				~~0.800~~ 0.650	4	
7	Input inrush current per pairset						
	Dual-signature PD Class 1 to 4	I_{Inrush_PD-2P}	A		0.400	3	Peak value—See 33.3.7.3
	~~Single-signature PD Class 5 to 6 Dual-signature PD~~				~~0.300/ TBD~~	~~3, 4~~	
	~~Single-signature PD Class 7 to 8~~ Dual-signature PD Class 5				~~0.600~~ 0.325	4	

Table 33–28

Baseline Text, cont'd

Modify section 33.3.7.3:

> For Type 1 and Type 2 PDs, input inrush current at startup is limited by the PSE if C_{Port} < 180 µF, as specified in Table 33–11.
>
> For Type 1 and Type 2 PDs, if C_{Port} ≥ 180µF, input inrush current shall be limited by the PD so that $I_{Inrush\_PD\_max}$ is satisfied.

Baseline Text, cont'd

Modify section 33.3.7.3:

The PSE minimum guaranteed charge when both pairsets are in POWER_UP state, Q_{Inrush}, is described by Equation 33–A:

$$\{Q_{Inrush}\}_C = I_{Inrush\ min} * T_{Inrush\text{-}2P\ min} \quad (33–A)$$

Input inrush current at startup I_{Inrush_PD} is limited by the PSE if the combination of PD C_{Port} and I_{Load} satisfy Equation (33–B).

$$\{Q_{Inrush}\}_C > \{C_{Port} * V_{Port\_PSE\text{-}2P\ max}\}_C + \{I_{Load} * t_{Inrush\text{-}2P\ min}\}_C \quad (33–B)$$

where

C_{Port} is the total capacitance seen on both pairsets as defined in Figure 33–33

I_{Load} is the PD load current during PSE POWER_UP state on both pairsets simultaneously

For all Type 3 and Type 4 PDs, if the combination of C_{Port} and I_{Load} exceeds the PSE minimum guaranteed charge Q_{Inrush}, input inrush current shall be limited by the PD such that $I_{Inrush\_PD\text{-}max}$ is satisfied.

Baseline Text, cont'd

Modify section 33.3.7.3:

The PSE minimum guaranteed charge when only one pairset is in POWER_UP state, $Q_{Inrush\text{-}2P}$, is described by Equation 33–C:

$$\{Q_{Inrush\text{-}2P}\}_C = I_{Inrush\text{-}2P\ min} * T_{Inrush\text{-}2P\ min} \qquad (33\text{–}C)$$

Input inrush current at startup $I_{Inrush\_PD\text{-}2P}$ is limited by the PSE if the combination of PD C_{Port} and $I_{Load\text{-}2P}$ satisfy Equation (33–D).

$$\{Q_{Inrush\text{-}2P}\}_C > \{C_{Port} * V_{Port\_PSE\text{-}2P\ max}\}_C + \{I_{Load\text{-}2P} * t_{Inrush\text{-}2P\ min}\}_C \qquad (33\text{–}D)$$

where

C_{Port}	is the capacitance seen on a particular pairset as defined in Figure 33–33
$I_{Load\text{-}2P}$	is the PD load during PSE POWER_UP state on only that pairset

For Type 3 and Type 4 dual-signature PDs, if the combination of C_{Port} and $I_{Load\text{-}2P}$ exceeds the PSE minimum guaranteed charge $Q_{Inrush\text{-}2P}$, input inrush current shall be limited by the PD such that $I_{Inrush\_PD\text{-}2P\ max}$ is satisfied.

Conclusions

- The proposed remedy…
  - Maintains legacy behavior
  - Provides straight-forward requirements that can easily be validated
  - Guarantees interoperability
    - –PSE minimum inrush requirements are dependant upon Table 33–17
    - –PD inrush requirements and informative statements are dependant upon…
      - The same PSE variables when PSE controls inrush
      - Corresponding and symmetric PD inrush variables in Table 33–28 when PD controls inrush
  - Provides design flexibility to PD designers
    - –All valid combinations of C_{Port} and I_{Load} are defined
    - –The PSE has clearly defined behavior for simultaneous and staggered inrush

Interoperability and Relationships