MPS Baseline proposal

v240

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Goals

- Allow modified MPS parameters as defined in yseboodt_01_0314.pdf
- Keep safety parameter $T_{MPDO(MAX)}$ unchanged
- Reduce MPS power to <= 25mW

Definitions

- Currently “Type 3” is undefined
- This proposal assumes Type 3 to be the new type we create in 802.3bt
  - If we create Type 4 in addition to Type 3, Type 4 will have the same MPS behavior as Type 3 and the text will be modified accordingly.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
17	DC MPS current	I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
				TBD	TBD	3	
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
				0.3535		3	
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.06		1, 2	See 33.2.9.
				0.0065		3	

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS for Type 1 and Type 2 PDs shall be current draw equal to or above **10 mA** for a minimum duration of 75 **ms measured at the PD PI** followed by an optional MPS dropout for no longer than 250ms . The MPS for Type 3 PDs shall be:

a) Current draw equal to or above **10 mA** for a minimum duration of 75 **ms measured at the PD PI** followed by an optional MPS dropout for no longer than 250ms **when connected to a Type 1 or 2 PSE, and**

b) Current draw equal to or above **TBD mA** for a minimum duration of **7 ms measured at the Test Circuit PI in Figure 33-##** followed by an optional MPS dropout for no longer than **318 ms when connected to a Type 3 PSE.**

In addition, the MPS for all PDs shall have input impedance with resistive and capacitive components as defined in Table 33–19.

Item	Parameter	Symbol	Unit	Min	Max	Additional information
~~1~~	~~Input current~~	~~I_{Port_MPS}~~	~~A~~	~~0.01~~	~~-~~	~~See 33.3.8~~
1	Input resistance	R_{pd_d}	kΩ		26.3	
2	Input capacitance	C_{pd_d}	µF	0.05		See Table 33–12

Note: Figure 33-## will reference proposed MPS Test Circuit.

33.3.8 PD Maintain Power Signature (cont.)

Other Proposed Changes:

A PD that does not maintain the MPS components ~~in a) and b)~~ above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

Powered PDs that no longer require power shall remove both the current draw and impedance components ~~a) and b)~~ of the MPS. To cause PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

NOTE—A Type 1 or 2 PD with C_{port} > 180 µF may not be able to meet the I_{Port_MPS} specification in Table 33–19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

Original MPS Text

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall be both:

a) Current draw equal to or above the minimum input current (I_{Port_MPS} min) as specified in Table 33–19 for a minimum duration of 75 ms followed by an optional MPS dropout for no longer than 250 ms, and

b) Input impedance with resistive and capacitive components as defined in Table 33–19.

A PD that does not maintain the MPS components in a) and b) above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

Powered PDs that no longer require power shall remove both components a) and b) of the MPS. To cause PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

Table 33–19—PD Maintain Power Signature

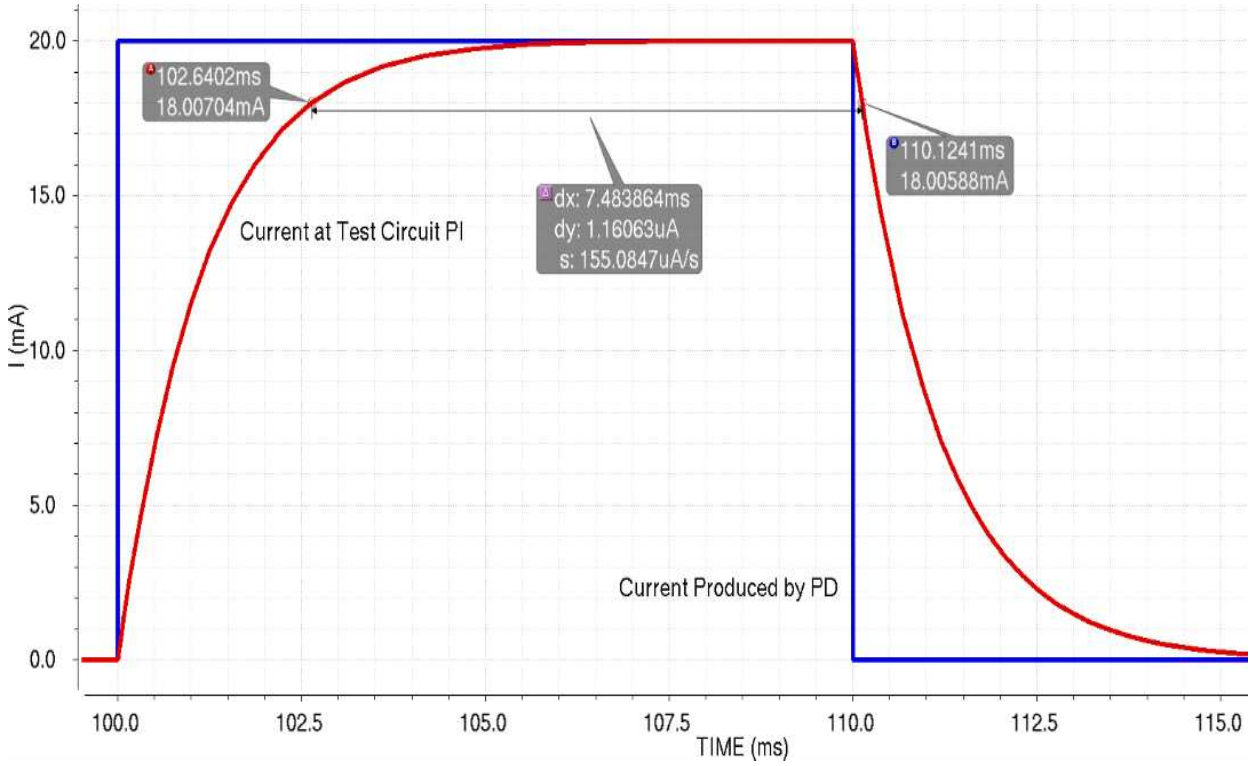
Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{Port_MPS}	A	0.010		See 33.3.8
2	Input resistance	R_{pd_d}	kΩ		26.3	
3	Input capacitance	C_{pd_d}	µF	0.050		See Table 33–12

NOTE—A PD with $C_{port} > 180$ µF may not be able to meet the I_{Port_MPS} specification in Table 33–19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

Explanation

MPS Pulse Current Stealing

- PD capacitance can effectively shorten the MPS pulse by “stealing” the current from the PSE.
  - The impedance of the capacitor is lower than that of the cable and PSE at high frequencies (edges of the pulse).
  - Adding margin between the steady state PD current and the PSE threshold removes a large amount of the exponential rise time from the measurement.
    - Lowing the PSE threshold slightly (10 mA per channel to 9 mA per channel) accomplishes this while keeping the PD standby power as low as possible.



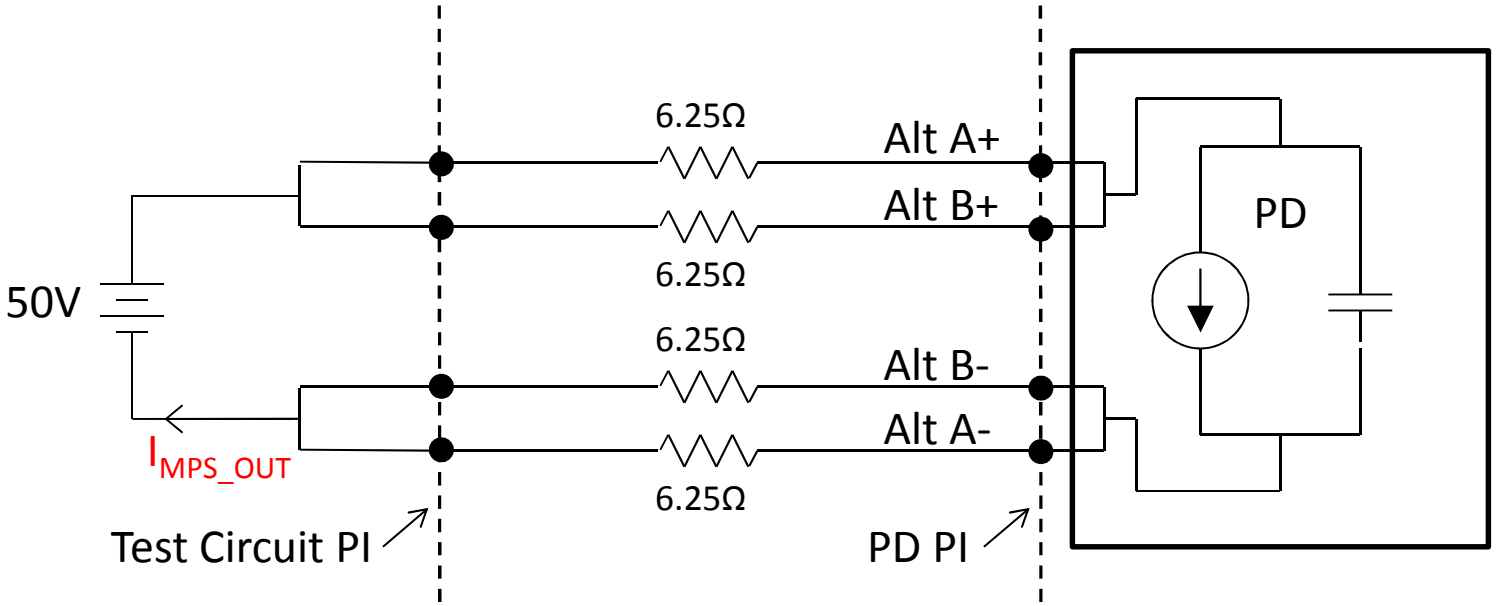
Example: A 10 ms pulse produced by the PD results in a 7.5 ms pulse (measured at 90%) at the PSE.

Note: PD consisted of ideal current source and 180uF Capacitor. A resistance of 6.25Ω was used for each wire pair.

The Test Circuit Approach

- A test circuit will be used to:
  - Allow PDs to draw as little power in standby mode as possible
  - Ensure that the PSE will receive a large enough MPS pulse to be consistently detected.
- The test circuit will account for the worst case cabling connection between a PD and a Type 3 PSE.
- The test circuit approach allows for both flexibility in implementation and specifications that result in very low standby power by replacing spec margin with actual measurement.

MPS Test Circuit



- PD must draw enough current to guarantee an MPS pulse of a given magnitude for at least a certain length when measured at the test circuit PI.

Flexibility in Implementation

- The PD manufacturer could choose to:
  - Increase pulse width of MPS signal to account for a given range of load capacitance.
    - Increase in pulse width for an ideal system is shown to the right.
    - Calculated increase was found using the 10%-90% rise time of an exponential signal.

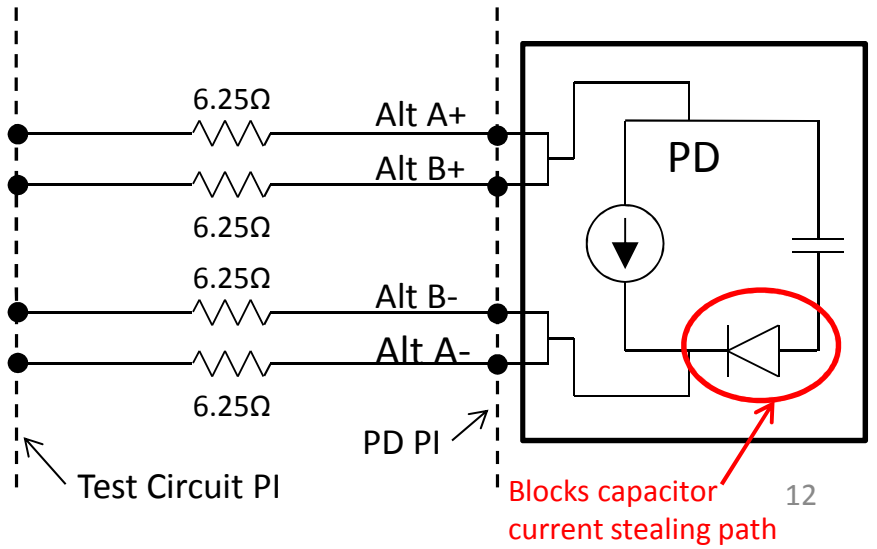
$$Addition\ Pulse\ Width = \frac{0.35}{f_c}$$

$$f_c = \frac{1}{2\pi * R_{Wire} * C_{PD}} \qquad R_{Wire} = 6.25\Omega$$

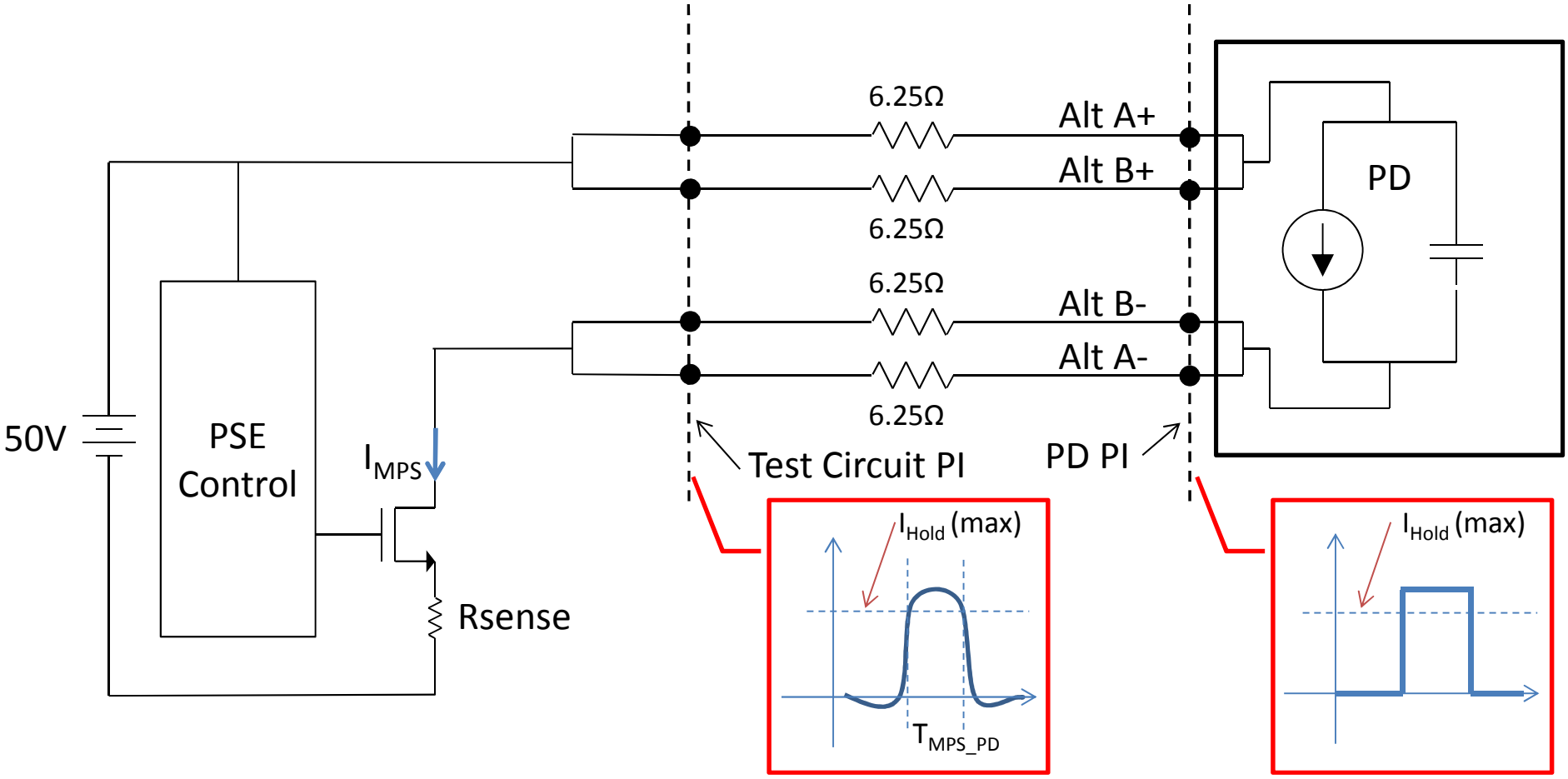
  - Design a system to block the load capacitance from "stealing" the current pulse.
  - Implement any other system to ensure that at the MPS specification is met at the test circuit PI.

PD Capacitance (uF)	Additional Pulse Time Needed (ms)	
	Calculated	Simulated
10	0.137	0.140
50	0.687	0.701
100	1.374	1.402
150	2.062	2.105
180	2.474	2.511
200	2.749	2.809
220	3.024	3.091
250	3.436	3.517
360	4.946	*

Note: These numbers are for idea system with no PD, PSE, or diode bridge impedance. Extra margin will be needed to compensate for these.



The Whole System Illustrated



Notes:

1. PD produces an MPS pulse of any size and shape so that T_{MPS_PD} (7 ms) is met at the test circuit PI.
2. PSE considers MPS present when the current is higher than I_{Hold} (TBD mA) for more than T_{MPS} (6.5 ms).
3. PSE shown is an example. Actual PSE may consist of two power channels measuring total current.