PSE current limiting v100

Info (not part of baseline)

Draft 3.3: The PSE shall limit a pairset current to $I_{LIM\text{-}2P}$ for a duration of up to T_{LIM}.
Draft 3.4: The PSE shall limit the pairset current to $I_{LIM\text{-}2P}$ for a duration of at least T_{LIM}.

This change was made because the construct "up to T_{LIM}" makes the entire requirement optional. Furthermore, the PD is dependent on the PSE limiting current during transients to successfully ride out voltage transients. In draft 3.4 however, we now have conflicting requirements / statements:

page	line	
181	33	A PSE may remove power from the PI if the current on any pair meets or exceeds the "PSE lowerbound template" in Figure 145–23 or Figure 145–24.
183	26	The PSE shall limit the pairset current to $I_{LIM\text{-}2P}$ for a duration of at least T_{LIM}.
184	1	If a short circuit condition is detected on a pairset, power removal from that pairset shall begin within T_{LIM} as defined in Table 145–16.
184	2	If $I_{Port\text{-}2P}$ exceeds the PSE lowerbound template, the PSE output voltage may drop below $V_{Port\_PSE\text{-}2P}$ min.
184	5	A PSE in a power on state may remove power from that pairset without regard to T_{LIM} when the pairset voltage no longer meets the $V_{Port\_PSE\text{-}2P}$ specification.

So what do we need?

- The PSE needs to limit current to $I_{LIM\text{-}2P}$ for **at least** T_{LIM} in order for the PD to be able to deal with transients
- The PSE should not be required to limit the current when there is a short on the PI, that would require it to be able to dissipate huge amounts of power

Proposal
If $V_{PSE} > V_{Tran\text{-}2P}$ the PSE is required to limit to current for at least T_{LIM}, however if $V_{PSE} < V_{Tran\text{-}2P}$ it may shutdown immediately and is required to shutdown **before** T_{LIM}. Such a proposal would seem to be in line with the original intention of 802.3at.

145.2.10.8 Short circuit current

A PSE may remove power from the PI if the current on any pair ~~meets or~~ exceeds the "PSE lowerbound template" in Figure 145–23 or Figure 145–24. Power shall be removed from a pairset of a PSE before the pairset current exceeds the "PSE upperbound template" in Figure 145–23 or Figure 145–24. When connected to a single-signature PD, the PSE should remove power from both pairsets before the current exceeds the "PSE upperbound template" on either pairset.

. . .

The PSE shall limit the pairset current to $I_{LIM\text{-}2P}$ for a duration of at least T_{LIM} , when V_{PSE} is greater or equal to $V_{Tran\text{-}2P}$. The cumulative duration of the current limit event may be measured with a sliding window of at most 1 second width.

. . .

A short circuit condition occurs when the pairset voltage, V_{PSE}, is less than $V_{Tran\text{-}2P}$, during a power on state. If a short circuit condition is detected on a pairset, power removal from that pairset shall begin within T_{LIM} as defined in Table 145–16. If $I_{Port\text{-}2P}$ exceeds the PSE lowerbound template, the PSE output voltage may drop below $V_{Port\_PSE\text{-}2P}$ min.

A PSE in a power on state may remove power from that pairset without regard to T_{LIM} when the pairset voltage no longer meets the $V_{Port\_PSE\text{-}2P}$ specification.