POWER_ON multiple true fix & simplification v100

Info (not part of baseline)

The D2.2 state POWER_ON for the Type 3 and Type 4 PSE state diagram contains a number of permutations that would cause multiple arcs to be true simultaneously. This baseline fixes those, as well as introducing a compound error variable to simplify the logic. Also, the statement pse_ss_mode_update is added to the POWER_ON state. This statement was forgotten to include in D2.2 when implementing ➠yseboodt_07_1116_2p4p.pdf

33.2.5.9 Type 3 and Type 4 variables

Insert new variables as follows:

error_pri

A variable indicating if either a short-circuit or an overload is detected on the Primary Alternative, or if the voltage on the Primary Alternative is outside of the operating range. This variable is set according to logical result of "short_det_pri + ovld_det_pri + option_vport_lim_pri".
Values:

FALSE: short_det_pri, ovld_det_pri, and option_vport_lim_pri are FALSE
TRUE: short_det_pri, ovld_det_pri, or option_vport_lim_pri is TRUE

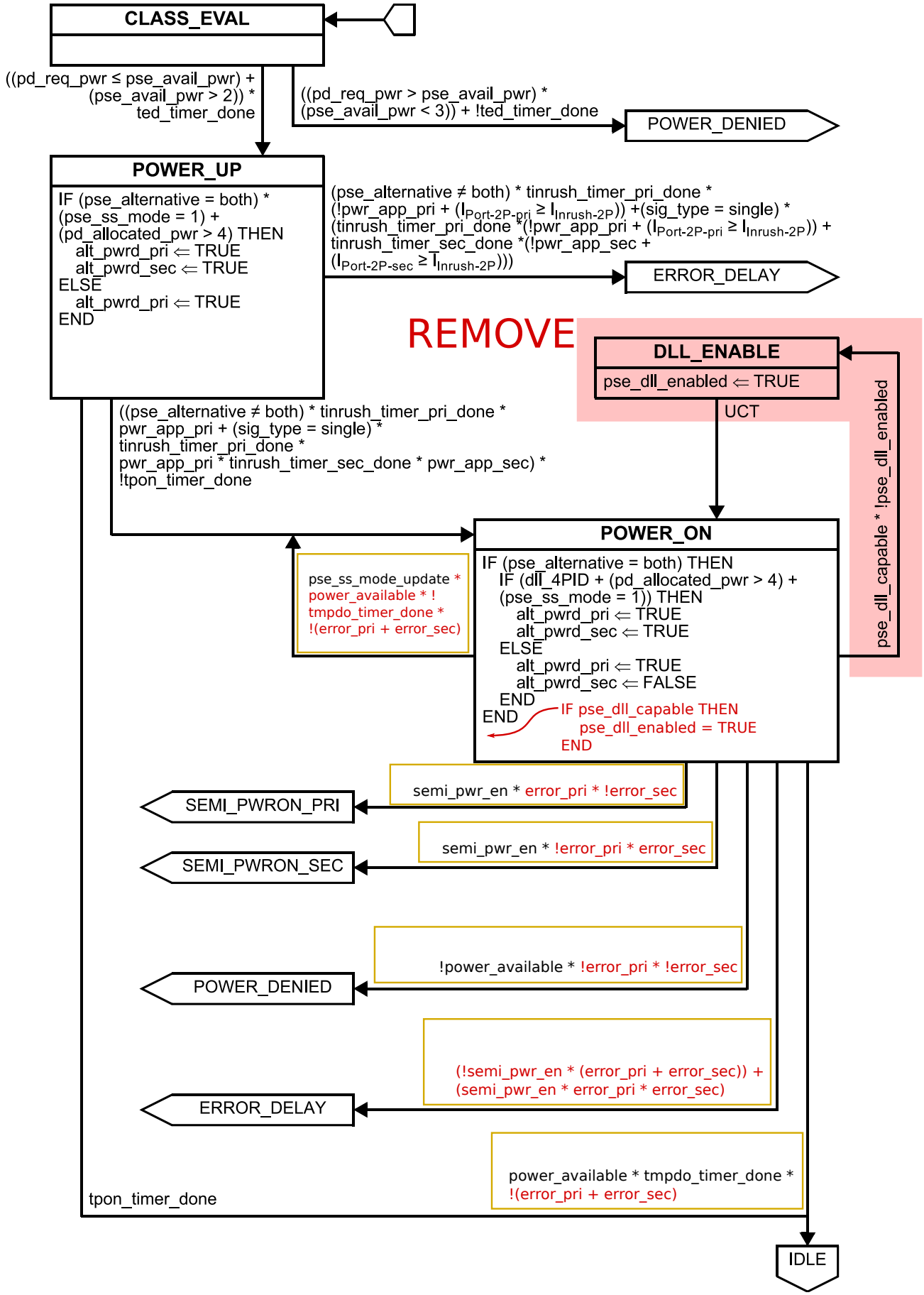
error_sec

A variable indicating if either a short-circuit or an overload is detected on the Secondary Alternative, or if the voltage on the Primary Alternative is outside of the operating range. This variable is set according to logical result of "short_det_sec + ovld_det_sec + option_vport_lim_sec".
Values:

FALSE: short_det_sec, ovld_det_sec, and option_vport_lim_sec are FALSE
TRUE: short_det_sec, ovld_det_sec, or option_vport_lim_sec is TRUE

33.2.5.12 Type 3 and Type 4 state diagrams

Modify Figure 33–15 on page 95 as follows:



Info (not part of baseline)

For reference, the original D2.2 POWER_ON state: