

Updated comment and remedy for comment #214

33.6 Data Link Layer classification need to be updated in order to:

1. Cleanup parameters that are not used by single-signature DLL state machines.
2. Support dual-signature PD with the following objectives:
 - 2.1 Power Demotion use cases.
 - 2.2 Addressing cases when power is not sufficient for one of the modes or both modes.
2. To fix some error regarding the sync between variable names in PD state machine and its variable list, clause 33.6 PD/PSE DLL power state machine (Figures 33-49 and 33-50) and its variable list.

Proposed Remedy:

Adopt darshan_11_0915.pdf if ready for the meeting. If not, add the following editor note to the beginning of clause 33.6:

"Editor Note: 33.6 Data Link Layer classification need to be updated in order to:

1. Cleanup parameters that are not used by single-signature DLL state machines.
 2. Support dual-signature PD.
 2. To fix some error regarding the sync between variable names in PD state machine and its variable list, clause 33.6 PD/PSE DLL power state machine (Figures 33-49 and 33-50) and its variable list.
- "

Proposed Baseline starts here

33.6 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Single-signature PDs advertising a Class 4 signature or higher and Type 3 and Type 4 dual-signature PDs support Data Link Layer classification (see 33.3.6). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

33.6.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2 and the Power via MDI Measurements TLV defined in 79.3.7; and shall support the control state diagrams defined in 33.6.3.

33.6.2 Data Link Layer classification timing requirements

Type 2, 3, and 4 PSEs shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable `pse_dll_enabled` (33.2.5.4, 33.6.3.3).

A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable `pse_dll_ready` (33.6.3.3).

Type 1 PDs that implement Data Link Layer classification and Type 2, 3, and 4 PDs shall set the state variable `pd_dll_ready` within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable `pd_dll_enabled` (33.3.3.7, 33.6.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PSE allocated power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PD requested power value” field is different from the previously communicated value.

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PD requested power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PSE allocated power value” field is different from the previously communicated value.

33.6.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–49. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–50.

The power control state diagrams shown in Figure 33-49 and Figure 33-50 are used for PSEs connected to single-signature PDs and dual-signature PDs.

For dual-signature PDs, the state machine is used for mode A and mode B independently.

33.6.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 33.2.5.2.

33.6.3.2 Constants

This is not part of the baseline
The following modifications are meant to differentiate between single-signature PDs and dual-signature PDs.

PD_DLLMAX_VALUE

For single-signature PD:

This value is derived from pd_max_power variable (33.3.3.7) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255
5	400
6	600
7	620
8	999

For dual-signature PD:

This value is derived from pd_max_power_Y variable (33.3.3.12) described as follows:

pd_max_power _Y	PD_DLLMAX_VALUE
1	39
2	65
3	130
4	255
5	355

PD_INITIAL_VALUE

For single-signature PD:

This value is derived as follows from the pd_max_power (33.3.3.7) variable used in the PD state diagram (Figure 33–32):

pd_max_power	PD_INITIAL_VALUE
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0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255
5	≤ 400
6	≤ 600
7	≤ 620
8	≤ 900

For dual-signature PD:

This value is derived as follows from the `pd_max_powerY` variable (33.3.3.12) used in the PD state diagram (Figure 33–33):

<code>pd_max_powerY</code>	<code>PD_INITIAL_VALUE</code>
1	≤39
2	≤ 65
3	≤ 130
4	≤255
5	≤355

`PSE_INITIAL_VALUE`

For single-signature PD:

This value is derived as follows from `parameter_type` and the `mr_pd_class_detected` (33.2.5.6) variable used in the PSE state diagram (Figure 33–13):

<code>parameter_type</code>	<code>pd_allocated_power</code>	<code>PSE_INITIAL_VALUE</code>
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	4	255
3	5	400
3	6	600
4	7	620
4	8	900

Variables `PD_DLLMAX_VALUE`, `PD_INITIAL_VALUE`, and `PSE_INITIAL_VALUE`, are quantized to fit the available resolution. Additional information on power levels for Classes 6 and 8 may be found in 33.3.8.2.

For dual-signature PD:

This value is derived as follows from `parameter_type` and the `mr_pd_class_detected` (33.2.5.6) variable used in the PSE state diagram (Figure 33–13):

<code>parameter_type</code>	<code>pd_allocated_power</code>	<code>PSE_INITIAL_VALUE</code>
3	1	39
3	2	65
3	3	130
3	4	255
4	5	355

Variables `PD_DLLMAX_VALUE`, `PD_INITIAL_VALUE`, and `PSE_INITIAL_VALUE`, are quantized to fit the available resolution. Additional information on power levels for Classes 1 - 5 may be found in 33.3.8.2.

33.6.3.3 Variables

Editor Note: To verify that the content of this subclause is matching clause 30.

The PSE power control state diagram (Figure 33–49) and PD power control state diagram (Figure 33–50) use the following variables:

MirroredPDRRequestedPowerValue

The copy of PDRRequestedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where X is the decimal value of MirroredPDRRequestedPowerValue.

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

MirroredPDRRequestedPowerValueEcho

The copy of PDRRequestedPowerValueEcho that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRRequestedPowerValue attribute (30.12.3.1.17).

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

MirroredPSEAllocatedPowerValue

The copy of PSEAllocatedPowerValue that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where X is the decimal value of MirroredPSEAllocatedPowerValue. For

single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

MirroredPSEAllocatedPowerValueEcho

The copy of PSEAllocatedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).

PDRRequestedPowerValueEcho

This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRRequestedPowerValue attribute (30.12.2.1.17).

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

PDMaxPowerValue

Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.8.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where X is the decimal value of PDMaxPowerValue.

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

PDRRequestedPowerValue

Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.8.2) the PD requests. This power value is encoded according to Equation (79–1), where X is the decimal value of PDRRequestedPowerValue. This variable is mapped from the aLldpXdot3LocPDRRequestedPowerValue attribute (30.12.2.1.17).

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValue

Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.8.2) the PD ever draws. This power value is encoded according to Equation (79–2), where X is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

PSEAllocatedPowerValueEcho

This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).

For single-signature PD: Values: 1 through 999

For dual-signature PD: Values: 0 through 499.

When a PD mode is not active, the value shall be set to zero.

TempVar

A temporary variable used to store Power Value of 1 through 999 for single-signature PD or 0 to 499 for dual-signature PD. Actual power numbers are represented using an

integer value that is encoded according to Equation (79–1) or Equation (79–2), where X is the decimal value of TempVar.

local_system_change

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.

Values:

FALSE: The local system does not want to change the power allocation.

TRUE: The local system wants to change the power allocation.

This is not part of the baseline

parameter_type is used only in Type 1 and 2 PSEs and shown only in figure 33-13. However the text below address also Type 3 and 4 PSEs which parameter_type variable is not in the list of 33.3.3.7 and not used by the Type 3 and 4 state machine as well. The text need to be modify to used only for Type 1 and 2. See also comment #309 for D2.0.

parameter_type

A Type 1 and 2 PSE state diagram control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification. Type 3 and 4 PSE state diagrams do not use this variable.

~~A control variable output by the PSE state diagram (Figure 33–13) used by a Type 2, Type 3, or Type 4 PSE to choose operation with Type 1, Type 2, Type 3, or Type 4 PSE output PI electrical requirement parameter values defined in Table 33–17.~~

Values:

1: Type 1 PSE parameter values (default).

2: Type 2 PSE parameter values.

~~3: Type 3 PSE parameter values.~~

~~4: Type 4 PSE parameter values.~~

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–32) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values:

FALSE: PD Data Link Layer classification is not enabled.

TRUE: PD Data Link Layer classification is enabled.

pd_dll_power_type

A control variable that indicates the Type of PD that is connected to the PSE as advertised through Data Link Layer classification.

Values:

- 1: PD is a Type 1 PD (default).
- 2: PD is a Type 2 PD.
- 3: PD is a Type 3 PD.
- 4: PD is a Type 4 PD.

pd_dll_ready

An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values:

- FALSE: Data Link Layer classification has not completed initialization.
- TRUE: Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–13) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values:

- FALSE: PSE Data Link Layer classification is not enabled.
- TRUE: PSE Data Link Layer classification is enabled.

This is not part of the baseline

pse_dll_power_level is not used by Figure 33-50 therefore deleted from 33.6.3.3.

See darshan_12_0916.pdf and per comment #296

~~pse_dll_power_level~~

~~A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered.~~

~~Values:~~

- ~~1: The PSE has allocated Class 3 power or less (default).~~
- ~~2: The PSE has allocated Class 4 power.~~
- ~~3: The PSE has allocated Class 5 or Class 6 power.~~
- ~~4: The PSE has allocated Class 7 or Class 8 power.~~

This is not part of the baseline

pse_dll_power_type is used in Figure 33-50 and missing from 33.6.3.3.

See also Schindler_02_0916.pdf addressing this variable.

pse_dll_power_type

A control variable output by the PD power control state diagram (Figure 33-50) that indicates the PSE type as 1 or 2, see 79.3.2.4.1.

Values:

- 1: The PSE is a Type 1 PSE, for a Type-1 PSE (Default).
- 2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE

This is not part of the baseline

Adding two new variables **pd_dll_load_type** and **pd_dll_mode_selection** that are already specified in Table 79-6b, to be used by DLL state machines to correctly allocate power per pairset.

Editor Note: The parameters **pd_load** and **pd_mode_selection** are missing from Table 79-8 and 79-9.

pd_dll_load_type

A control variable output by the PD control state diagram (Figure 33-50) that based on the information in Table 79-6b **bit #1**, in order to ensure execution of PSE new power allocation correctly per pairset. This variable is not used in single-signature PD.

Values:

FALSE: PD power demand on Mode A and Mode B are not electrically isolated. New assigned power value for Mode A and mode B is identical.

TRUE: PD power demand on Mode A and Mode B are electrically isolated. New assigned power for Mode A and mode B is assigned independently with optional different values from each other.

This is not part of the baseline

pd_dll_mode_selection in Table 79-6b bit 0 was updated accordingly to enable this functionality.

pd_dll_mode_selection

A control variable output by the PD or PSE control state diagrams (Figure 33-49 and Figure 33-50).

When the power type is PD (see Table 79-6b) then this bit shall be set as defined in Table 79-6b bit 0 in order to inform the PSE if the PD is requesting power over mode A or mode B.

When the power type is PSE (see Table 79-6b) then this bit shall be set as defined in Table 79-6b bit 0 in order to inform the PD if PSE is allocating power over Alternative A or Alternative B.

This variable is used only when dual-signature PD is connected to the PSE.

Values:

FALSE: PD requested power applies to Mode A pairset or PSE allocated power applies to Alternative B.

TRUE: PD requested power applies to Mode B pairset or PSE allocated power applies to Alternative A.

This is not part of the baseline

pse_power_level is not used by Figure 33-50 hence deleted. See also darshan_12_0916.pdf and per comment #312

~~pse_power_level~~

~~A control variable output by the PD state diagram that indicates the power level assigned by the PSE. This value is a result of the Class requested by the PD and the power available from the PSE.~~

A summary cross-references between the DTE Power via MDI classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33-40.

33.6.3.4 Functions

pse_power_review

This function evaluates the PSE power allocation or **power** budget of the PSE based on local system changes. The function returns the following variables:

PSE_NEW_VALUE:

The new maximum power value that the PSE expects the PD to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where X is the decimal value of PSE_NEW_VALUE.

The PSE_NEW_VALUE content is a function of Power type, pd_dll_load_type and pd_dll_mode_selection which was derived from the Power type, PD Load and PD mode selection in Table 79-6b as follows:

Power type	pd_dll_load_type	pd_dll_mode_selection	PSE_NEW_VALUE
Type 1, Type 2 and single-signature Type 3 and Type 4 PDs	-----	-----	The new maximum total power value that the PSE expects the PD to draw.
dual-signature Type 3 and Type 4 PDs	FALSE	-----	The new maximum total power value that the PSE expects the PD to draw divided by 2 for each PSE alternative A and B.
dual-signature Type 3 and Type 4 PDs	TRUE	TRUE	The new maximum power value that the PSE expects the PD to draw over mode A.
dual-signature Type 3 and Type 4 PDs	TRUE	FALSE	The new maximum power value that the PSE expects the PD to draw over mode B.

execute_allocation

This function fills the TLV information fields **PD requested power value**, **PSE allocated power value** and PD mode selection, and send the information based on PD structure; single-signature or dual-signature.

In case of single signature PD, the PSE allocation power value will be performed in a single LLDP transaction when PSE allocated power value will be set.

In case of dual signature PD, the PSE allocation power value will be performed consecutively for each alternative, while the PD will be informed for each alternative allocation, using pd_mode_selection variable.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:

PD_NEW_VALUE:

The new maximum power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where X is the decimal value of PD_NEW_VALUE.

Table 33–40—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRequestedPowerValue	←	PDRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	←	PSEAllocatedPowerValue
	aLldpXdot3LocReady	←	pse_dll_ready
PD	aLldpXdot3LocPDRequestedPowerValue	←	PDRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	←	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	←	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerType Value ¹ 11 01	⇒ ⇒	pd_dll_power_type Value ¹ 01 10
PD	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
	aLldpXdot3RemPowerType Value ¹ 10 00	⇒ ⇒	pse_dll_power_type Value ¹ 01 10

¹Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

33.6.3.5 State diagrams

The general state change procedure for PSEs is shown in Figure 33–49.

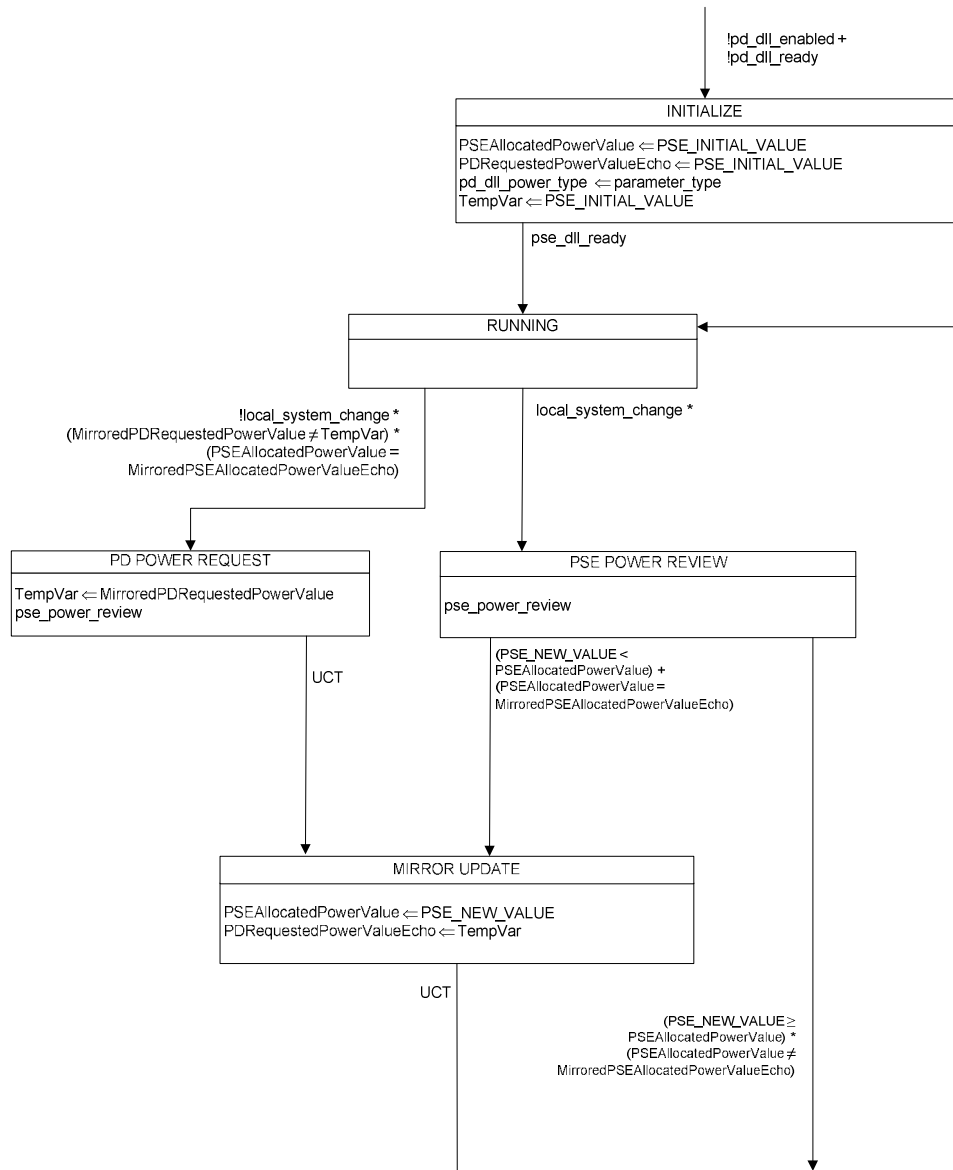


Figure 33–49—PSE power control state diagram

The general state change procedure for PDs is shown in Figure 33–50.

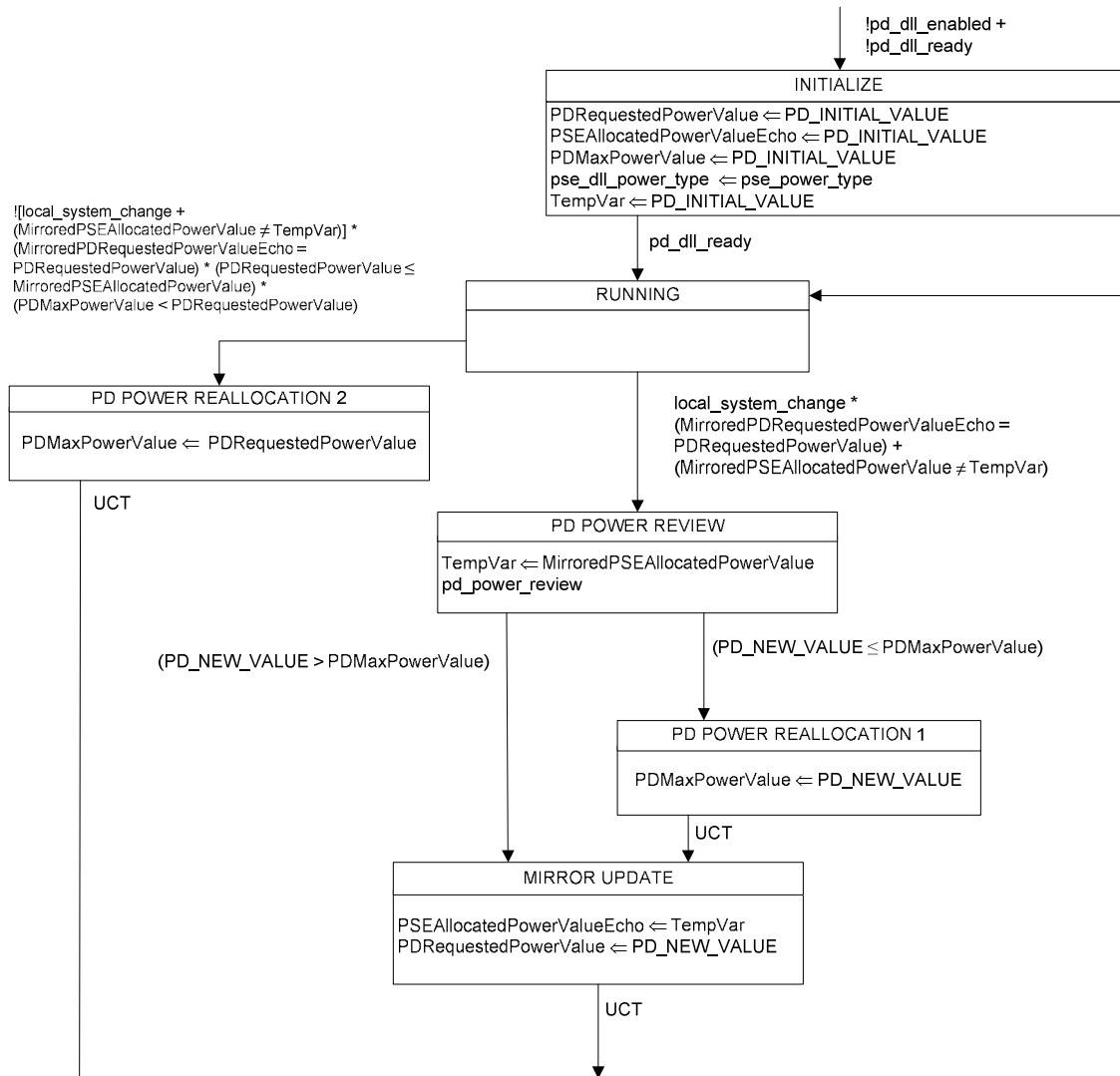


Figure 33–50—PD power control state diagram

33.6.4 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the `aLldpXdot3LocPDRequestedPowerValue` (30.12.2.1.17) attribute in the `oLldpXdot3LocSystemsGroup` object class. The request appears to the PSE as a change to the `aLldpXdot3RemPDRequestedPowerValue` (30.12.3.1.17) attribute in the `oLldpXdot3RemSystemsGroup` object class.

The PSE responds to the PD's request through the `aLldpXdot3LocPSEAllocatedPowerValue` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup` object class. The PSE also copies the value of the

to the `aLldpXdot3LocPDRRequestedPowerValue` (30.12.2.1.17) in the `oLldpXdot3LocSystemsGroup` object class. This appears to the PD as a change to the `aLldpXdot3RemPSEAllocatedPowerValue` (30.12.3.1.18) attribute in the `oLldpXdot3RemSystemsGroup` object class.

The PSE may allocate a new power value through the `aLldpXdot3LocPSEAllocatedPowerValue` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup` object class. The request appears to the PD as a change to the `aLldpXdot3RemPSEAllocatedPowerValue` (30.12.3.1.18) attribute in the `oLldpXdot3RemSystemsGroup` object class. The PD responds to a PSE's request through the `aLldpXdot3LocPDRRequestedPowerValue` (30.12.2.1.17) attribute in the `oLldpXdot3LocSystemsGroup` object class. The PD also copies the value of the `aLldpXdot3RemPSEAllocatedPowerValue` (30.12.3.1.18) attribute in the `oLldpXdot3RemSystemsGroup` object class to the `aLldpXdot3LocPSEAllocatedPowerValue` (30.12.2.1.18) attribute in the `oLldpXdot3LocSystemsGroup` object class. This appears to the PSE as a change to the `aLldpXdot3RemPDRRequestedPowerValue` (30.12.3.1.17) attribute in the `oLldpXdot3RemSystemsGroup` object class.

The state diagrams describe the behavior above.

33.6.4.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of `PSEAllocatedPowerValue` matches the value of `MirroredPSEAllocatedPowerValueEcho`. When the PSE is not in sync with the PD, the PSE is allowed to change its power allocation.

During normal operation, the PSE is in the `RUNNING` state. If the PSE wants to initiate a change in the PD allocation, the `local_system_change` is asserted and the PSE enters the `PSE POWER REVIEW` state, where a new power allocation value, `PSE_NEW_VALUE`, is computed. If the PSE is in sync with the PD or if `PSE_NEW_VALUE` is different than `PSEAllocatedPowerValue`, it enters the `MIRROR UPDATE` state where `PSE_NEW_VALUE` is assigned to `PSEAllocatedPowerValue`. It also updates `PDRRequestedPowerValueEcho` and returns to the `RUNNING` state.

If the PSE's previously stored `MirroredPDRRequestedPowerValue` changes, a request by the PD to change its power allocation is recognized. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the `PD POWER REQUEST` state. A new power allocation value, `PSE_NEW_VALUE`, is computed. It then enters the `MIRROR UPDATE` state where `PSE_NEW_VALUE` is assigned to `PSEAllocatedPowerValue`. It also updates `PDRRequestedPowerValueEcho` and returns to the `RUNNING` state.

33.6.4.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of `PDRRequestedPowerValue` matches the value of `MirroredPDRRequestedPowerValueEcho`. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the `RUNNING` state. If the PD's previously stored `MirroredPSEAllocatedPowerValue` is changed or `local_system_change` is asserted by the PD so as to change its power allocation, the PD enters the `PD POWER REVIEW` state. In this state, the PD evaluates the change and generates an updated power value called `PD_NEW_VALUE`. If `PD_NEW_VALUE` is less than `PDMaxPowerValue`, it updates `PDMaxPowerValue` in the `PD POWER REALLOCATION 1` state. The PD finally enters the `MIRROR UPDATE` state where `PD_NEW_VALUE` is assigned to `PDRRequestedPowerValue`. It also updates `PSEAllocatedPowerValueEcho` and returns to the `RUNNING` state.

In the above flow, if `PD_NEW_VALUE` is greater than `PDMaxPowerValue`, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the `PD POWERREALLOCATION 2` state. In this state, the PD assigns `PDMaxPowerValue` to `PDRRequestedPowerValue` and returns to the `RUNNING` state.

33.6.5 Autoclass

This is not part of the baseline
This clause was not addressed in this document.

79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and

Editor Note: The parameters PD Load and PD Mode selection are missing from Table 79-8 and 79-9. To scan 33.6 and verify that all variables related to DLL are defined in clause 79 and in Tables 79-8 and 79-9.

value (TLV) information elements

Table 79–6b—System setup value field

Bit	Function	Value/meaning																																																																																					
7:4	Power type	<table border="1"> <tr> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>= Type 4 PD</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>= Type 4 PSE</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>= Type 3 PD</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>= Type 3 PSE</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>= Type 2 PD</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>= Type 2 PSE</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>= Type 1 PD</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>= Type 1 PSE</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>= Reserved/Ignore</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>= Reserved/Ignore</td> </tr> </table>	7	6	5	4		1	1	1	1	= Reserved/Ignore	1	1	1	0	= Reserved/Ignore	1	1	0	1	= Reserved/Ignore	1	1	0	0	= Reserved/Ignore	1	0	1	1	= Reserved/Ignore	1	0	1	0	= Reserved/Ignore	1	0	0	1	= Type 4 PD	1	0	0	0	= Type 4 PSE	0	1	1	1	= Type 3 PD	0	1	1	0	= Type 3 PSE	0	1	0	1	= Type 2 PD	0	1	0	0	= Type 2 PSE	0	0	1	1	= Type 1 PD	0	0	1	0	= Type 1 PSE	0	0	0	1	= Reserved/Ignore	0	0	0	0	= Reserved/Ignore
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3	PD 4PID	1 = PD supports powering of both modes 0 = PD does not support powering of both modes																																																																																					
2	PD PI	1 = Physical layer P _{Class} PD is the sum of the indicated PD mode power class values. 0 = Physical layer P _{Class} PD is indicated by either PD mode power class values.																																																																																					
1	PD Load	1 = PD power demand on Mode A and Mode B are electrically isolated. 0 = PD power demand on Mode A and Mode B are not electrically isolated.																																																																																					
0	PD Mode selection	When power type is PD: 1 = PD requested power applies to Mode A pairset 0 = PD requested power applies to Mode B pairset When power type is PSE: 1 = PSE Allocated power applies to Alt-A pairset 0 = PSE Allocated power applies to Alt-B pairset																																																																																					

79.3.2.6b.5 PD Mode selection

This field shall be set according to Table 79–6b to select the Mode for which the PD is requesting power when the power type is PD. This field shall be set according to Table 79–6b to select the Alternative for which the PSE allocates power when the power type is PSE.
 This field shall be ignored.

End Of Proposed Baseline