Classification Margin and other Thoughts

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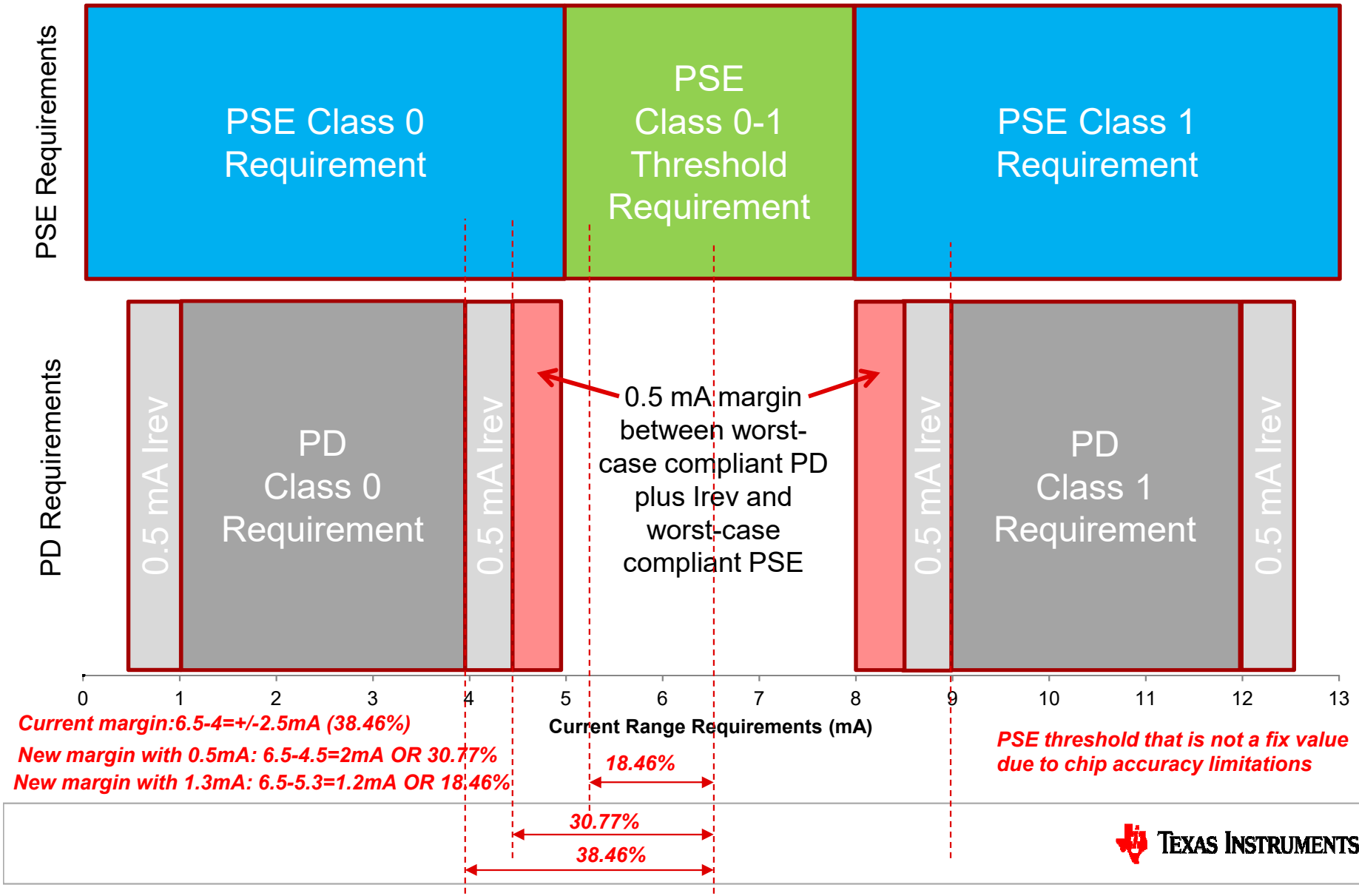
Yair Review of David Presentation. Please see my inputs.

Classification Margin

The problem; Legacy PDs that used to work well with Type 1 and Type 2 PSEs, now with Type 3 and 4 PSEs some will move to next class. ➔ Interoperability issues. See below how it happens. For new Type 3 and 4 PSE designs, in addition, it increases the requirements for PSE threshold accuracy range.



Classification Margin Thoughts

- There is an existing 1 mA of margin between the PD class signature requirements and the PSE class threshold requirements.
  - This applies for all classes (not just the classes shown on the previous slide).
  - This margin accounts only for leakage currents between the PD PI and the PSE PI.
    - Will be extremely close to zero, as the only thing between the PI is the cable (and connectors).
    - This margin is not the same as is needed for voltage thresholds as current does not change when flowing through resistance.

The intent was "grey area" and not cable leakage

The problem is not that margin. See previous slide.

- The amount of margin taken up by the "off" pairset is completely controlled by the PSE.
  - The "off" pairset pull-up resistance is a design choice. PSE implementers can choose a much higher value than 45 KΩ or can choose to remove it when performing class on the other pairset. There are many solutions.
  - The 0.467 mA maximum requirement for current sourced onto the negative pair (for below 21 V) makes sure that PSE implementers who do not consider this are still safe.

Yes, but PSE has other requirements to meet. When we specified 802.3af and at, we thought about these considerations and now you propose to violate them and create new problems. See previous slide.

Incorrect assumptions. High resistance creates other problems (slow discharge of Cpd. And you ignore interoperability issues.

It helps compare to 1.3mA but still you didn't solve the interoperability issues.

Other Thoughts

- Splitting the Irev requirement into two voltage ranges and limiting it to sourced current on the negative pair allows for the simplest specification on both the PSE and the PD.
  It helps compare to 1.3mA but still you didn't solve the interoperability issues.
  - There is no situation in which the PSE should source any significant current on the negative pair.
    still you didn't solve the interoperability issues.
    - Thus, this requirement can be written independent of operating mode.
  - This allows the PD requirement for backfeed (2.8 V with a 100 KΩ resistor) to be limited to 10.1V.
    This problem is irrelevant to the 100K. The problem is when the ideal diode bridge is on, the 45K is directly in parallel to Iclass. No diode Rrev resistance to help. See backfeed model in darshan_01_0518.pdf annex B
    - Even if the backfeed spec was applied up to 21 V, there is still no guarantee of interoperability as the backfeed spec is specific to a 100K resistor.
      - The current on the "off" Mode is unspecified with any other resistor value.
- Devices that backfeed during 3-pair classification exist in the world and are compliant to Type 1 or Type 2.
  Yes…I am using the same argument on PDs that was OK with legacy PDs and now will fail in Type 3 and 4 PSEs… See first slide.
  - PSEs will have to find a way to deal with the backfeed during 3-pair classification.
    - The lower Irev spec for the class range is a way to make sure this happens.
      PDs too.
  - Is there enough justification to outlaw it despite the fact that this situation will have to be dealt with?
    YES. See all my inputs above