Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3 Powered devices (PDs)

33.3.1 PD PI A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

Type 1 and Type 2 PDs shall be capable of accepting power on either of two pairsets and may accept power on both pairsets. Type 3 and Type 4 PDs shall be capable of accepting power on either pairset and shall be capable of accepting power on both pairsets. The two pairsets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power modes.

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that are not implemented to be insensitive to polarity, are specifically not allowed by this standard

The PD shall not source power on its PI. The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{PD}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.2 PD Type descriptions

PDs can be categorized as either Type 1, Type 2, Type 3/SS, Type 3/DS, Type 4/SS or Type 4/DS. Table 33–13a shows the permissible PD types along with supported parameters.

Table 133–2—Permissible PD Types

PD Type	PD Class	4-pair Capable	Low MPS support[1]	Physical Layer Classification	Data Link Layer Classification	Other Optional Features
Type 1	0-3	Optional	No	Single-Event	Optional	
Type 2	4	Optional	No	Multiple Event	Mandatory	
Type 3/SS	1-6	Mandatory	Yes[2]	Multiple Event	Mandatory[3]	Autoclass
Type 3/ DS	1-4	Mandatory	Yes[2]	Multiple Event	Mandatory	Autoclass
Type 4/SS	7-8	Mandatory	Yes[2]	Multiple Event	Mandatory	Autoclass
Type 4/ DS	5	Mandatory	Yes[2]	Multiple Event	Mandatory	Autoclass

[1] - Refer to Section 33.3.8 for details. "Low" means lower standby MPS power, "high" means higher standby MPS power.
[2] - Need to support High MPS when connected to Type 1 or Type 2 PSEs for backward compatibility.
[3] - Type 3/SS Class 1-3 PDs are not required to implement DLL classification.

Type 1 PDs implement a minimum of EventSingle-Event Physical Layer classification and advertise a Single-Event Class signature of 0, 1, 2, or 3. Class 0 is only permitted for Type 1 PDs.

Type 2 PDs implement both Multiple-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6) and advertise a Multiple-Event Class signature of 4 during all Class events.

Type 3/SS PDs operating up to a maximum power draw corresponding to Class 3 or less implement a minimum of Multiple-Event Physical Layer Classification and advertise a Single-Event Class signature of 1,2, or 3.

Type 3/SS and Type 4/SS PDs operating with a maximum power draw corresponding to Class 4 or greater implement both Multiple-Event Physical Layer classification (see 133.3.5.2) and Data Link Layer classification (see 33.6). Such Type 3 PDs advertise a Class signature of 4, 5, or 6, while Type 4 PDs advertise a Class signature of 7 or 8.

Type 3/DS and Type 4/DS PDs implement a minimum of Multiple-Event Physical Layer classification and Data Link Layer Classification (see 33.6). Type 3/DS PDs advertise a Class signature of 1, 2, 3, or 4 on each pairset, while Type 4/DS PDs advertise a Class signature of 5 on at least one pairset.

Type 4/SS PDs only advertise Class 7 and 8. Type 4/DS PDs advertise Class 5 on at least one pairset.

A Type 2, Type 3 or Type 4 PD that does not successfully observe a Multiple-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

Type 2, Type 3 and Type 4 PDs implementing 100BASE-TX (Clause 25) PHYs shall meet the requirements of 25.4.5 in the presence of (Iunb / 2).

Note - For PDs implementing both Clause 25 and Clause 33, this adds the unbalance current to the requirements in Clause 25.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.3.2 Constants

The PD state diagram uses the following constants:

VReset_th
: Reset voltage threshold (see Table 33–17)

VMark_th
: Mark event voltage threshold (see Table 33–17)

class_sig
: PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required

A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.

Values:FALSE:PD functionality is disabled.

TRUE:PD functionality is enabled.

pd_multi-event

A control variable indicating whether the PD presents a Multiple-Event Class signature.

Values:FALSE:PD does not present a Multiple-Event Class signature.

TRUE:PD does present a Multiple-Event Class signature.

pd_dll_capable

This variable indicates whether the PD implements Data Link Layer classification.

Values:FALSE:The PD does not implement Data Link Layer classification.

TRUE:The PD does implement Data Link Layer classification.

pd_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled.

Values:FALSE:Data Link Layer classification is not enabled.

RUE:Data Link Layer classification is enabled.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

pd_max_power

A control variable indicating the max power that the PD may draw from the PSE. See power

classifications in Table 33–18.

Values:

0: PD may draw Class 0 power

1: PD may draw Class 1 power

2: PD may draw Class 2 power

3: PD may draw Class 3 power

4: PD may draw Class 4 power

5: PD may draw Class 5 power

6: PD may draw Class 6 power

7: PD may draw Class 7 power

8: PD may draw Class 8 power

pd_reset

An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.

Values:FALSE:The device has not been reset (default).

TRUE:The device has been reset.

power_received

An indication from the circuitry that power is present on the PD's PI.

Values:FALSE:The input voltage does not meet the requirements of VPort_PD in Table 33–18.

TRUE:The input voltage meets the requirements of VPort_PD.

present_class_sig_A

Controls presenting the classification signature that is used during first two Class events (see 133.3.5) by the PD.

Values:FALSE:The PD classification signature is not to be applied to the link.

TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B

Controls presenting the classification signature that is used during the third Class event and all subsequent Class events (see 133.3.5) by the PD.

Values:FALSE:The PD classification signature is not to be applied to the link.

TRUE:The PD classification signature is to be applied to the link.

present_det_sig

Controls presenting the detection signature (see 133.3.4) by the PD.

Values:FALSE:A non-valid PD detection signature is to be applied to the link.

TRUE:A valid PD detection signature is to be applied to the link over each pairset.

present_mark_sig

Controls presenting the mark event current and impedance (see 133.3.5.2.1) by the PD.

Values:FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mps
Controls applying MPS (see) to the PD's PI.
Values:FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

pse_dll_power_level
A control variable output by the PD power control state diagram (Figure 33–28) that indicates the power level of the PSE by which the PD is being powered.
Values:1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5 or Class 6 power.
4: The PSE has allocated Class 7 or Class 8 power.

pse_power_level
A control variable that indicates to the PD the level of power the PSE is supplying.
Values:1: The PSE has allocated the PD's requested power or Class 3 power, whichever is less
2: The PSE has allocated the PD's requested power or Class 4 power, whichever is less
3: The PSE has allocated the PD's requested power or Class 6 power, whichever is less.
4: The PSE has allocated the PD's requested power or Class 8 power, whichever is less.

VPD
Voltage at the PD PI as defined in 1.4.422.

133.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer
A timer used to prevent the Type 2, 3, or 4 PD from drawing more than inrush current during the PSE's inrush period; see Tdelay-2P in Table 33–18.

33.3.3.4a Functions

do_class_timing
This function is used by a Type 3 or Type 4 PD to evaluate the type of PSE connected to the link by measuring the length of the classification event. The classification event timing requirements are defined in Table 33–17. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use.
Values: TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.3.5 State diagrams

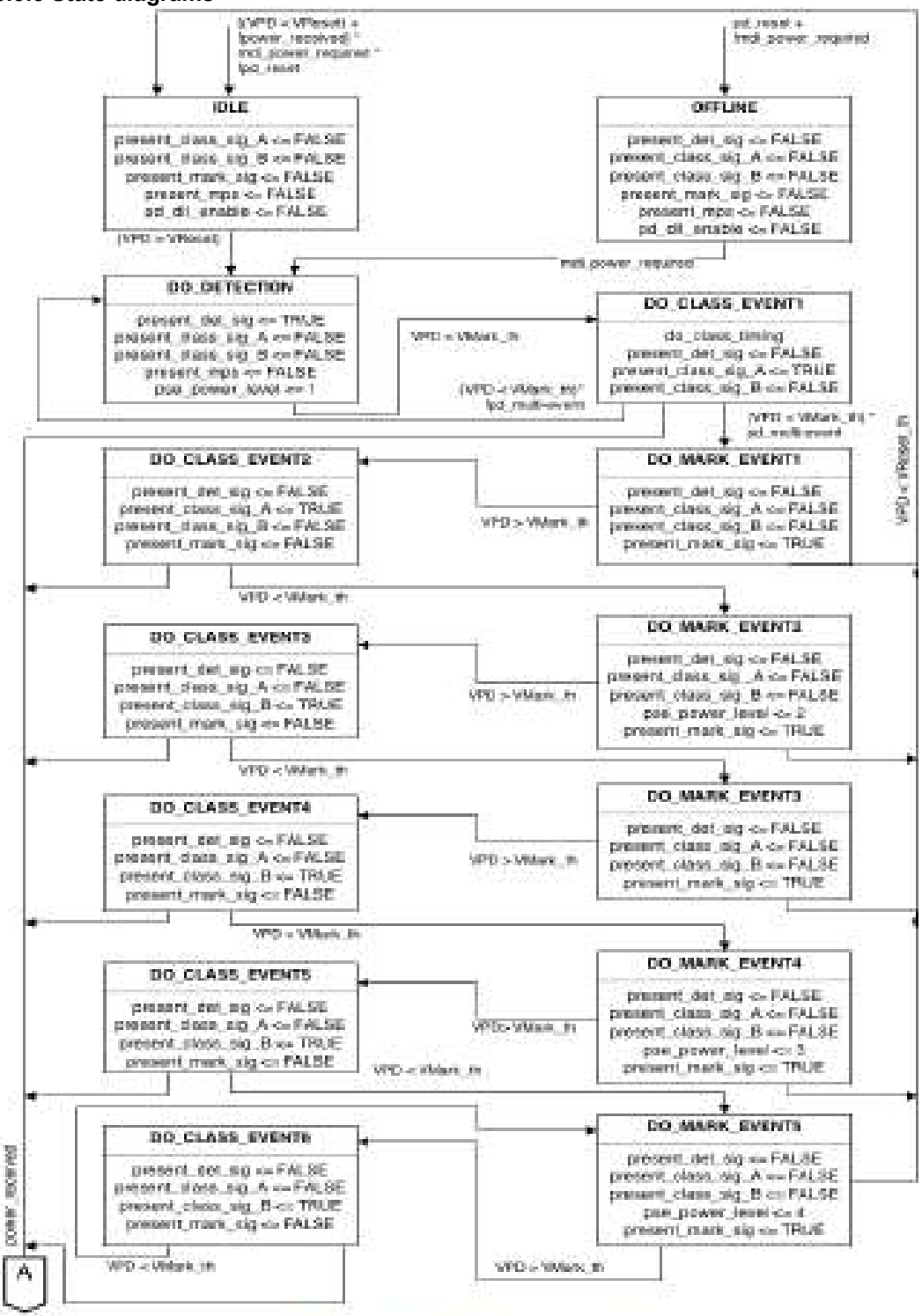

Figure 33–16—PD state diagram

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

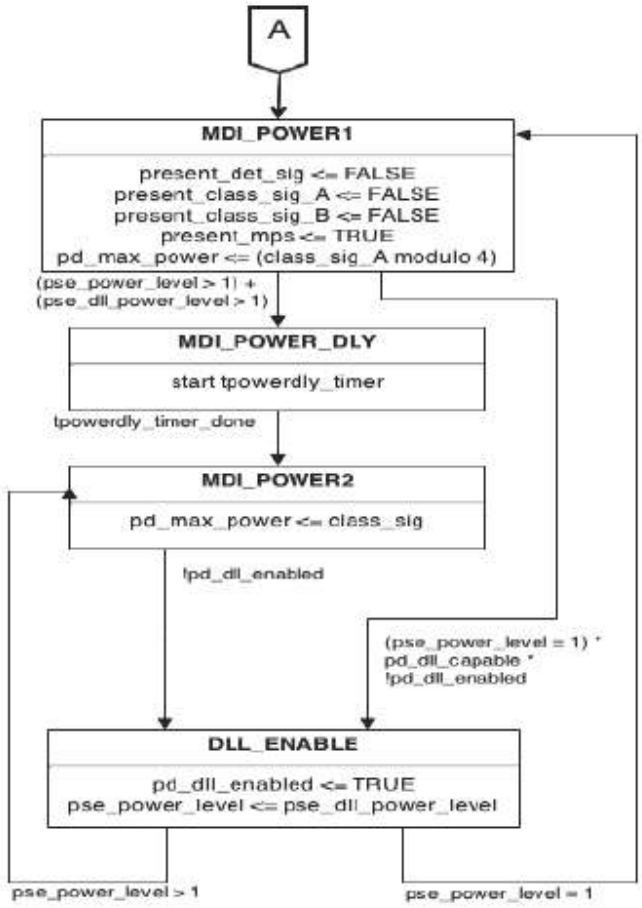

Figure 133–2—PD state diagram (*continued*)

NOTE 1—DO_CLASS_EVENT6 creates a defined behavior for a Type 2, Type 3 and Type 4 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

133.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 133–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 133–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive VPD and Negative VPD of PD Mode A and PD Mode B as defined in 133.3.1.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

A Type 1, Type 2, or single-signature Type 3 or Type 4 PD that is powered over only one pairset shall present a non-valid detection signature on the unpowered pairset. A dual-signature Type 3 or Type 4 PD that is powered over only one pairset shall present a valid detection signature on the unpowered pairset.

Any PD may indicate the ability to accept power on both pairsets using TLV variable PD 4P-ID in Table 79– 6b or TBD

A PD may or may not present a valid detection signature when in the IDLE state.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process as defined in Equation (133–1).

$$R_{detect} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (133\text{–}1)$$

where

V_1 and V_2 are the first and second voltage measurements made at the PD PI, respectively

I_1 and I_2 are the first and second current measurements made at the PD PI, respectively

R_{detect} is the effective resistance

A valid PD detection signature shall have the characteristics of Table 133–3.

A non-valid detection signature shall have one or both of the characteristics in Table 133–4.

A PD that presents a signature outside of Table 133–3 is non-compliant, while a PD that present the signature of Table 133–4 is assured to fail detection.

Table 133–3—Valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Minimum	Maximum	Unit
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.70 V to 10.1 V	23.7	26.3	kΩ
V offset	See Figure 133–3	0	1.90	V
Voltage at the PI	I_{Port} = 124 µA	2.70		V
Input capacitance	2.70 V to 10.1 V	0.050	0.120	µF
Series input inductance	2.70 V to 10.1 V		0.100	mH

Table 133–4—Non-valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Range of values	Unit
R_{detect}	V < 10.1 V	Either greater than 45.0 or less than 12.0	kΩ
Input capacitance	V < 10.1 V	Greater than 10.0	µF

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

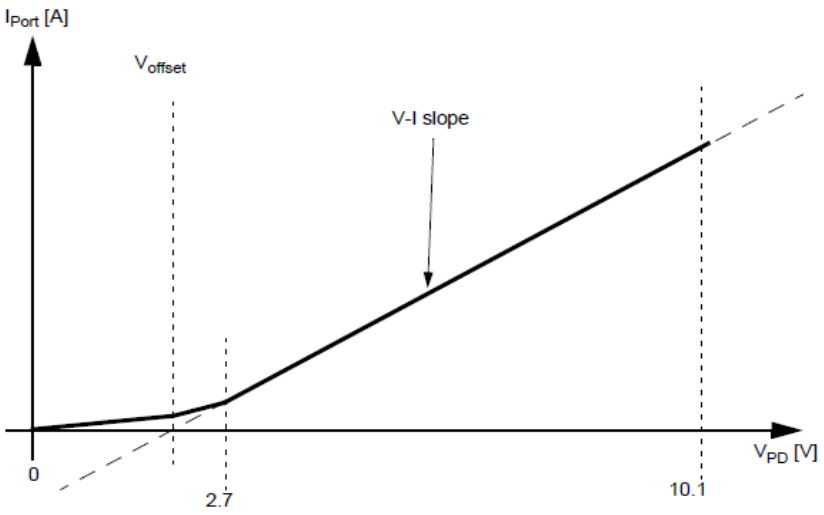

Figure 33–17—Valid PD detection signature offset

33.3.5 PD classifications

See 33.2.6 for a general description of classification mechanisms.

The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.

A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer (DLL) classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2, Type 3 and Type 4 PSEs and Type 2, Type 3 and Type 4 PDs.

The method of classification depends on the type of the PD and the type of the attached PSE.

A PD shall meet at least one of the allowed classification configurations listed in Table 33–15a.

A Type 1 PD may implement any of the Class signatures in 33.3.5 and 33.6.

Type 2, Type 3, and Type 4 PDs at Class 4 or greater power levels shall implement both Multiple-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

Table 33–15a—PD Classification configurations

PD Classification Configurations		
Type 1 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Valid	Valid
Single-Event	Valid	Valid
None	Invalid	Invalid
Type 2 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Invalid	Valid
Single-Event	Invalid	Invalid
None	Invalid	Invalid
Type 3, Type 4 PD		
Physical Layer	**No DLL**	**DLL**
Multiple-Event	Invalid[1]	Valid
Single-Event	Invalid	Invalid
None	Invalid	Invalid

[1]Single-signature PDs not capable of drawing more than Class 3 power levels may omit Data Link Layer classification (see 33.6)

33.3.5.1 PD Single-Event Class signature

Class 0 is the default for Type 1 PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

PDs implementing a Multiple-Event class signature shall return class_sig_A in accordance with the maximum power draw, PClass_PD, as specified in Table 33–16a and the responses specified in Table 33–16a.

Type 3 PDs operating with a maximum power draw corresponding to Class 1-3 respond to Single-Event classification by returning a Class signature 1, 2, or 3 in accordance with the maximum power draw, PClass_PD.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

Since Single-Event classification is a subset of Multiple-Event classification, Type 2, Type 3, and Type 4 PDs operating with a maximum power draw corresponding to Class 4 or higher, respond to classification with a Class 4 signature.

Type 1 PDs may choose to implement a Multiple-Event Class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, PClass_PD.

The Type 2, Type 3 and Type 4 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. Type 1 and Type 2 PDs shall present one, and only one, classification signature during classification.

Table 33–16—Classification signature, measured at PD PI

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class Signature 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class Signature 0 (Type 3)	14.5 V to 20.5 V	1.00	4.00	
Current for Class Signature 1	14.5 V to 20.5 V	9.00	12.0	
Current for Class Signature 2	14.5 V to 20.5 V	17.0	20.0	
Current for Class Signature 3	14.5 V to 20.5 V	26.0	30.0	
Current for Class Signature 4	14.5 V to 20.5 V	36.0	44.0	

33.3.5.2 PD Multiple-Event Class signature

PDs shall present class_sig_A during DO_CLASS_EVENT1 and DO_CLASS_EVENT2 and class_sig_B during DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5 and DO_-CLASS_EVENT6, as defined in Table 133–7a.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

Table 33–16a—Physical Layer Classifications and Multiple Event Responses

PD Type	PD Signature	Class	class_sig_A	class_sig_B	P_{Class_PD} (W)
1	.	0	0	0	13.0
		1	1	1	3.84
		2	2	2	6.49
		3	3	3	13.0
2	.	4	4	4	25.5
3	Single-signature	1	1	1	3.84
		2	2	2	6.49
		3	3	3	13.0
		4	4	4	25.5
		5	4	0	40.0
		6	4	1	51.0
	Dual-signature	1	1	0	3.84
		2	2	0	6.49
		3	3	0	13.0
		4	4	0	25.5
4	Single-signature	7	4	2	62.0
		8	4	3	71.0
	Dual-signature	5	4	3	35.5

The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

Until successful Multiple-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2, Type 3 and Type 4 PD's pse_power_level state variable is set to '1'.

A Type 2, Type 3 and Type 4 PDs shall conform to the electrical requirements as defined by Table 33–18 for the level defined in the pse_power_level state variable.

Dual-signature PDs shall advertise a Class signature of 1, 2, 3, 4, or 5 on each pairset. The Class advertised on each pairset is the power requested by the PD on that pairset. Dual-signature PDs may advertise a different Class signature on each pairset. It is not recommended to use different Class signatures if the dual-signature PD powers a single electrical load.

Type 3 and Type 4 PDs may determine if the PSE they are connected to supports low MPS by measuring the length of the first class event. The default value for short_mps is FALSE. If it chooses to implement

low MPS, a PD may set short_mps to TRUE if the first class finger is longer than TLCF_PD min and shall set short_mps to TRUE if the first class finger is longer than TLCF_PD max.

NOTE : See Table 33–16 for definition of Class signatures 1-4.

Table 33-17 —Multiple-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 133.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 133.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 133.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 133.3.5.2.1
7	Long first Class event timing	T_{LCF_PD}	ms	75.5	87.5	See 133.3.8

33.3.5.2.1 Mark Event behavior

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw IMark as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the IMark current limits when voltage at the PI enters the VMark specification as defined in Table 33–17.

VMark_th is the PI voltage threshold at which the PD implementing Multiple-Event Class signature transitions into and out of the DO_CLASS_EVENT1, or DO_CLASS_EVENT2, DO_CLASS_EVENT3, DO_CLASS_EVENT4, DO_CLASS_EVENT5 or DO_CLASS_EVENT6 states as shown in Figure 33–16.

The PD shall draw IMark until the PD transitions from a DO_MARK_EVENT state to the IDLE state.

VReset_th is the PI voltage threshold at which the PD implementing Multiple-Event Class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

33.3.5.3 Autoclass

Type 3 and Type 4 PDs may choose to implement an extension of Physical Layer classification known as Autoclass. The purpose of Autoclass is to allow the PSE to determine the actual maximum power draw of the connected PD. See Annex 33C for more information on Autoclass.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

A PD implementing Autoclass shall respond to Physical Layer classification as specified in 33.3.5.1 and 33.3.5.2 with the exception that the PD shall change its current during the first class event to class signature '0' no earlier than TACS min and no later than TACS max (as defined in Table 33–17a).

After power up, a PD implementing Autoclass shall draw its highest required power, subject to the requirements on PClass_PD in 33.3.7.2, throughout the period bounded by TAUTO_PD1 and TAUTO_PD2, measured from when VPort_PD rises above VPort_PD min. The PD shall not draw more power than the power consumed during the time from TAUTO_PD1 to TAUTO_PD2 (as defined in Table 33–17a) at any point until VPort_PD falls below VReset_th, unless the PD successfully negotiates a higher power level, up to the advertised Physical Layer classification, through Data Link Layer classification as defined in section 33.6.

Table 33–17a—Autoclass PD timing requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Autoclass signature timing	T_{ACS}	ms	75.5	87.5	Measured from transition to state DO_CLASS_EVENT_1
2	Autoclass power draw start time	T_{AUTO_PD1}	s		1.35	Measured from when V_{Port_PD} rises above V_{Port_PD} min
3	Autoclass power draw end time	T_{AUTO_PD2}	s	3.65		Measured from when V_{Port_PD} rises above V_{Port_PD} min

33.3.6 PSE Type identification

A PD shall identify a PSE Type as a Type lower or equal to its own Type.

A PD connected to a higher PSE Type than its own may identify that PSE as its own Type.

The default value of pse_power_level is 1. After a successful Multiple-Event Physical Layer classification has completed the pse_power_level is set to either 2, 3, or 4. After a successful Data Link Layer classification has completed, the pse_power_level is set to either 1, 2, 3 or 4.

The PD resets the pse_power_level to '1' when the PD enters the DO_DETECTION state.

33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage per pairset						
	Class 1	V_{Port_PD-2P}	V	42.1	57.0	1,3	See 133.3.7.1, Table 33–1
	Class 2			40.8		1,3	
	Class 0, 3			37.0		1,3	
	Class 4			42.5		2,3	
	Class 5, single-signature			44.3		3	
	Class 5, dual-signature			41.2		4	
	Class 6			42.5		3	
	Class 7			42.9		4	
	Class 8			41.2		4	
2	Transient operating input voltage per pairset	V_{Tran_lo-2P}	V	36.0		2,3,4	For time duration defined in 33.2.7.2
3	Input voltage range per pairset during overload	$V_{Over-load-2P}$	V	41.4	57.0	2,3	See 133.3.7.4, Table 33–1
				39.5		4	
4	Input average power	P_{Port_PD}	W		P_{Class_PD}[1]	All	See 133.3.7.2, Table 33–1, Table 133–7a
5	Input inrush current per pairset	$I_{In-rush\_PD-2P}$	A		0.400	All	Peak value—See 133.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2,3,4	See 133.3.7.3 single-signature PDs only
6a	Inrush to operating state delay per pairset	$T_{delay-2P}$	s	0.080		3,4	Dual-signature PDs only

Missing line for item 3 (36V min) for type 1.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

Table 33–18—PD power supply limits *(continued)*

Items 7-13.

- The same concept
- Same amount of rows
- PD Type columns include information regarding Type 1 and 2 PDs…

33.3.7.1 Input voltage

The specification for $V_{Port\_PD\text{-}2P}$ in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD\text{-}2P} = V_{PSE\text{-}2P} – (R_{Chan} \times I_{Port\text{-}2P})$.

The PD shall turn on at a voltage less than or equal to VOn_PD. After the PD turns on, the PD shall stay on over the entire VPort_PD-2P range. The PD shall turn off at a voltage less than VPort_PD-2P minimum and greater than or equal to VOff_PD.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by VPort_PSE-2P min to VPort_PSE-2P max (as defined in Table 33–11) with a series resistance within the range of valid Channel Resistance.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.7.2.1 System stability test conditions during startup and steady state operation

$P_{Port\_PD} = V_{Port\_PD} \times I_{Port}$ Eq 33-9

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–9):

where P_{Port_PD} is the average input power at the PD PI V_{Port_PD} is the static input voltage at the PD PI I_{Port} is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with Vport_PD-2P requirements as defined in Table 133–7a, and ending when CPort has reached a steady state and is charged to 99% of its final value. This period shall be less than TInrush-2P min per Table 33–11. PDs shall consume a maximum of Class 3 power for at least Tdelay-2P min. This allows the PSE to properly compete inrush.

Tdelay-2P for each pairset starts when VPD-2P crosses the PD power supply turn on voltage, VOn_PD. This delay is required so that the Type 2, Type 3 and Type 4 PDs does not enter a high power state before the PSE has had time to switch current limits on each pairset from IInrush-2P to ILIM-2P.

Input inrush current at startup is limited by the PSE if CPort per pairset < 180 µF, as specified in Table 33–11.
If CPort per pairset >=180 µF, input inrush current shall be limited by the PD so that IInrush_PD per pairset max is satisfied.

NOTE— PDs may be subjected to PSE POWER_ON current limits during inrush when the PD input voltages reaches 99% of steady state or after Tinrush-2p min. See 33.2.7.4 for details.
CPort in Table 33–18 is the total PD input capacitance during POWER_UP and POWER_ON states that a PSE sees when connected to a single-signature PD over a pairset or both pairsets. When PSE is connected to dual-signature PDs, CPort value requirements are specified in 33.3.7.6.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.7.4 Peak operating power

$V_{Overload\text{-}2P}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, with the exception of Class 6 or Class 8 PDs, the peak power shall not exceed P_{Class_PD} max for more than $T_{CUT\text{-}2P}$ min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

For Class 6 and Class 8 PDs in any operating condition with any static voltage at the PI, the peak power shall not exceed P_{Class} at the PSE PI for more than T_{CUT} min, as defined in Table 33–11 and with 5% duty cycle.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max, or P_{Class} at the PSE PI for Class 6 and Class 8 PDs.

The RMS, DC and ripple current shall be bounded by Equation (33-10):

$$I_{Port} = \left(\sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2}\right)_A \qquad \textbf{33-10}$$

where

I_{Port}	is the RMS input current
I_{Port_dc}	is the DC component of the input current
I_{Port_ac}	is the RMS value of the AC component of the input current

The maximum I_{Port} value for all PDs except those in Class 6 or Class 8, over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation (33–4).

$$I_{portmax} = \left\{\frac{P_{Class\_PD}}{V_{Port\_PD\text{-}2P}}\right\}_A \qquad (33\text{-}11)$$

where

*I*portmax is the maximum DC and RMS input current

*V*Port_PD-2P is the voltage minimum specified input voltage at a PD pairset.

*P*Class_PD is the maximum power, *P*Class_PD max, as defined in Table 33–18

The maximum I_{Port} value for all PDs in Class 6 or Class 8, over the operating $V_{Port\_PD\text{-}2P}$ range shall be defined by Equation **33-11a:**

$$I_{portmax} = \left\{\frac{P_{Class}}{V_{PSE}}\right\}_A \qquad \textbf{33-11a}$$

where

$I_{portmax}$	is the maximum RMS input current
P_{Class}	is the allocated Class power as defined in 33.2.6 and Equation (33–3)
V_{PSE}	is the voltage at the PSE PI as defined in 1.4.426

Peak power, *P*Peak_PD, for Class 4 is based on Equation (33–12). Peak power, *P*Peak_PD, for Class 5 through 8 is based on Equation (33–12a). Equation (33–12) and Equation (33–12a) are used to approximates the ratiometric peak powers of Class 0 through Class 8. This equation may be used to

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

calculate peak operating power for *P*Peak_PD values obtained via Data Link Layer classification or Autoclass.

$$P_{Peak\_PD} = \{1.11 \times P_{Class\_PD}\}_W \quad (33\text{–}12)$$

$$P_{Peak\_PD} = \{1.05 \times P_{Class\_PD}\}_W \quad (33\text{–}12a)$$

where

P_{Peak_PD} is the peak operating power

P_{Class_PD} is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

33.3.7.5 Peak transient current

When the input voltage at the PI is static and in the range of V_{Port_PD} defined by Table 33–18, the transient current drawn by a single-signature PD shall not exceed 4.70 mA/µs in either polarity. A dual-signature PD shall not exceed 4.70 mA/us in either polarity per pairset under the same conditions. This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected.

Under normal operating conditions when there are no transients applied at the PD PI, Class 6 or Class 8 PDs, shall operate below the PD extended template defined in Figure 33-18. PDs of all other the PD shall operate below the PD upperbound template defined in Figure 33–18. See 33.3.7.2 for details on Class 6 and Class 8 PD allowances.

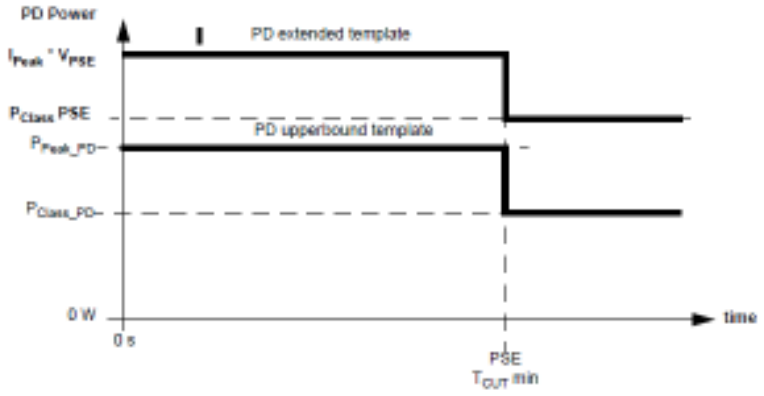

Figure 33–18—PD static operating mask

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–13):

$$P_{PDUT}(t) = \left\{ \begin{array}{ll} P_{Peak\_PD} & \text{for } (0 \le t < T_{cutmin}) \\ P_{Class\_PD} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_W \quad (33\text{–}13)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
P_{Peak_PD}	is the peak operating power, P_{Peak_PD} max, as defined in Table 33–18
P_{Class_PD}	is the maximum power, P_{Class_PD} max, as defined in Table 33–18
T_{cutmin}	is $T_{CUT\text{-}2P}$ min, as defined in Table 33–11

The PD extended template in Figure 33-18, P_{PDET}, is described by Equation (33-13a):

$$P_{PDET}(t) = \left\{ \begin{array}{ll} I_{Peak} \times V_{PSE} & \text{for } (0 \le t < T_{cutmin}) \\ P_{Class} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_W \quad (33\text{–}13a)$$

where

t	is the duration in seconds that the PD sinks I_{Port}
I_{Peak}	is the peak operating current, I_{Peak} max, as defined in Equation (33–4)
V_{PSE}	is the voltage at the PSE.
P_{Class}	is the minimum power output by the PSE, as defined in Table 33-7 and Section 33.2.6
T_{cutmin}	is $T_{CUT\text{-}2P}$ min, as defined in Table 33–11

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least *T*LIM-2P min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

A PD shall continue to operate without interruption in the presence of transients at the PSE PI as defined in 33.2.7.2. A single-signature PD shall include Cport as defined in Table 33–18 item 9. A dual-signature PD shall meet this requirement for each pairset.

PDs with power draw greater than Class 4 may require extra capacitance to maintain operation during PSE transients. Class 5 and 6 single-signature PDs will meet the requirement with Cport ≥ 10µF. Class 5 dual-signature PDs should include these Cport values at each pairset. Class 7 and 8 single signature PDs will meet this requirement with Cport ≥ 20µF.

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.

A Type 2 or Type 3 PD with peak power draw that does not exceed *P*Class_PD max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI.

A Type 4 PD with peak power draw that does not exceed PClass PD max and has an input capacitance of 360µF or less requires no special considerations with regards to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after TLIM min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a RCh resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from VPort_PSE min to VPort_PSE max at 2250 V/s.

A Type 2 or Type 3 PD that demands less than Class 5 power levels shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from VPort_PSE min to VPort_PSE min+2.5 V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 ohm, and a source that supports a current greater than 2.5 A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives VPD from VPort_PSE min to 56 V at 2250 V/s, the source impedance within 2.5% of RCh (see Table 33–1), and the voltage source limits the current to MDI ILIM-2P per Equation (33–14).

The current limit per pairset at the MDI (MDI ILIM-2P) is defined by Equation (33–14):

Eq 33-14……. (33–14)

where

*pse*ILIM-2Pmin is the PSE ILIM-2P min as defined in Table 33–11
*mdi*ILIM-2P is the per pairset current limit at the MDI (MDI ILIM)

A Type 3 PD that demands Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 2.5A and shall settle below the PD upperbound template value (see Figure 33-18) within 4ms. During the test, both PD Modes voltages are driven from VPort_PSE min to VPort_PSE min + 2.5V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 ohm and a source that supports a current greater than 5.0A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56V at 2250V/µs, the source impedance within 2.5% of RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM-2P per Equation (33-14).

A Type 3 or Type 4 PD that demands more than Class 5 power levels shall meet both of the following:

a) The PD mode input current spike shall not exceed 3.0A and shall settle below the PD extended template value (see Figure 33-18) within 4ms. During the test, both PD Modes voltages are driven from VPort_PSE min to VPort_PSE min + 2.5V at greater than 3.5 V/µs, a source impedance within 2.5% of 1.5 ohm and a source that supports a current greater than 5.0A.

b) The PD shall not exceed the PD upperbound template beyond TLIM min under worst-case current draw under the following conditions. The input voltage source drives both PD Modes from VPort_PSE min to 56V at 2250V/µs, the source impedance within 2.5% of RCh (see Table 33-1), and the voltage source limits the current to MDI ILIM-2P per Equation (33-14).

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

33.3.7.7 Ripple and noise

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of VPort_PD-2P, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

33.3.7.8 PD classification stability time

Following a valid detection and a rising voltage transition from Vvalid to VClass, the PD Physical Layer clas-sification signature shall be valid within Tclass as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

Following a valid detection and a rising voltage transition from V_{valid} to V_{Class}, the PD Physical Layer clas-sification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kohm load resistor

33.3.7.10 PD PI pair-to-pair resistance and current unbalance

All Class 5 and higher PDs shall not exceed $I_{con\text{-}2P\text{-}unb}$ as defined in Table 33–11 on any pair. PDs shall meet this requirement when connected to a common source voltage through a resistance of R_{source_min}=0.16 Ω ± 1% and R_{source_max}=0.19 Ω ± 1% to PD PI pairs of the same polarity for all PD operating conditions as shown in Figure 33–18a. R_{source_min} and R_{source_max} represent the V_{in} source impedance that consists of the PSE PI components (R_{Pair_min} and R_{Pair_max} as specified in 33.2.7.4.1) and the channel resistance. I_A and I_B are the pair currents of pairs with the same polarity. See Annex 33A.5 for design guide lines for meeting the above requirements.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

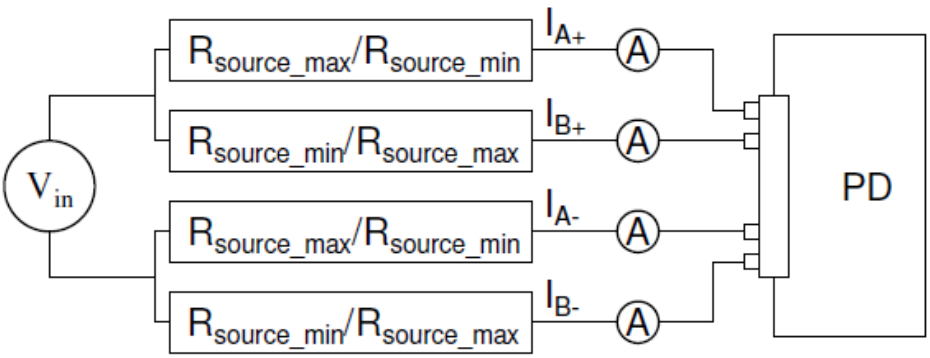

Figure 33–18a—PD PI pair-to-pair test circuit

R_{pair_max} and R_{pair_min} represents PSE and channel effective source impedance that includes the effect of $V_{Port\_PSE\_diff}$ as specified in Table 33–11.

33.3.8 PD Maintain Power Signature

A PD that requires power from the PI shall provide a valid Maintain Power Signature (MPS) at the PI. A PD that does not maintain the MPS components mentioned above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

The MPS shall consist of current draw equal to or above I_{port_MPS} for a minimum duration of T_{MPS_PD} measured at the PD PI followed by an optional MPS dropout for no longer than T_{MPDO_PD}. The values of I_{port_MPS}, T_{MPS_PD}, and T_{MPDO_PD} are shown in Table 33–1a. A Type 1 or Type 2 PD, or a PD which does not detect a long first class event, shall in addition show the input impedance with resistive and capacitive components defined in Table 33–1.

Type 3 and Type 4 PDs that detect a long first class event in the range of TLCF_PD may reduce TMPS_PD in order to draw a lower standby MPS power. In absence of a long first class event the minimum TMPS_PD is higher, and the standby MPS power is also higher.

A Type 3 or Type 4 PD shall have TMPS_PD measured with a series resistance representing the worst case cable resistance between the measurement point and the PD PI.

PDs using Autoclass shall use the Iport_MPS associated with the PD Class assigned by the PSE during Physical Layer classification.

See Annex 33F for PD design guidelines for MPS behavior.

Powered PDs that no longer require power, and identify the PSE as Type 1 or Type 2, shall remove both the current draw and impedance components of the MPS. To cause Type 1 and Type 2 PSE power removal,

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

the impedance of the PI should rise above Zac2 as specified in Table 33–12. Powered PDs that no longer require power, and identify the PSE as Type 3 or Type 4, shall remove the current draw component and may remove the impedance components of the MPS.

Table 33-19 - PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input resistance	R_{pd_d}	kΩ		26.3	
2	Input capacitance	C_{pd_d}	µF	0.050		See Table 33–12

Table 33–1a—PD DC Maintain Power Signature

Item	Parameter	Symbol	Units	Min	Max	PD Type	Conditions
1	Input Current	I_{Port_MPS}	A	0.01		1-4	- All Type 1 and Type 2 PDs and Type 3 single-signature PDs with P_{class_PD} ≤ PD Class 4 power limit. - Total PD current is sum of both pairsets.
				0.016		3, 4	- Single-signature PDs with P_{class_PD} > PD Class 4 power limit. - Total PD current is sum of both pairsets.
				0.008		3, 4	- Dual-signature PDs - Applies to each powered pairset.
2	PD Maintain Power Signature Time	T_{MPS_PD}	ms	75		1, 2	
						3, 4	short_mps = FALSE
				7		3, 4	short_mps = TRUE
3	PD Drop Out Period	T_{MPDO_PD}	ms		250	1, 2	
						3, 4	short_mps = FALSE
					310	3, 4	short_mps = TRUE

NOTE—PDs may not be able to meet the I_{Port_MPS} specification in Table 33–1a during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Cb}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

Simulation of: What if the PD spec part will stay in one chapter and include all types.
PD spec: 24 pages, and 29 pages for 33.4 through 33.8.

The following are additional clauses (29) pages including (that will be doubled if we use two PoE chapters):

33.4 Additional electrical requirements

33.4.1 Isolation

33.4.2 Fault tolerant

33.4.3 Impedance unbalance

33.4.4 CM…..

33.4.5 P2P NOISE

33.4.6 DIFF NOISE

33.4.9 Midspan Requirements

33.5. Management

33.6 DLL

33.7.6 EMC

33.3.7 TEMP

33.7.7 Labling

33.8 PICS