Table 79–6—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	~~Power = 0.1 × (decimal value of bits) Watts.~~ Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 255999.

~~where~~

~~*Power* is the effective allocated PSE power value~~

~~*X* is the decimal value of the power value field, bits 15:0~~

"PSE allocated power value" is the maximum input average power (see 33.3.8.2 and 145.3.8.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the input to the PD's PI. The PSE uses this value to compute P_{Class} defined in 33.2.7 and 145.2.7.

Not part of the changes:
1. Sections related to DS devices only do not indicate this. Therefore the text incorrectly applies to all devices.
2. Some DS cross references are incorrect.
3. Values for Type 1,2 and SS devices are not provided.

Insert 79.3.2.6a through 79.3.2.6f after 79.3.2.6 as follows:

79.3.2.6a Dual-signature PD requested power value Mode A and Mode B

The "Dual-signature PD requested power value Mode A and Mode B" field shall contain the PD's requested power value defined in Table 79–6a.

~~For Type 3 and Type 4, the value should be (PD requested power value Mode A + PD requested power value Mode B). For Type 3 and Type 4, the PD requested power field defined in Table 79-3.2.5 is the sum of the PD requested power values defined in Table 79–6a.~~

Table 79–6a—Dual-signature PD requested power value ~~field for~~ Mode A and Mode B field

Bit	Function	Value/meaning
15:0	Dual-signature PD requested power value Mode A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	Dual-signature PD requested power value Mode B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

The value for the "Dual-signature PD requested power value Mode A" field shall indicate ~~should be (PD requested power value –~~the PD requested power value for Mode ~~B~~A~~)~~.

The value for the "Dual-signature PD requested power value Mode B" field ~~should~~ shall be the ~~(~~PD requested power value ~~– PD requested power value~~ for Mode ~~A)~~B.

"Dual-signature PD requested power value Mode A" and "Dual-siganture PD requested power value Mode B" are the maximum input average power levels (see 145.3.8.2) the PD wants to draw for the respective pairset. "Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" are the power values at the input to the PD's PI. Type 1, Type 2, and single-signature Type 3 and Type 4 PDs, all place 0 in the "Dual-signature PD requested power value Mode A" and "Dual-signature PD requested power value Mode B" fields.

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79.3.2.6b PSE allocated power value Alternative A and Alternative B

The "PSE allocated power value Alternative A and Alternative B" field ~~Alternative A and the PSE allocated power value field Alternative A~~ shall contain the PSE's allocated power value for Alternative A and Alternative B respectively, defined in Table 79–6b. ~~For Type 3 and Type 4, the PSE allocated power value field defined in Table 79.3.2.5 is the sum of the PSE allocated power values defined in Table 79–6b.~~

The value for the "PSE allocated power value Alternative A" field ~~should~~ shall ~~be (~~indicate the ~~PSE allocated power value – –~~PSE allocated power value for Alternative A~~B)~~. The value for the "PSE allocated power value Alternative B" field ~~should be (~~shall indicate the PSE allocated power value ~~PSE allocated power value~~for Alternative ~~A~~B~~)~~.

"PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" are the maximum input average power levels (see 145.3.8.2) the PSE expects the connected dual-signature PD to draw on the respective Alterna-

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Table 79–6b—PSE allocated power value ~~field for~~ Alternative A and Alternative B field

Bit	Function	Value/meaning
15:0	PSE allocated power value Alternative A	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.
15:0	PSE allocated power value Alternative B	Power expressed in units of 0.1 W. Valid values for these bits are decimal 1 through 499.

tives. "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" are the power levels at the input to the dual-signature PD's PI. The PSE uses this value to compute $P_{Class\text{-}2P}$ defined in 145.2.7. A PSE providing power to a Type 1, Type 2, and single-signature Type 3 and Type 4 PD, place 0 in the ~~11~~ "PSE allocated power value Alternative A" and "PSE allocated power value Alternative B" fields.

79.3.2.6c Power status

The power status field shall contain the PSE's bit-map of the PSE power pair and PSE or PD power class, defined in Table 79–6a, and is reported for the device generating the TLV.

79.3.2.6c.1 PSE power pairsx

The PSE power pairsx field shall contain an integer value for PSE power pairs defined by 145.2.4. A TLV generated by a PD shall set the field to 00.

79.3.2.6c.2 Dual-signature Power Classx Mode A

When the power type is PD this field shall be set to the requested Class of the dual-signature PD for Mode A during Physical Layer Classification as defined in 145.3.6. When the power type is PSE and the PSE is connected to a dual-signature PD, this field shall be set to the PSEs assigned Class for Alternative A as defined in 145.2.7. PSEs connected to a Type 1, Type 2, or single-signature PD ~~and single-signature PDs~~ set this field to value 0.

79.3.2.6c.3 Dual-signature Power Classx Mode B

When the power type is PD this field shall be set to the requested Class of the dual-signature PD for Mode B during Physical Layer Classification as defined in 145.3.6. When the power type is PSE and the PSE is connected to a dual-signature PD, this field shall be set to the PSEs assigned Class for Alternative B as defined in 145.2.7. PSEs connected to a Type 1, Type 2, or single-signature PD ~~and single-signature PDs~~ set this field to value 0.

79.3.2.6c.4 Power Classx

When the power type is PD this field shall be set to the requested Class of the PD during Physical Layer Classification as defined in 145.3.6. When the power type is PSE this field shall be set to the PSEs assigned Class as defined in 145.2.7. PSEs connected to a dual-signature PD and dual-signature PDs set this field to value 15.

79.3.2.6d System setup

The System setup field shall contain the device bit-map of the Power typex, PD 4PID, and PD Load defined in Table 79–6b and is reported for the device generating the TLV. The value of the System setup field transmitted by a PSE is undefined and shall be made 0.

79.3.2.6d.1 Power typex

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This field shall be set according to Table 79–6b.

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Table 79–6a—Power status field

Bit	Function	Value/meaning
15:13	Reserved	Transmit as zero. Ignore on receive.
12:11	PSE power pairsx	6 5 1 1 = Both Alternatives 1 0 = Alternative B 0 1 = Alternative A 0 0 = Reserved/Ignore
10	Reserved	Transmit as zero. Ignore on receive.
9:7	Dual-signature Power Classx Mode A	9 8 7 1 1 1 = Reserved/Ignore 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Single-signature PD
6:4	Dual-signature Power Classx Mode B	6 5 4 1 1 1 = Reserved/Ignore 1 1 0 = Reserved/Ignore 1 0 1 = Class 5 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Single-signature PD
3:0	Power Classx	3 2 1 0 1 1 1 1 = Dual-signature PD 1 1 1 0 = Reserved/Ignore 1 1 0 1 = Reserved/Ignore 1 1 0 0 = Reserved/Ignore 1 0 1 1 = Reserved/Ignore 1 0 1 0 = Reserved/Ignore 1 0 0 1 = Reserved/Ignore 1 0 0 0 = Class 8 0 1 1 1 = Class 7 0 1 1 0 = Class 6 0 1 0 1 = Class 5 0 1 0 0 = Class 4 0 0 1 1 = Class 3 0 0 1 0 = Class 2 0 0 0 1 = Class 1 0 0 0 0 = Class 0

79.3.2.6d.2 PD 4PID

This field shall be set according to Table 79–6b when the power type is PD. This field shall be set to 0 when the power type is PSE. This field shall be set to ‘1’ when the power type is Type 3 PD or Type 4 PD.

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