Power Matters

IEE802.3 4PPoE Task Force

Type 4 System Power Parameters Analysis March 2015

Rev 009

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Objectives

- To set the Type 4 PSE/PD system values over ISO/IEC 11801:1995 with 12.5Ω/100m resistance:
  - PSE minimum guaranteed power, Ptype
  - PSE minimum voltage, Vpse_min.
  - PSE maximum voltage, Vpse_max.
  - PD maximum available power (P2P_Iunb effect on PD available power will be addressed in darshan_02_0315.pdf).
  - PD minimum / maximum operating voltage
  - Icable per pair-set and total cable current

Work Premise

- **Meeting LPS requirements**
- **Total port current and**
- **Total port power for maximum power available at the PD.**
- Addressing Power Limit implementations
  - True power limit (Power limit is the end result required by EN60950)
  - ILIM (Monitoring the current, assuming Vpse is constant)
  - Variable ILIM (Monitoring the current=Pclass/Vpse=, assuming Vpse is variable, Set ILIM)
- This presentation will not address system P2P_Iunb/Runb (E2ECP2PRUNB). This will be covered bydarshan_02_01315.pdf.
  - As a result, specific values of current per pair-set will not be addressed.

Type 4 PSE Voltage Considerations

See annex E1-E5 for more details

- PSE systems contains the following main parts
  - PSE Power supply (or supplies),
  - PSE controller circuitry, Data interface
  - Routing (IR drop)

- Current PSE Power supplies are typically set to ~53V to 54V to benefit the ±3.5V margin (±6.5%) for:
  - Accuracy, Line/Load/Transient variations
  - PSE output resistance resistance (RDSON, Rsense, PCB traces, Transformers, Connectors, EMI filters)
  - Cross Regulation in multiport systems

- Increasing Vpse-min for Type 4,
  - **Helps in increasing Type 4 efficiency (lower current) and power delivered to PD**
  - **Has impact on PSE design**
    - A balance needs to be maintained
- Suggested Vpse-min = 52V (3 system vendors are Ok with it)
  - This will optimize the Type 4 parameters to keep mixed Type 2,3 and 4 systems, cost effective and the transition cost from Type 3 to Type 4, to be reasonable.

Type 4 PSE minimum power

- The objective is to have maximum power delivered from the PSE in order to get maximum power at the PD, resulting with more applications to be supported.
  - PSE output power max=100W per UL60950 LPS definitions. (see Annex D1 for more details)
  - The PSE power limiting circuitry accuracy limits the minimum guaranteed power from the PSE, Ptype_min.
- PSE system accuracy
  - Sense resistors = 1%
  - ADC accuracy = 3%
  - Headroom = 1%
  - TOTAL = +/-5%

  This accuracy is achievable by all vendors resulting with 90W PSE minimum guaranteed power.
- Few vendors developed system accuracy of less than +/-2.5% which allow PSE minimum guaranteed power of 95W.

As a result, PSE Minimum guaranteed Power = 90W (based on worst case available accuracy value above)

PSE Table 33-11 - Missing values marked in Red

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1	Output voltage per pair-set in the POWER_ON state	VPort_PSE_2P	V	44.0	57.0	1	See 33.2.7.1
				50.0	57.0	2,3	
				52.0	57.0	4	
4	Continuous output current capability in POWER_ON state per pair-set	Icon-2P	A	0.5*Pclass/Vport_PSE_2P		3	Without E2EP2PRunb effect
				0.5*Pclass/Vport_PSE_2P		4	
4.1	Pair current due to E2EP2PRunb within E2EP2PRunb range	Icon-2P_unb	A		0.668[a] (TBD)	3	See 33.2.7.4. See note 1.
					0.931[a] (TBD)	4	
12	PSE Type power minimum	Ptype	W	2×ICable × (VPort_PSE- 2P min)		1,2	See 33.1.4
						3[1]	
						3	
12.1	PSE Type power			90	100	4	

Note 1: The total port current of both pairs of the same polarity shall not exceed ***Ptype/Vport_PSE_2P=0.5*(Ptype/***VPort_PSE_2P***)*(1+α)+0.5*(Ptype/***VPort_PSE_2P***)*(1-α)***

Note a: Not part of the table. See darashan_02_0315.pdf for maximum pair current due to E2EP2PRunb.

PD Type 4 Specifications

- Type 4 PSE minimum guaranteed power = 90W
- PSE power may reach 100W and is still LPS compliant.
- The 100W-90W=10W difference is the PSE margin to meet LPS.
- PSE power peak may vary due to PD Peak (load ripple current with duty=5% average over 1sec etc.) and it is limited at PSE side by Pmax=100W (LPS)
- → so define PD minimum voltages based on the above.
- **VPort_PD-2P=40V**
  - VPort_PD-2P=Vpse_min-6.25*(Pmax/Vpse_min)=52V – 6.25Ω*100W/52V =40V
  - Allows for flexible system implementations in field

- **Voverload-2P=39.5V**
  - For overload per Table 33-18: Ppeak_PD=1.11*Pclass_PD
  - Per Equation 33-4, Ipeak can be found from Ppeak_PD
  - Voverload-2P=Vpse_min-6.25*Ipeak=39.5V
  - Allow using Eq 33-4 and Ppeak/Pclass ratio unchanged with Type 3 and 4.

- For more information on this please see Annex F, G and K.

PD Table 33-18 - Missing values marked in Red.

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional Information
1	Input voltage per pair-set	VPort_PD-2P	V	37.0	57.0	1	See 33.3.7.1, Table 33-1
				42.5	57.0	2,3	
				40	57.0	4	
3	Input voltage range per pair-set during overload	Voverload-2P	V	39.5	57.0	4	See 33.3.7.4.
4	Input average power, Class 7	Pclass_PD	W		71.3[a]	4	See 33.3.7.2.

Editor note a:
Pclass_PD for class 7 was calculated for Ptype=90W and 0.5*Rch_max=6.25Ω according to:

$$\left[Ptype - Rch \cdot \left(\frac{Ptype}{Vport\_pse - 2P\_\min} \right)^2 \right]$$

P2P_Iunb effect on Pclass_PD for Type 3 and 4 is addressed in darshan_02_0315.pdf.

Defining Icable

- Icable of Type 4 need to be addressed differently from the other types 1-3.
  - Icable is maximum current related to 100W (max possible power) and not to Ptype_min.
    - Required to allow margins from Ptype to 100W in terms of current/power so system will be compliant when power is near 100W but not crossing it.

- Proposal:Icable_min=0.5*100W/Vpse_min=1.923A/2=0.962A.
  - Ptype=90W is the guaranteed power at PSE PI.
  - Icont-2P_max=0.5*Ptype/Vpse_min=0.5*90W/52V=1.73A/2= 0.865A.

- **Additional information to be added for Icable definitions:**

Icable is defined for system with P2P_Iunb=0.
For P2P_Iunb>0 conditions as defined in clause TBD, Icable which is defined per pair-set, can be higher up to Icable*(1+ α) as long as the total current sum of the two pairs of the same polarity is ≤ 2*Icable.

Checking other system issues

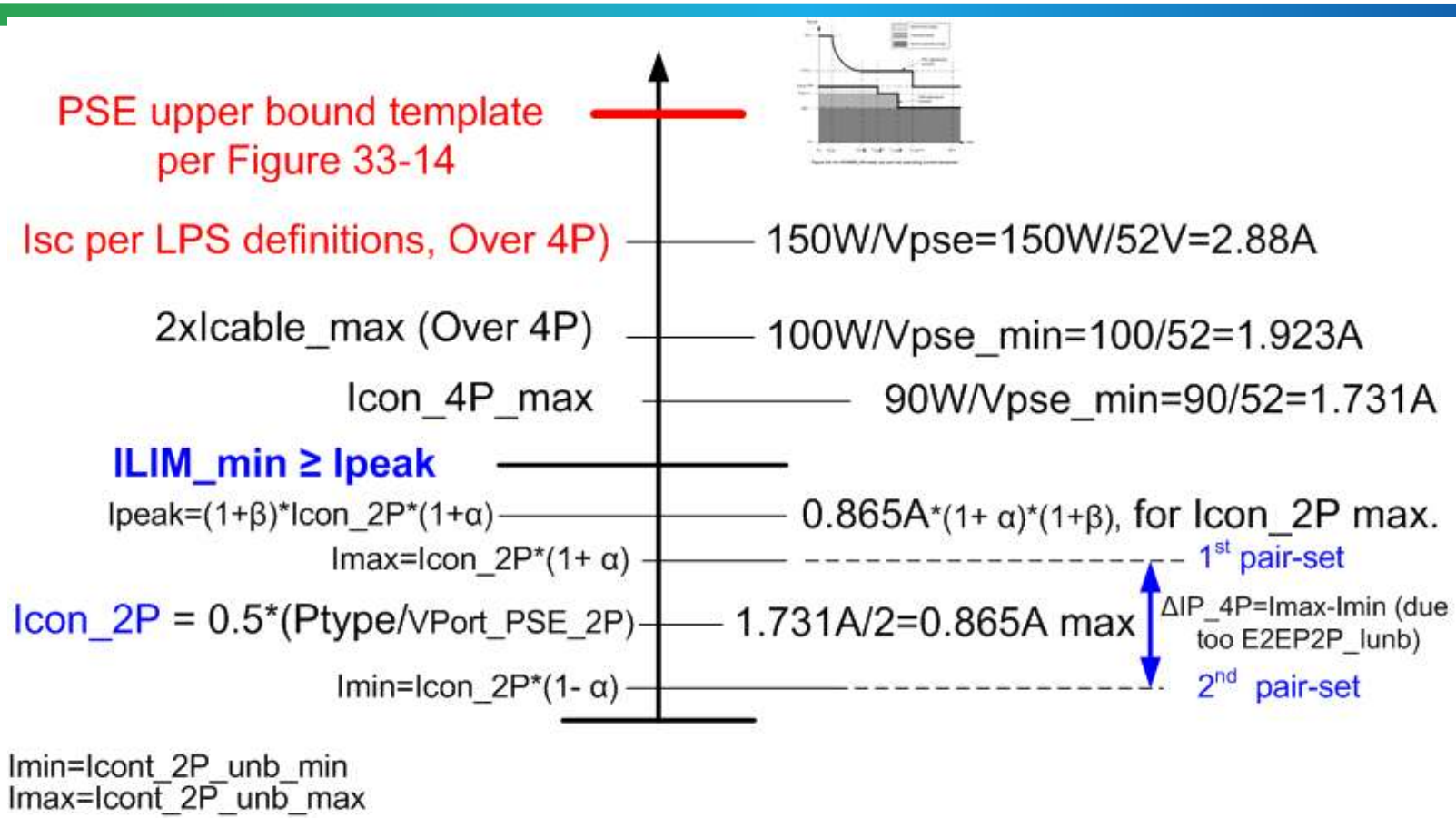
- Total PD load current is not affected by system P2P_Iunb (E2ECP2PRUNB). See Annex C for details.

- Maximum Current per LPS definitions.
  - UL allows Normal and short circuit current to be significantly higher than normal PoE current for any PSE voltage operating range and up to 100W. See details in Annex D1.

- System stability
  - No stability issues with Vpse from 50V to 57V at Output power up to 100W. See Annex F2 and F3 for details.

- Addressing Power Limit implementations. See Annex K for details

How ILIM_MIN is affected by Type 4 parameters Example with Ptype=90W.



- ILIM_MIN= Icon_2P + 0.5*ΔIP_4P + Design Margin = Icon_2P*(1+α)*(1+β)
  - α =System P2P_Iunb effect. Example: α=TBD %, See darshan_02_0315.pdf for details.
  - β=Current ripple contribution (affects Ipeak, PD Ppeak) and Design Margin. Design margin is implementation decision.

Summary – Type 4 parameters

	#	Parameter	Min	Max	Notes
PS E	1	Ptype[W]	90	100	
	2	Vpse[V]	52	57	
	3	Icont_2P [A]	(0.5*90W/52V)*(1+α)		
	4	Equation 33-4	Can be used for Type 3 and 4.		Note 3
PD	5	Pclass_PD[W]	71.3	Note 1	
	6	VPort_PD-2P [V]	40		Note 2
	7	Voverload-2P	39.5		
	8	Ppeak_PD	=1.11*Pclass_PD. Can be used for Type 3 and 4.		
Cable	9	Icable[A]	0.962A		
	10	Numbers of CAT5e cables per bundle for Type 4 is 22 (TBD). See reference 4.			
	11	Maximum loop resistance per pair-set: 12.5Ω/100m per pair set.			

Notes:
1. Can be as high as ~89.xxW for Short cable e.g. 1m with extended power feature.
2. This is the PSE pair-set minimum current capability.
3. Equation 33-4 set Ipeak-2P as function Ppeak_PD-2P, Vpse and Rch.

Thank You

Annex A: Current capacity per conductor

gauge	Conductor Diameter Inches	Conductor Diameter mm	Ohms per 1000 ft.	Ohms per km	Maximum amps for chassis wiring	Maximum amps for power transmission
18	0.0403	1.02362	6.385	20.9428	16	2.3
19	0.0359	0.91186	8.051	26.40728	14	1.8
20	0.032	0.8128	10.15	33.292	11	1.5
21	0.0285	0.7239	12.8	41.984	9	1.2
22	0.0254	0.64516	16.14	52.9392	7	0.92
23	0.0226	0.57404	20.36	66.7808	4.7	0.729
24	0.0201	0.51054	25.67	84.1976	3.5	0.577
25	0.0179	0.45466	32.37	106.1736	2.7	0.457
26	0.0159	0.40386	40.81	133.8568	2.2	0.361

Table was taken from: http://www.powerstream.com/Wire_Size.htm.
See also reference 3.

Notes:
-The current capacity per wire in the above table is based on the traditional 700 circular mils per Ampere as we used to design power transformers however this is very conservative approach.
-See http://www.engineeringtoolbox.com/wire-gauges-d_419.html for >2A/wire for AWG#24.
-Numbers are at free air and not in a bundle.

Annex B: Calculation Procedure

Steps	Optimization/Derivation methods	Notes
1	Ppse_min=X. e.g. 95W or 90W. Vpse_min=Y. e.g. 50V, 52V or 53V.	Main Inputs
Example is given with Ppse=95W and Vpse=50V		
2	Ip=Ppse_min/Vpse_min=95W/50V=1.9A	Total 4P current
3	Vpd_min=Vpse_min-R*Ip=50V-6.25*1.9=38.28V	>37V ➔ OK.
4	Ppd_max=Vpd_min*Ip=38.28*1.9=72.43W	74.1W with Vpse=52V
5	PD can get up to 95W if actual channel resistance is known e.g. for R=0.1Ω, Ppd=94.6W	94.7W with Vpse=52V

Annex C: Total PD load current is not affected by system P2P_Iunb (E2ECP2PRUNB)

$$Ip_{4P} = I_{2P}Max + I_{2P}M\min = \left(\frac{Ip_{4P}}{2} + \frac{\Delta I}{2}\right) + \left(\frac{Ip_{4P}}{2} - \frac{\Delta I}{2}\right) = Ip_{4P}$$

$$\Delta I = E2ECP2PRUNB_{effective} \cdot Ip_{4P}$$

$$effective = including\ \ PSE\ \ and\ \ PD\ Vdiff\ \ effect$$

$$\mathrm{Im}ax = 0.5 \cdot Ip_{4P} \cdot \left(1 + E2ECP2PRUNB_{effective}\right)$$

-We can see ΔI is not affecting total PD load current, IP_{4P}.
-ΔI is the Pair to Pair current difference of pairs of the same polarity
-E2ECP2P**R**UNB=End to End Channel Pair to Pair Resistance Unbalance.
-E2ECP2PRUNB=E2ECP2P**C**UNB i.e. Runb=Iunb by definition.
-PSE Vdif and PD Vdiff is integrated in E2ECP2PRUNB.
-Imax=The pair with maximum current due to system P2P_Iunb
-P2P_Iunb term is used often instead E2ECP2P**R**UNB and both are equivalent

Annex D: LPS requirements per EN60950

Output voltage [a] (U_{oc})		Output current [b d] (I_{sc})	Apparent power [c d] (S)
V a.c.	V d.c.	A	VA
≤ 30	≤ 30	≤ 8,0	≤ 100
–	30 < U_{oc} ≤60	≤ 150/U_{oc}	≤ 100

[a] U_{oc}: Output voltage measured in accordance with 1.4.5 with all load circuits disconnected. Voltages are for substantially sinusoidal a.c. and ripple free d.c. For non-sinusoidal a.c. and d.c. with ripple greater than 10 % of the peak, the peak voltage shall not exceed 42,4 V.

[b] I_{sc}: Maximum output current with any non-capacitive load, including a short-circuit.

[c] S (VA): Maximum output VA with any non-capacitive load.

[d] Measurement of I_{sc} and S are made 5 s after application of the load if protection is by an electronic circuit or a positive temperature coefficient device, and 60 s in other cases.

- Isc=150W/Uoc=150/Vpse ➔
- S≤100VA=100W for DC.
- S=Apparent power: The magnitude of the vector sum of active (P) and reactive (Q) power . In PoE systems (DC power suplies) Q=0.
- Icont_2P=0.5*Icont_4P excluding the P2P_Iunb effect.

Vport_pse-2P	Isc=Iport_max=ILIM_MAX= 150/Vport_pse-2P measured 60sec after application of the load.	Icont_4P= 100W/Vport_pse-2P
50	3	2
51	2.941	1.961
52	2.885	1.923
53	2.830	1.887
54	2.778	1.852
55	2.727	1.818
56	2.679	1.786
57	2.632	1.754

Annex D1: LPS considerations per EN60950 Table 2B

- See Annex D for more details about LPS per EN60950 and calculations

#	Operating Condition			
	A: Iport_4P at Normal operation max.		B: Isc at Short Circuit	Status
Vpse_min	100W/52	<	**150**W/52V	A<B. ➔ OK
Vpse_max	100W/57V	<	**150**W/57V	A<B. ➔ OK

- Isc: Port current at short circuit condition
- Iport_4P: Total port current (all pairs) at normal operation at 100W max.
- As a result:
- The allowed Isc > 100W/Vpse=Maximum allowed normal operating current.
  - We meet LPS requirements
  - We already met SELV requirements
- LPS is more about power limiting and less about current limiting.
- **Using current limiting only, will limit maximum power utilization!!!**

Annex E1: PSE Voltage considerations

- **Background**
- PSE systems contains 3 main parts:
  - PSE Power supply (or supplies)
  - PSE controller
  - Data interface (connectors, transformer)

- In existing multiport systems architecture of high power PoE :
  - Most of the ports are 802.3af/at (Type 1 or 2)
  - Some of the ports Type 3 equivalent
  - Some of the ports Type 4 equivalents
    - It is the typical cost effective/size architectures being used in the market today.

- PSE Power supply is typically set to ~53V to 54V* to benefit the ±3.5V margin (±6.5%) for:
  - Accuracy,
  - Line/Load/Transient variations
  - PSE controller series resistance **(RDSON, Rsense, PCB traces, Transformers, Connectors, EMI filters)**
  - Cross Regulation in multiport systems
- It helps to use low cost power supplies.
  - Many systems are set to 54-55V for better load regulation margins.

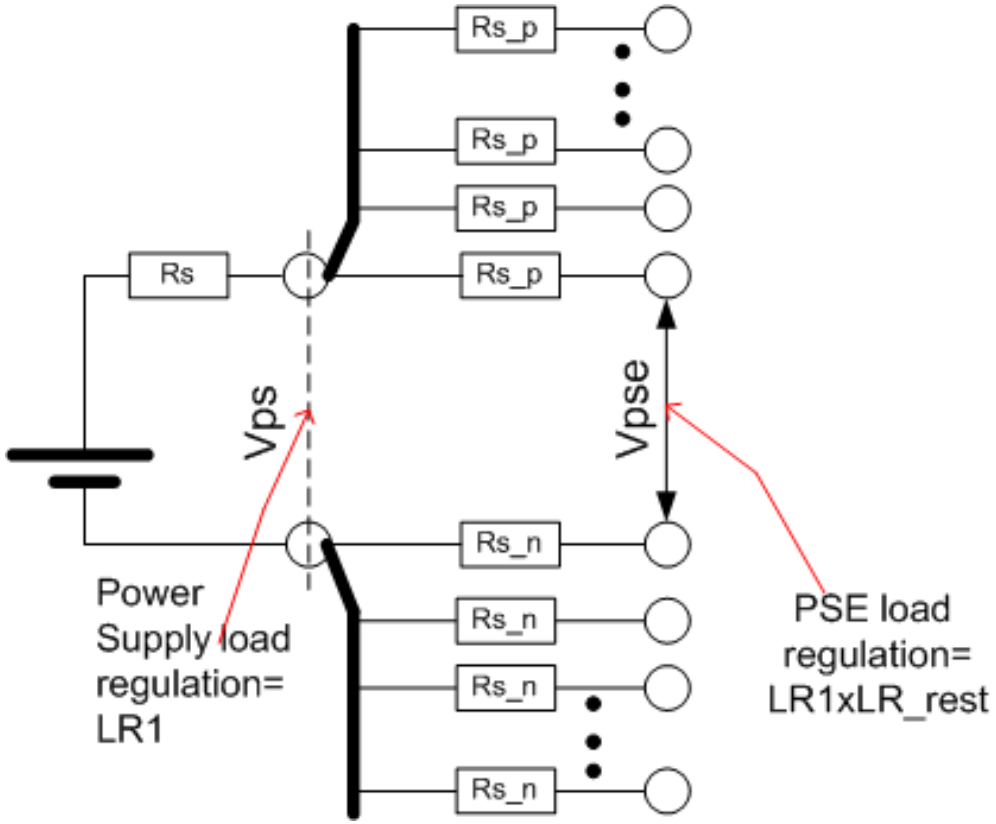
Annex E2: PSE Voltage considerations

- **Background cont.**

- Replacing existing power supplies + PSE controller circuitry that works from 50V to 57V to 52V to 57V **is possible <u>but need carefully be verified by system vendors</u>** due to possible effect on existing and future system performance and cost in terms of output voltage accuracy settings, load regulation, Response to load transients, and transition from normal to backup supply operation .
  - It is desired to use the same power supply operating range for all PSE types (1,2,3,4). (large quantities, same input voltage properties, easier system design for any PoE Type port)
    - Types 1,2 and 3 in multiport systems (largest quantities) will have to be designed for the worst case possible tighter proposal of 52V to 57V for Type 4.
- Inputs from 3 system vendors: 52V is OK, we are using 54-55V typical value in order to handle the above concerns.
- On the other hand, Increasing Vpse_min from 50V to 50V+X has some benefits in terms of lower port current for the same PD maximum input power or alternatively, increasing PD available power.
- The purpose of this work is to optimize the Type 4 parameters set to keep mixed Type 2,3 and 4 system cost effective and the transition cost from Type 3 to Type 4, to be reasonable.

Annex E3: Actual Vpse load regulation and operating range

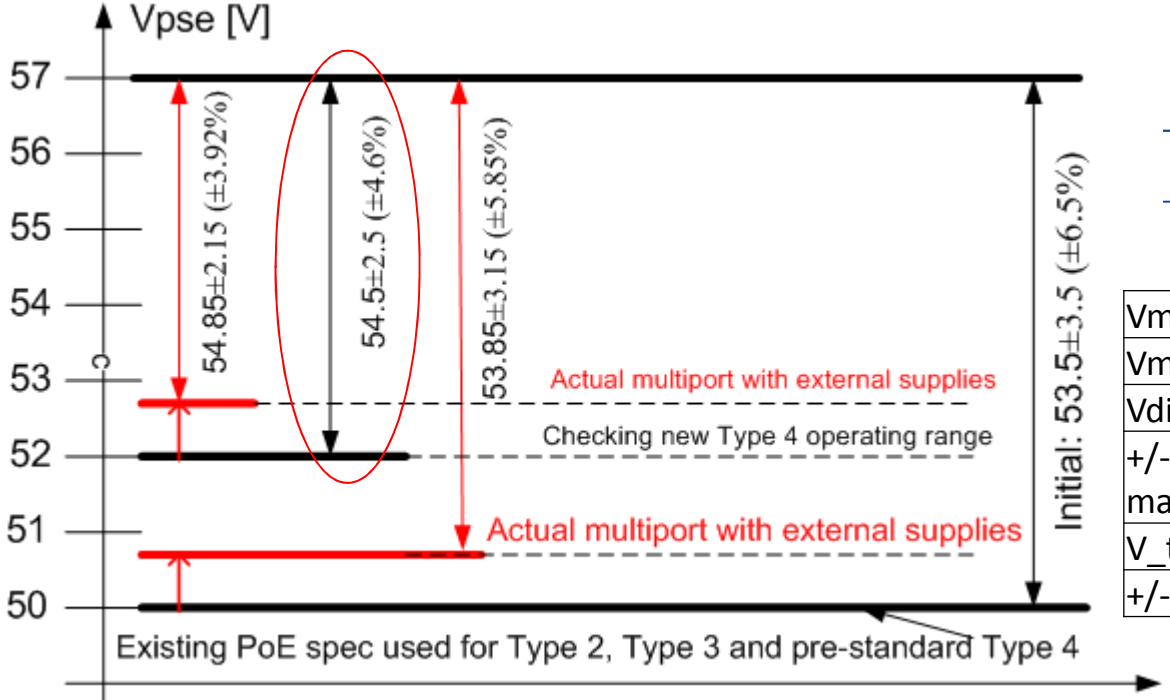
- System wise, PSE output voltage operating range and line, load and transient regulations is function of its power supply and PSE controller external circuitry.
- Some system vendors use simple calibration and compensation techniques to account for total PSE output current/voltage/power for improved accuracy and load regulation.



The actual Load Regulation and PSE output voltage operating range is worsen than the PSE Power supply alone due to:
-Power supply EMI filters
-PSE Chip Rs, Rdson.
-PCB traces
-Connectors
-Transformers
-Current sharing circuitry
-Backup/power Oring diodes

Annex E4: PSE Voltage considerations

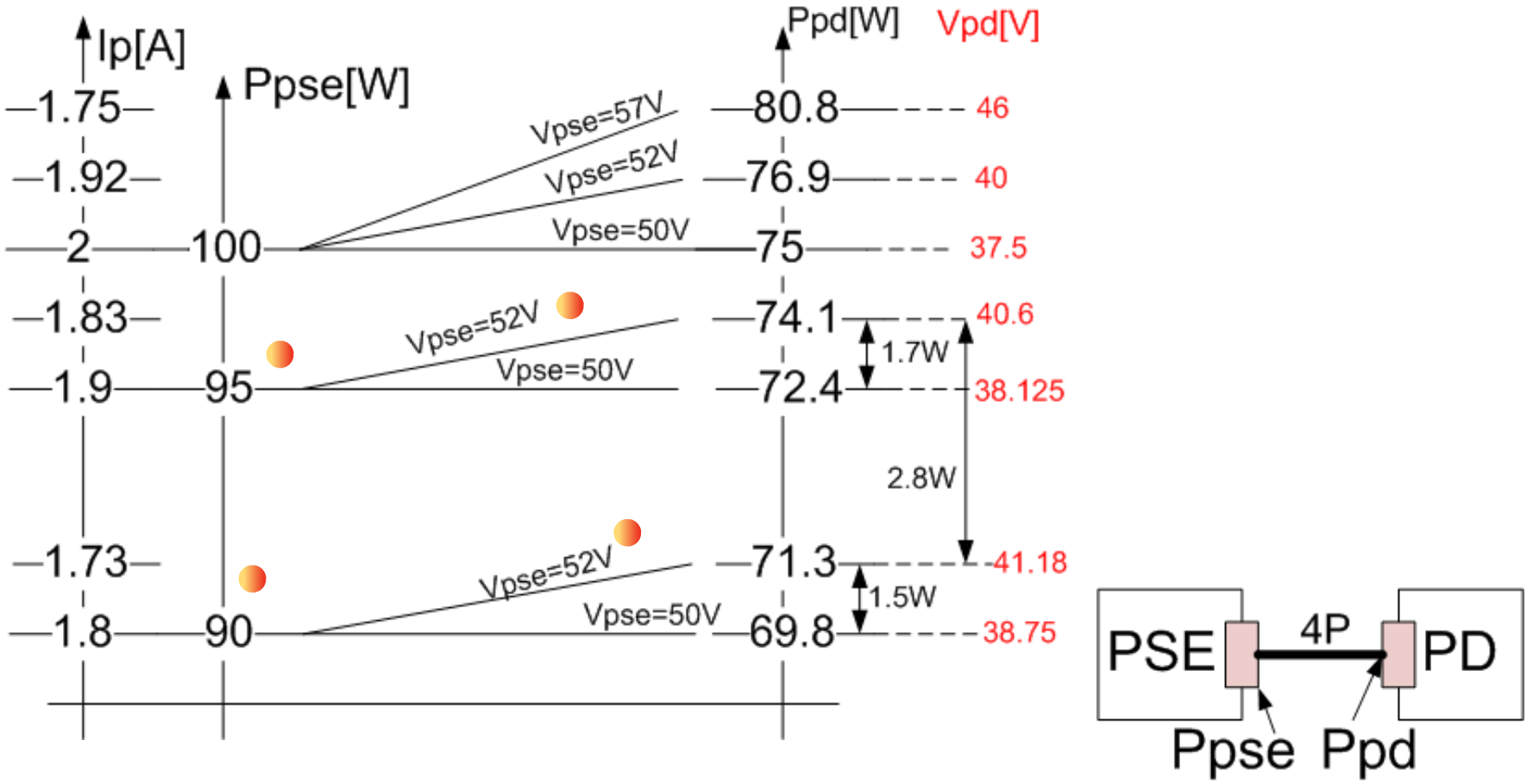
- Some multiport PoE systems (e.g. 24 ports with ~400W or higher power supply pending on their power management function capabilities) are using external power supply for backup (which may use series diodes) and/or add-in power (current sharing with droop method) functions which may require some additional PSE voltage margin <0.7V resulting with effective worst case operating rage of 50.7V to 57V which cause margin to drop from ± 6.5% to ±5.85 % that covers PSE power supply and PSE controller circuitry and other external components.
- If Vpse_min will be change to 52V, margins will drop further to ± 4.6% without external supplies case. However with adequate design, total system accuracy of ± 4.6% can be achieved, requiring < ± 4.6% supplies accuracy/line/load regulation.



Worst case WHAT-IF chart.

Vmax[V]	57	57	57	57	57
Vmin[V]	50	50.7	52	52.7	53
Vdiff[V]	7	6.3	5	4.3	4
+/- margin[V]	3.5	3.15	2.5	2.15	2
V_type[V]	53.5	53.85	54.5	54.85	55
+/- margin	6.54%	5.85%	4.59%	3.92%	3.64%

Annex E5: PD minimum available power vs. PSE min. Power

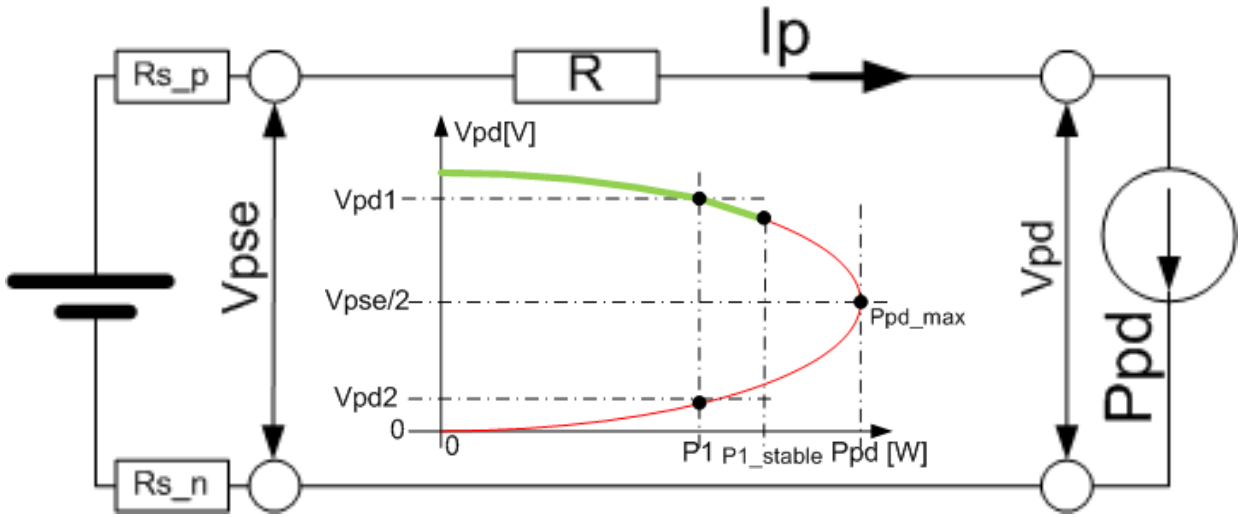


- In all use cases: Vpd>37.5V which fits to current PD chip UVLO
- 4 Pairs , 6.25Ω/100m
- Ip=Total PD load current. Ppd=Total PD input power. Ppse=Total PSE output power

Annex F1: Vpd_min considerations

- Vpd_min should be ≥37V. It should not be <37V
  - Using the same UVLO values for all types.
    - Simplest PD design (Same as we did for 802.3af and 802.3at)
      - 37V was minimum for Type 1. Type 2 was 42.5V>37V ➔ OK.
  - Using same PD input interface for all types (high quantities ➔ lower cost).
    - Allow using same PD chip for all types especially Type 2,3 and 4.
- Vpd_min should be only a result of system physical numbers Ptype, Vpse_min that maximize PD available power.
  - Vpd=Vpse_min-6.25*Ptype/Vpse_min=52V – 6.25Ω*90W/52V = 41.18V
  - Vpd=Vpse_min-6.25*PMAX/Vpse_min=52V – 6.25Ω*100W/52V =40V
- Due to the fact that PSE Ptype can vary from 90W to 100W max and PD minimum input average available power is 71.4W with AC power content that can go up to 76.88W **(limited by 100W average maximum at the PSE)**, PD need to be designed to work down to 40V.
- Conclusions:
- Type 4 Vpd=40V
- Type 2 and 3 Vpd_min=42.5V.
- Ppeak Type 4=76.88W ➔ 76.8W. Ipeak is calculated by Equation 33-4

Annex F2: Affecting parameters on PD maximum power



$$Vpd = \frac{Vpse + \sqrt{Vpse^2 - 4 \cdot R \cdot Ppd}}{2}$$

$$Ip = \frac{Vpse - Vpd}{R} =$$

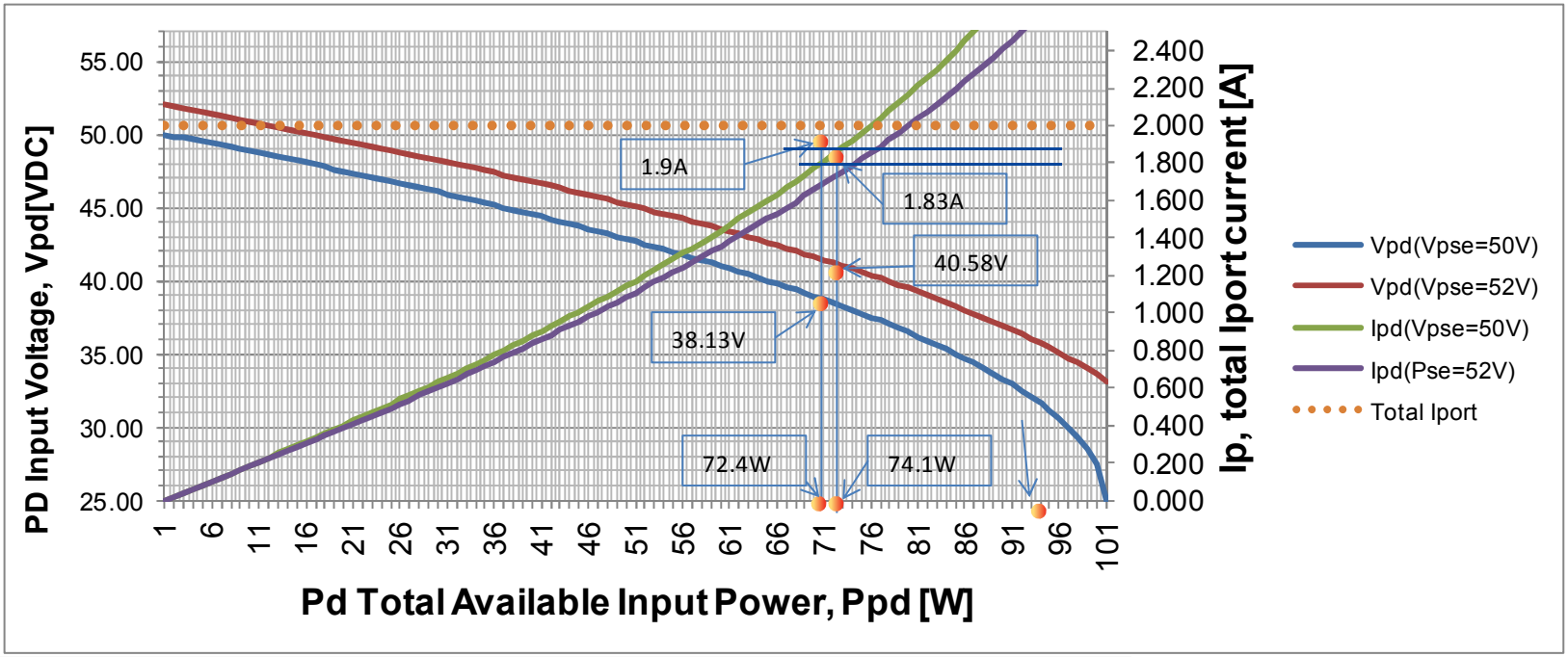
$$= \frac{Vpse - \sqrt{Vpse^2 - 4 \cdot R \cdot Ppd}}{2 \cdot R}$$

$$Ppd\_\max = \frac{Vpse^2}{4 \cdot R}$$

$$Ppd\_\max\_stable = \approx 0.75 \cdot \left(\frac{Vpse^2}{4 \cdot R} \right)$$

- Main control parameters
  - R, total 4P loop resistance at 100m, 6.25Ω max.
  - Vpse, PSE output voltage at the PI.
  - Vpd, PD input voltage at the PI.
  - Ppd, PD input power for a constant power sink load. Ip=Ppd/Vpd. Ppd=consant.
  - Ppd_max, Maximum theoretical PD available power
  - Ppd_max_stable, Maximum available PD input power at stable operating region (70 to 80% of Ppd_max).
  - Ip, Port total current of both ALT A and ALT B of pairs of the same polarity.

Annex F3:Stability and maximum current per wire.
Vpd and Ipd as a result of Ppd and Vpse



Ppse[W]	Vpse[V]	Ip[A]	Iport_2P[A]	Rch_4P[Ohm]	Vpd[V]	Ppd_max[W]
90	50	1.800	0.900	6.25	38.75	69.8
90	52	1.731	0.865	6.25	41.18	71.3
90	53	1.698	0.849	6.25	42.39	72.0
95	50	1.900	0.950	6.25	38.13	72.4
95	52	1.827	0.913	6.25	40.58	74.1
95	53	1.792	0.896	6.25	41.80	74.9
100	50	2.000	1.000	6.25	37.50	75.0
100	52	1.923	0.962	6.25	39.98	76.9
100	57	1.754	0.877	6.25	46.04	80.8

-Using system parameters that limits total **continuous** port current to 2A max.+margin. (Maximum 1A/pair, 0.5A/wire (brown doted line) as starting point. CAT5e with AWG#24 can stand ≥0.577mA/wire. **See Annex A** for details.
-See **Annex B** for calculation procedure

Annex G1: Input voltage range per pair-set during overload

- Overload occurs when PD load requires higher current/power than the average behavior.
- Due to the fact that PSE is limited to 100W anyway, we can calculate Vpd if PSE gets to 100W max due to PD utilized maximum DC power:
- Ppd_max=100W-6.25Ω*(100W/52V)^2=76.88W.
- As a result Vpd_min=52V-6.25Ω*100W/52V=39.98V ➔ 40V.
- So far the above is for worst case DC/Average behavior.
- How the above is sync with Overload conditions, AC current ripple, Eq 33-4 and Ppeak_PD?
  - **See Annex G2**.

Annex G2: Input voltage range per pair-set during overload

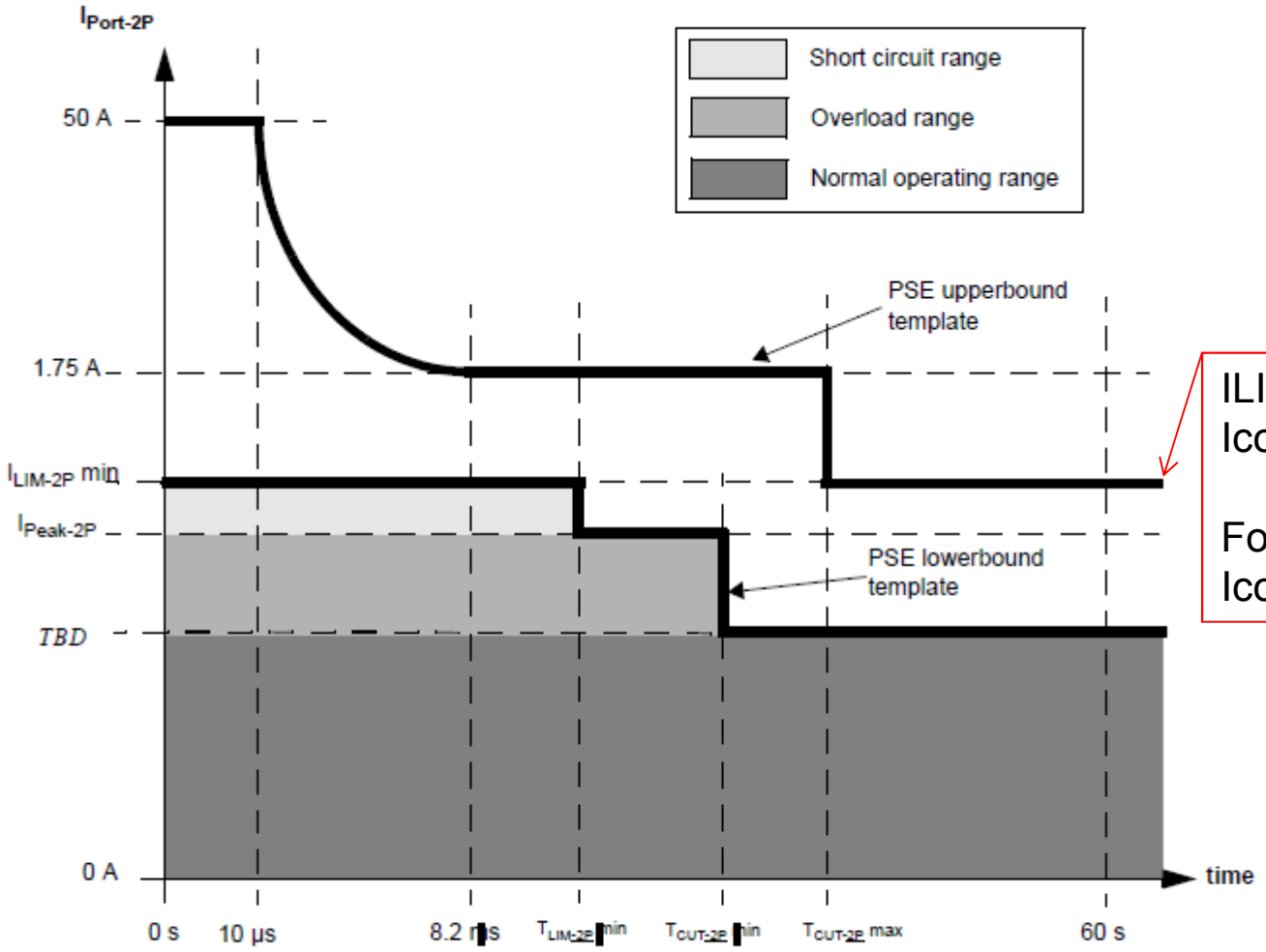
- Ppd_peak is defined by the current spec. as Ppd_peak=1.11*Pclass-PD=79.12W. This value is higher than 76.88W calculated for worst case DC value. This is not a problem due to the fact that the specification requires that overload conditions are average over 1sec with Tcut and 5% duty cycle that ends up back to 90W at PSE and 71.3W at PD. Ipeak per equation 33-4 can be used for Type 4 as well:

$$I_{\underline{\text{Peak-2P}}} = \left\{ \frac{V_{\underline{\text{PSE-2P}}} - \sqrt{V^2_{\underline{\text{PSE-2P}}} - 4(R_{\text{Chan}})(P_{\underline{\text{Peak\_PD-2P}}})}}{2(R_{\text{Chan}})} \right\}_{\text{A}}$$

- Ppeak_PD_2P=Ppeak_PD/2=79.18W/2=39.56W
- Ipeak_2P=1.002A.
- Voverload-2P=52V-12.5*1.002=39.5V
- Actual Ipeak_2P will be higher by (1+α). due to P2P_Iunb however it will not change Vpd_ovld due to the fact that the 2nd pair-set will be with lower current by a factor of (1-α).

$$I_{\underline{\text{Peak-2P}}} = \left\{ \frac{V_{\underline{\text{PSE-2P}}} - \sqrt{V^2_{\underline{\text{PSE-2P}}} - 4(R_{\text{Chan}})(P_{\underline{\text{Peak\_PD-2P}}})}}{2(R_{\text{Chan}})} \right\}_{\text{A}} \text{x(1+alfa)}$$

Annex K1: How ILIM_MIN is affected by Type 4 parameters



ILIM_2P_MIN≥Ipeak-2P= Icont_2P*(1+α)*(1+β)+margin.

For Type 2, (1+β)=1.14 i.e. Icont_2P=1.14*Icable.

Figure 33–14—POWER_ON state, per pair-set operating current templates

Annex K2: How Ilim_min is affected by Type 4 parameters (2)

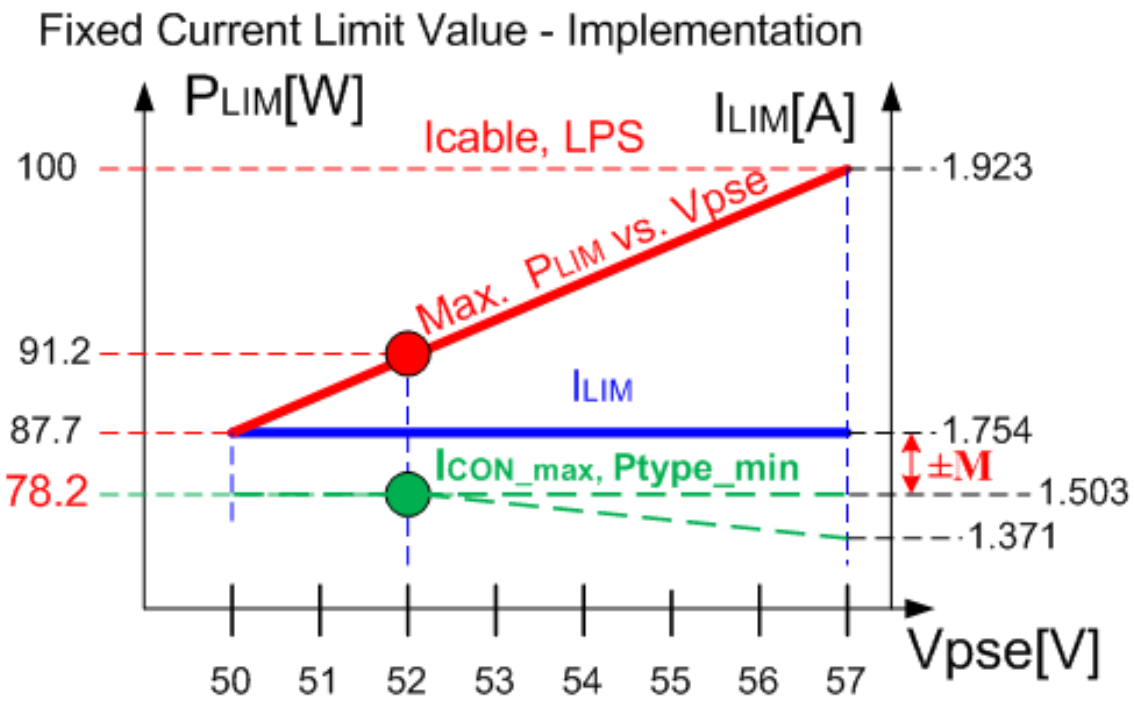
- Using ILIM and Power limit allows the following ILIM_MIN without violation 100W limit.

Examples:

- ILIM_MIN=Icont_2P*(1+α)*(1+β)=(90W/52V/2)*(1+0.05)*(1+0.05)=0.954A
- ILIM_MIN=Icont_2P*(1+α)*(1+β)=(100W/52V/2)*(1+0.05)*(1+0.05)=1.06A

- Moreover:
  - ILIM_Min is specified per pair-set.
  - Figure 33-12 concept can be used for Type 4 as well. See Annex K1 to K7 for details.

Annex K3: Less Ptype~=78W if we use only **fixed** ILIM value to limit PSE to 100W.



- Maximum available PSE power =78.2W (64W in PD) with:
- ± 5% circuit accuracy.
- p2p_Iunb=0.05 (Example. Higher P2P_Iunb will result with lower Ptype due to the need to use lower ILIM threshold value)
- Conclusion:
  - We can't use only current limit to achieve guaranteed 90W at PSE for the above parameters.

- ILIM_min = 100W/Vpse_max
- PLIM = ILIM_min*Vpse
- Current Limit doesn't depend on real system Vpse
- Without design margins and P2P_Iunb

● Maximum theoretical PSE available power

● Actual PSE available power=Ptype_min with +/-5% margin and P2P_Iunb effect=0.05.

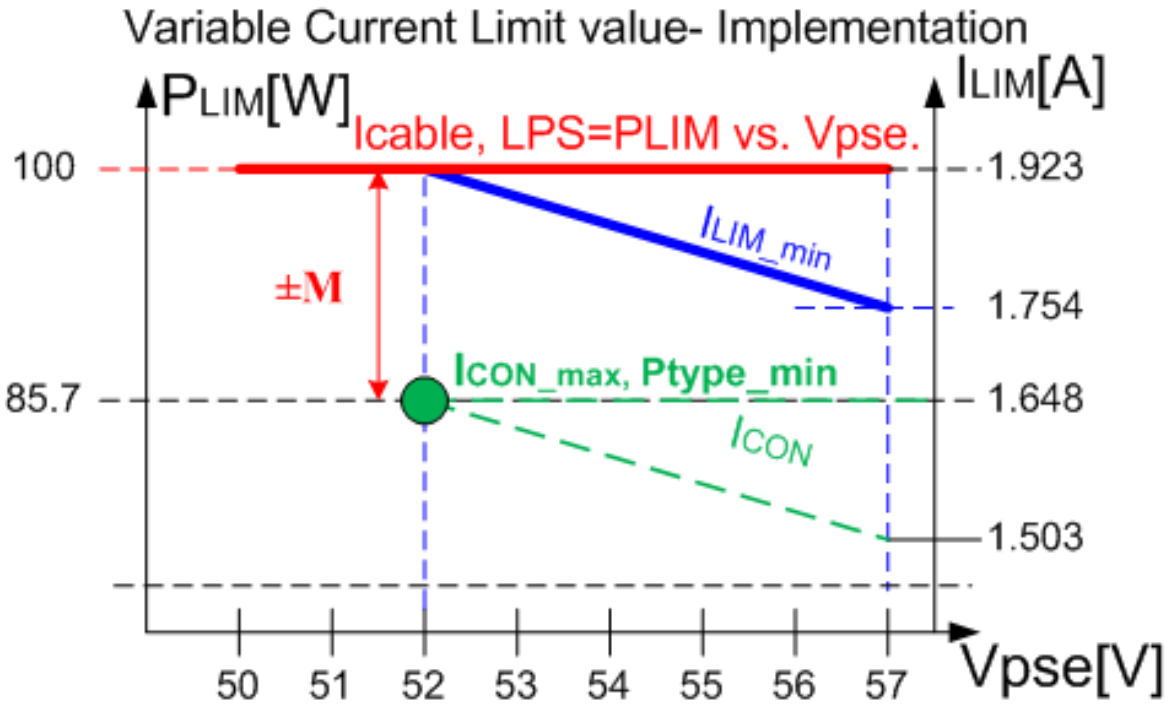
Annex K4: What will happen if we use only ILIM to limit PSE to 100W per LPS requirements.

To maximize PSE output power and as a result, PD available power, we need to use power limit and not only current limit.

With fixed current limit of ILIM_MAX=90W/57V=1.58A we will get maximum 64W (for +/-5% accuracy and 5% max P2P_Iunb) at PD which is just ~13W above Type 3 PD power which was not our intention when we start 802.3bt.. Using power limit will solve the problem.

PSE upper bound after 5sec to 60sec at ILIM_MIN PER FIGURE 33-14 for 100W max at Vpse=57V. [A]	ILIM_MIN	100W/57V/2	0.877
ILIM_MIN FOR 100W max at Vpse=57V Including P2P_Iunb effect of e.g. 5% max. [A]	ILIM_MIN *(1+P2P_Iunb)	Will result with 105W > 100W!	0.921
Reducing P2P_Iunb effect e.g. 5% from ILIM_MIN. [A]	ILIM_MIN /(1+p2p_Iunb)	(100W/57V)/(1+0.05)	0.835
ILIM_MIN WITH +/-5% margin [A]	0.9*ILIM_MIN/(1+p2p_Iunb)		0.752
Maximum PSE output power [W],	Ptype=0.9*Vpse_min*2*ILIM_MIN/(1+p2p_Iunb)		78.2
Maximum PD available power [W]	Ppd	Ptype-6.25*ILIM_max^2	**64**

Annex K5: Less than Ptype~=86W if we use only variable ILIM value to limit PSE to 100W.



- Maximum available PSE power =85.7W (68.7W in PD) with:
- ± 5% circuit accuracy.
- p2p_Iunb=0.05 (Example. Higher P2P_Iunb will result with lower Ptype due to the need to use lower ILIM threshold value)
- Conclusion:
  - We can't use only current limit to achieve guaranteed 90W at PSE for the above parameters.

- ILIM_min = 100W/Vpse, without margin, **M**.
- PLIM = 100W, without margin, **M**.
- Current Limit value is function of Vpse
- Maximum theoretical PSE available power is 100W without margins, M.
- Actual PSE available power=Ptype_min with +/-5% margin and P2P_Iunb effect=0.05, **M**.

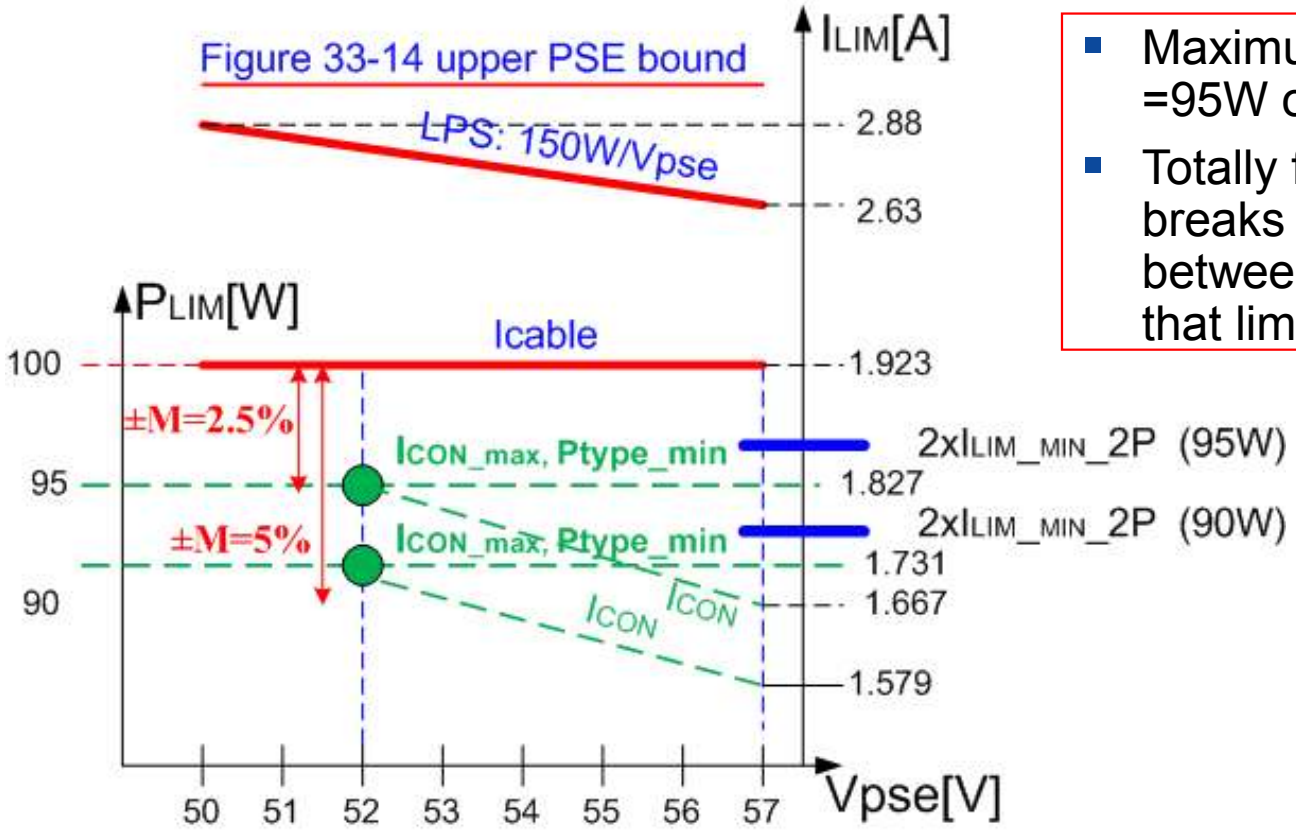
Annex K6: Less than Ptype~=86W if we use only variable ILIM value to limit PSE to 100W.

To maximize PSE output power and as a result, PD available power, we need to use power limit and not only current limit.

With variable current limit of ILIM=90W/Vpse we will get maximum 68.7W (for +/-5% accuracy and 5% max P2P_Iunb) at PD which is 18W only above Type 3 PD power which was less than our intention. PSE guranteed power will be <86W.

PSE upper bound after 5sec to 60sec at ILIM_MIN PER FIGURE 33-14 for 100W max at Vpse=52V. [A]	ILIM_MIN	100W/52V/2	0.962
ILIM_MIN FOR 100W max at Vpse=57V Including P2P_Iunb effect of e.g. 5% max. [A]	ILIM_MIN*(1+P2P_Iunb)	Will result with 105W > 100W!	1.01
Reducing P2P_Iunb effect e.g. 5% from ILIM_MIN. [A]	ILIM_MIN/(1+P2P_Iunb)	0.5*(100W/52V)/(1+0.05)	0.916
ILIM_MIN WITH +/-5% margin [A]	0.9*ILIM_MIN/(1+p2p_Iunb)		0.824
Maximum PSE output power [W],	Ptype=0.9*Vpse_min*2*ILIM_MIN/(1+P2P_Iunb)		85.71
Maximum PD available power [W]	Ppd	Ptype-6.25*(2*ILIM_max)^2	**68.73**

Annex K7: Greater than 90-95W if we use fixed ILIM and fixed PLIM to limit PSE to 100W per LPS and meet all our objectives.



- Maximum available PSE power =95W or 90W.
- Totally flexible solution that breaks any dependence between ILIM_2P and Ptype that limits Ptype_min.

- ILIM_min = 0.5*(1+α)*(Ptype_min/Vpse)+design margin.
- PLIM_max = 100W max. PLIM_min=Ptype_min.
- P2P_Iunb is not affecting Ptype_min.
- Ptype_min is function of possible accuracy, M only.

Annex T: Terms

- End to End Channel Pair to Pair Resistance Unbalance (E2ECP2PRUNB) is the resistance unbalance between pairs of the same polarity. P2P_Iunb term is equivalent term used for simplicity.
  - E2ECP2PRUNB includes the effect of PSE vdiff and PD Vdiff.
    - Current Unbalance and Resistance Unbalance are identical terms.
- LPS: Limited Power Source per EN60950 is about maximum power of 100W. It is about power limiting *and not about current limiting* at normal operation mode. At normal operation and short circuit, current is limited according to 150W/Voc. See annex D for details.

References

#	Subject	
1	PSE Vdiff	http://www.ieee802.org/3/bt/public/jan15/darshan_03_0115.pdf
2	PD Vdiff	PD http://www.ieee802.org/3/bt/public/jan15/darshan_02_0115.pdf
3	Cable/Wire maximum current	http://www.ieee802.org/3/bt/public/jan15/diminico_01_0115.pdf
4	Number of cables in a bundle for Type 4 (95W)	page 18 at http://www.ieee802.org/3/bt/public/jan14/maguire_1_0114.pdf