4Pair PoE
Current unbalance

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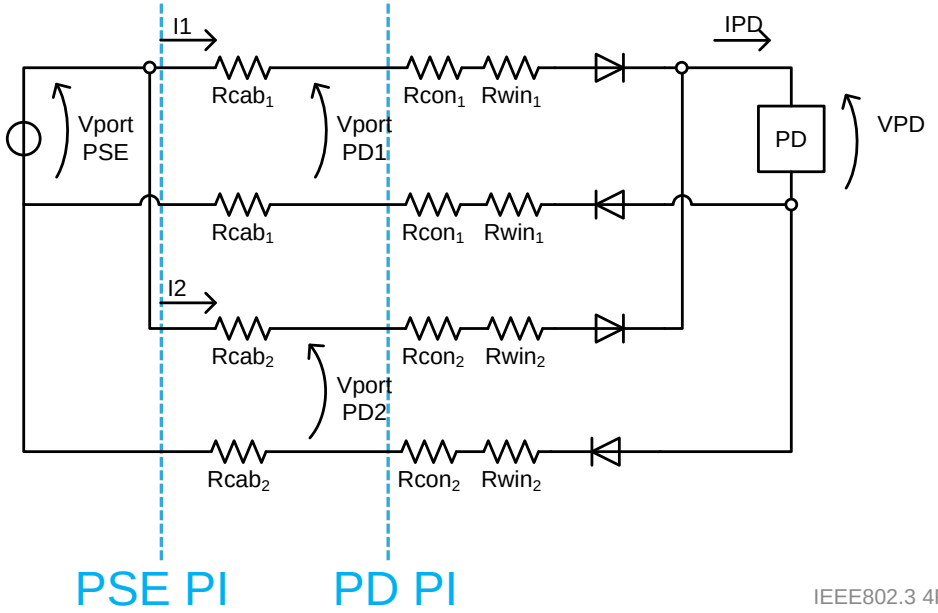
Introduction

- The purpose of this presentation is to provide a target value for Objective 4
  - **The project shall support a minimum of TBD Watts at the PD PI**
- The data used in this presentation come from the existing IEEE Std802.3-2012 standard.
  - **No new data will be used**
- The models shown are only an example of the simplest architectures that may be set up for a 4-pair system
- The scope is to show which are the causes of current unbalance in a real system, and their impact on power delivery
- In order to provide an easily achievable target a worst-case approach was used.
  - **In the Task Force there is room to make it better**

Assumptions

- This presentation uses the specification of a 2-pairs Type 2 system
  - **Vport_PSE min = 50V - as per Table 33-11**
  - **Channel maximum DC pair loop resistance = 12.5Ohm - as per Table 33-1**
  - **Cable resistance unbalance shall be 3 % or less**
  - **Icable = 0.6A – as per Table 33-1**
- The 4-pair PD was modeled as a single current source that draws current from the Alt-A and Alt-B through a diode bridge
- The PSE was modeled as a single voltage source

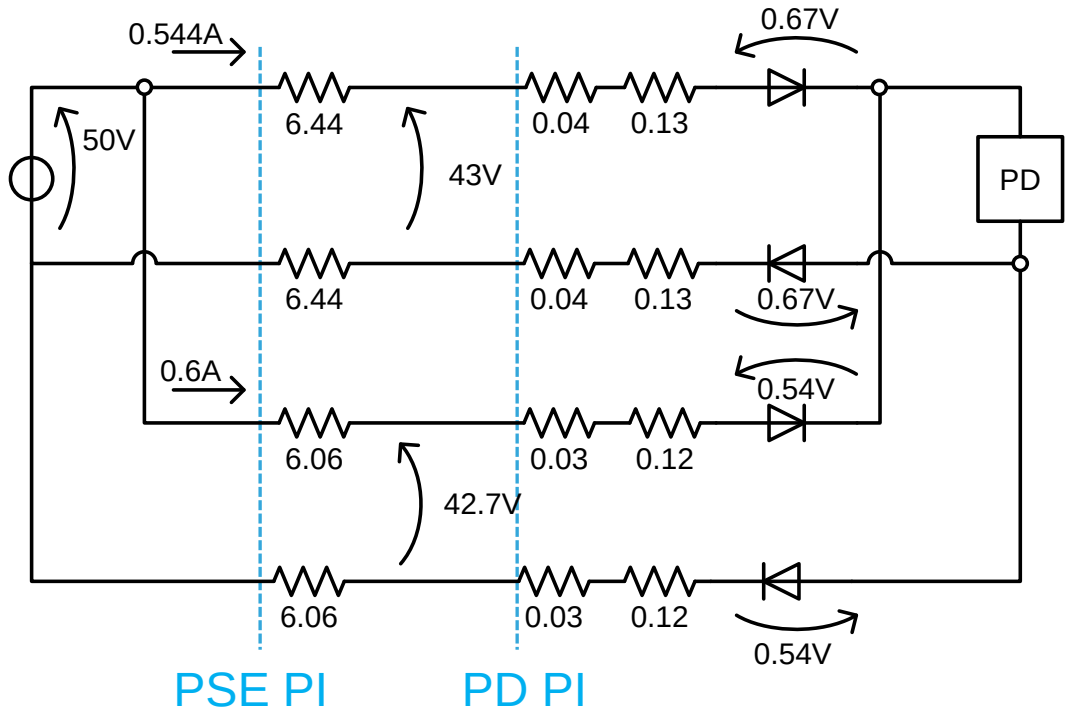


Unbalance estimation

- To estimate the current unbalance the following worst cases have been identified:
  - Cable resistivity: 125mOhm/m +/- 3%
  - Contact resistance: 30mOhm best case; 40mOhm worst case
  - Winding resistance: 125mOhm +/- 3.5%
  - Diodes (B1100 linearized model @0.6A): 0.3V+0.4Ohm*Id bc; 0.4V+0.5Ohm*id wc
- A spice simulation was performed to measure the current unbalance
  - The PD was modeled as a parametric current source
  - A dc-sweep was performed and the operating point was extracted when Icable=0.6A was met
- No more than 0.6A flows in any of the conductors
- The same simulation was repeated for different cable length between 1m and 100m

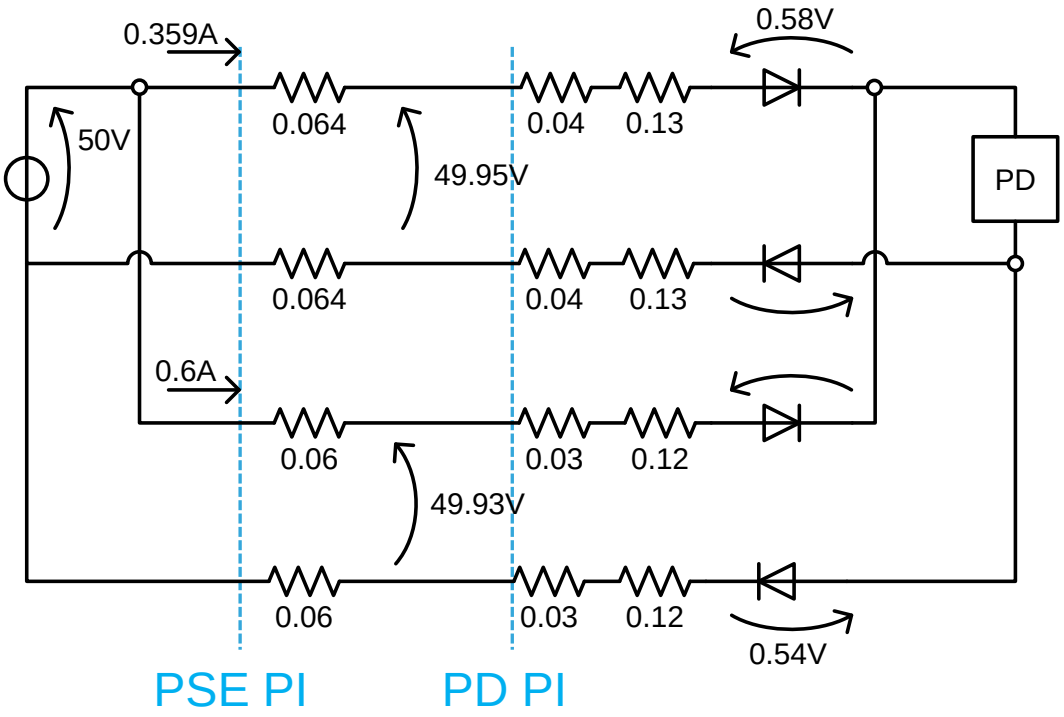
100m cable example

- 100m cable with maximum unbalance
- The current at each pair was clamped at 600mA
  - The highest current flows in the less resistive pair
- The available power at PD PI is 49.02W

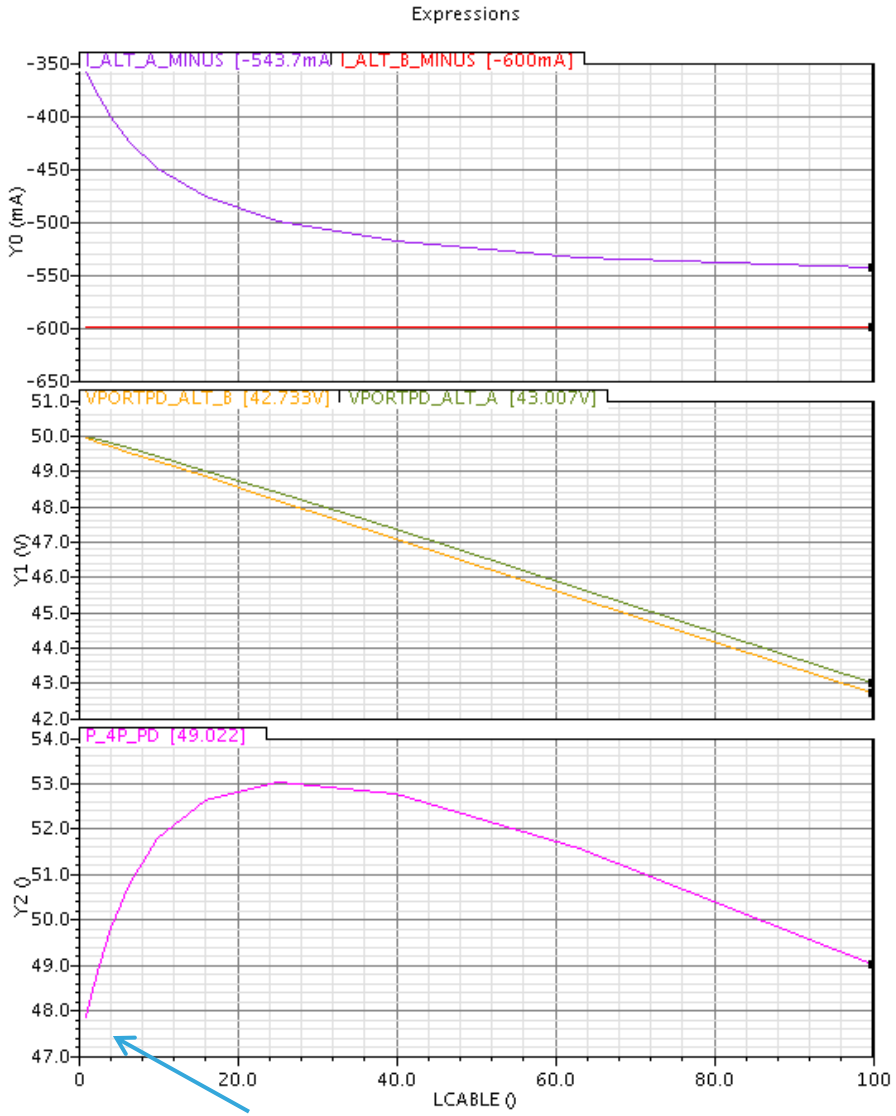


1m cable example

- 1m cable with maximum unbalance
- The “best” pair current is 0.6A, the other only 0.36A
- The available power at PD PI is 47.9W



Diode bridge 4P PD minimum power



47.9W @ 1m Cable

- The worst case power delivery is with short cables, due to heavy current unbalance.
- The current unbalance dramatically increases when the cable length is <10m
- The unbalance is due to the mix of diode forward voltage difference and very low shunt resistance
- Modeling the PSE as a real voltage source (with its series resistance) would give better results since it increases path resistance

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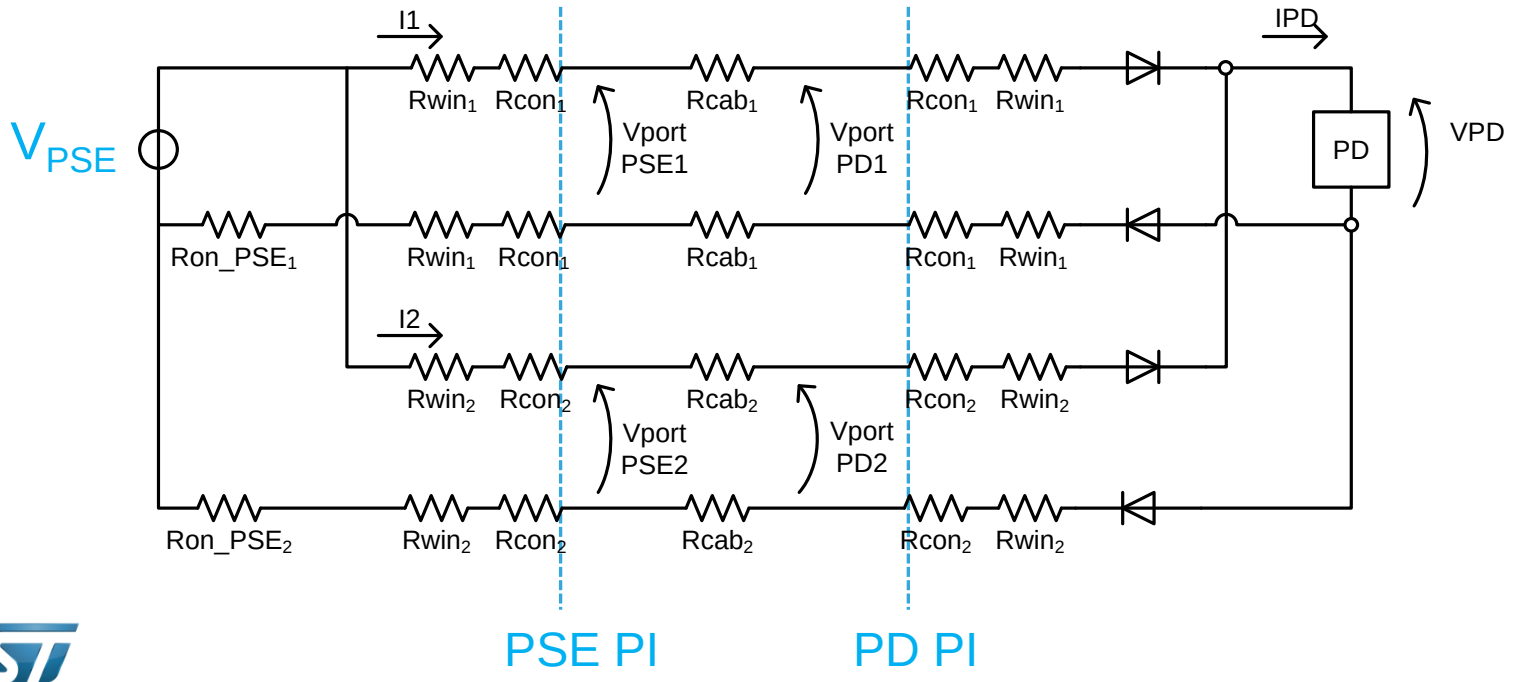
PSE output impedance effect

- In the previous models the PSE was modeled as an ideal 50V voltage source
- In real cases, PSE output impedance has en effect on current unbalance
- PSE ouput impedance was modeled as follows:
  - $Rout_{PSE}$=Rsense+Rds_on
  - Rsense=0.25Ohm
  - Nch Mosfet Rds_on=50mOhm best case, 100mOhm worst case
  - Contact resistance: 30mOhm bc; 40mOhm wc (same of PD port)
  - Winding resistance: 125mOhm +/- 3.5% (same of PD port)

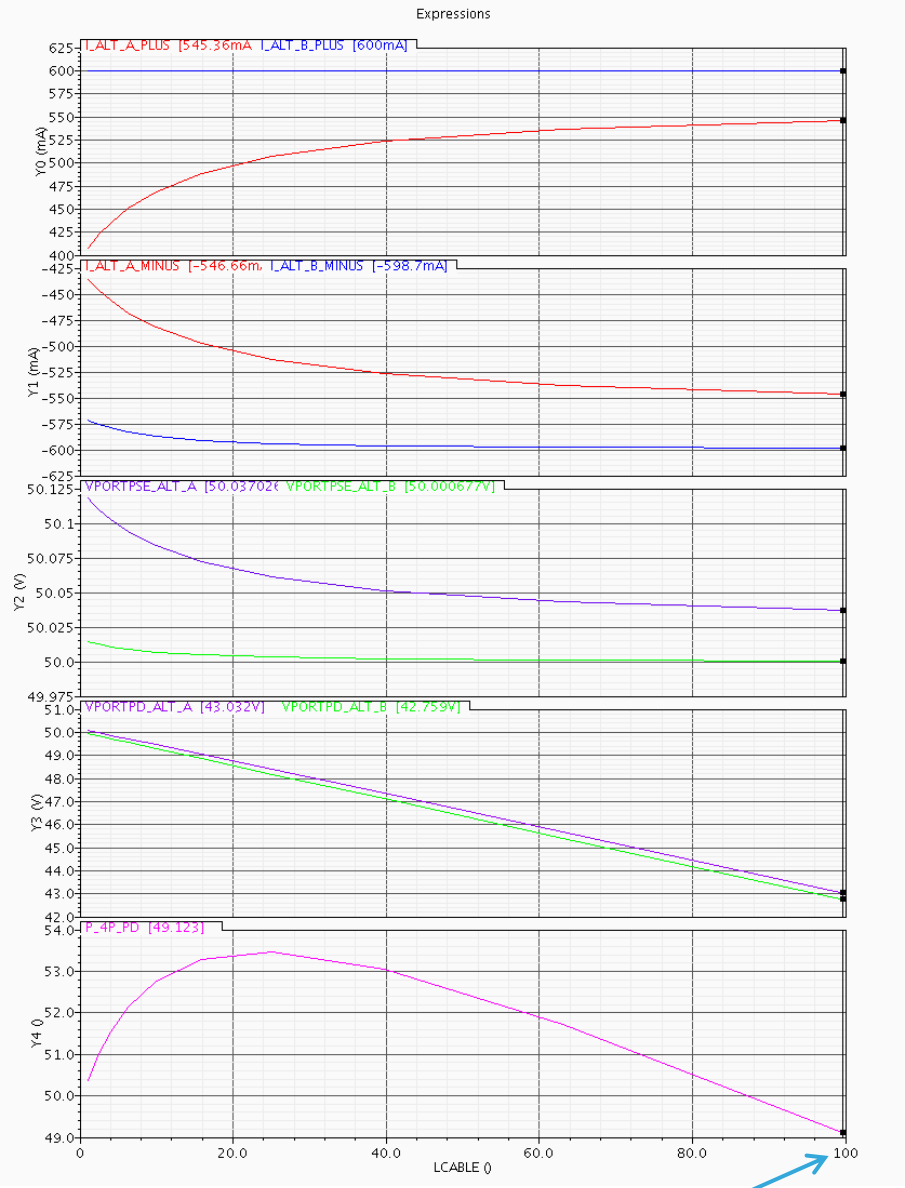
Real PSE + PD model

- Requirement: Vport_PSE_min=50V at the PSE PI
- To comply with this spec the PSE input voltage source must be at least :

$$V_{PSE} = 50V + 0.6A * \left(Rout_{PSE_{wc}} + 2R_{wind_{wc}} + 2R_{conn_{wc}}\right) = 50.414V$$



Real PSE + Diode bridge 4P PD min power max PSE resistance



49.1W @ 100m Cable

- A PSE with maximum output resistance on both the ports is a worst case for PD power delivery with long cable (100m)
- The highest current (clamped at 0.6A) flows in the less-resistive path
- The worst case power delivery with 100m cable is 49.1W
- The power delivery with short cables is better - 50.4W with 1m cable
- With real PSE model there is also an unbalance within the pairs (4.7% at 1m cable)

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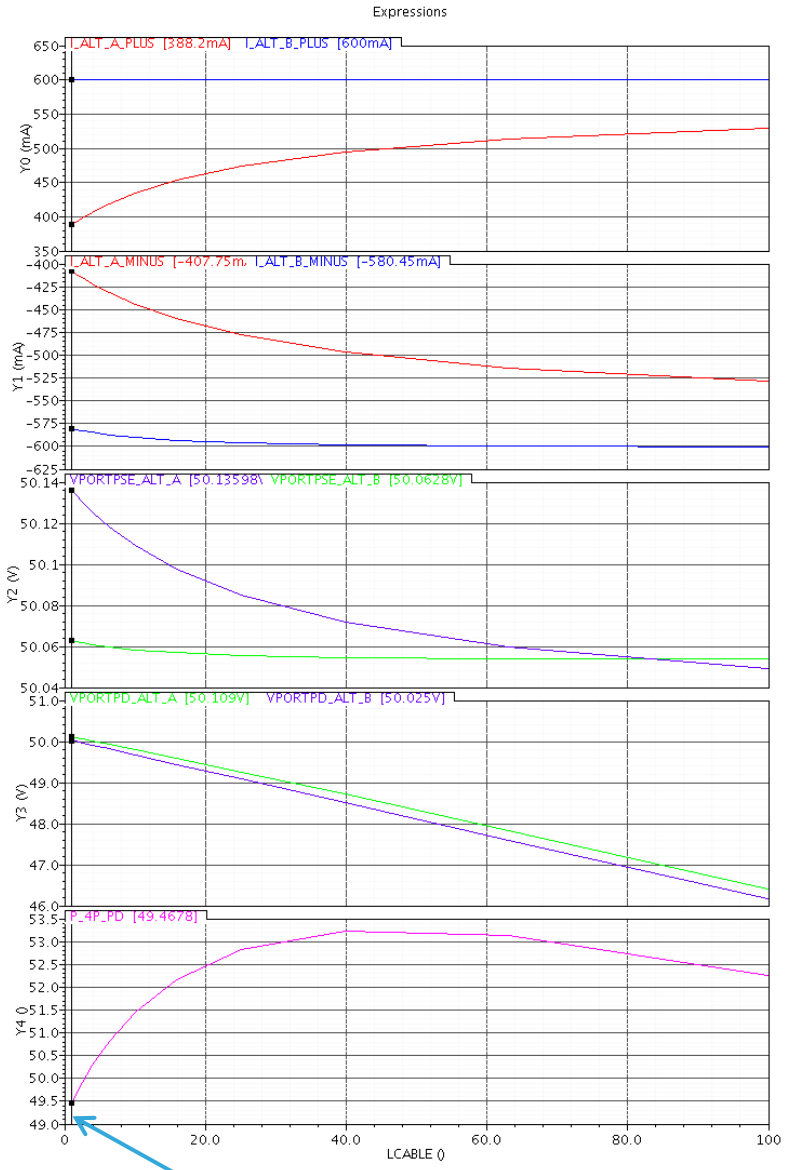
Real PSE + Diode bridge 4P PD min power with short cable



49.5W @ 1m Cable

- A PSE with maximum unbalance on output resistance is a worst case for short cables
- A very conductive cable is also a worst case condition for current unbalance
- The cable specific resistance was reduced to 6.68Ohm +-3% /100m to emulate a Cat6 cable (AWG 23)
- The highest current (clamped at 0.6A) flows in the less-resistive path
- The worst case power delivery with 1m cable is 49.5W

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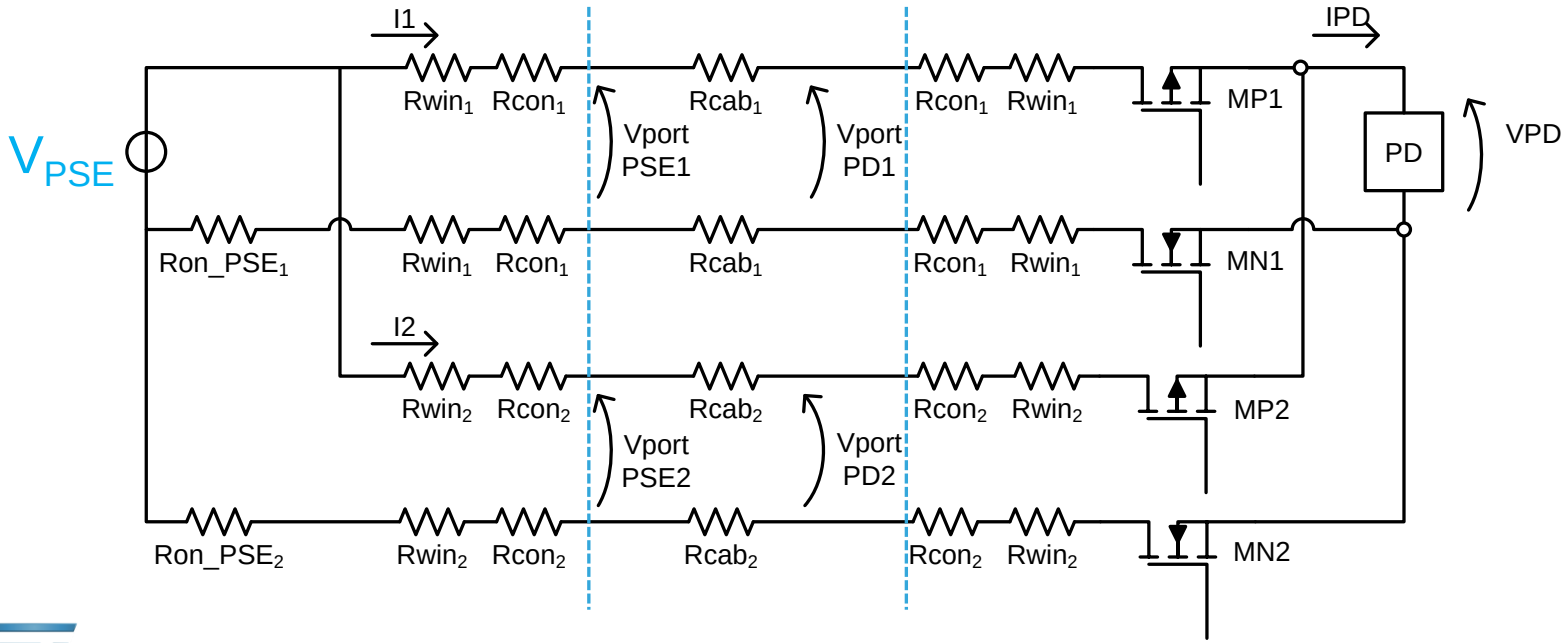
Real PSE + diode bridge 4P PD

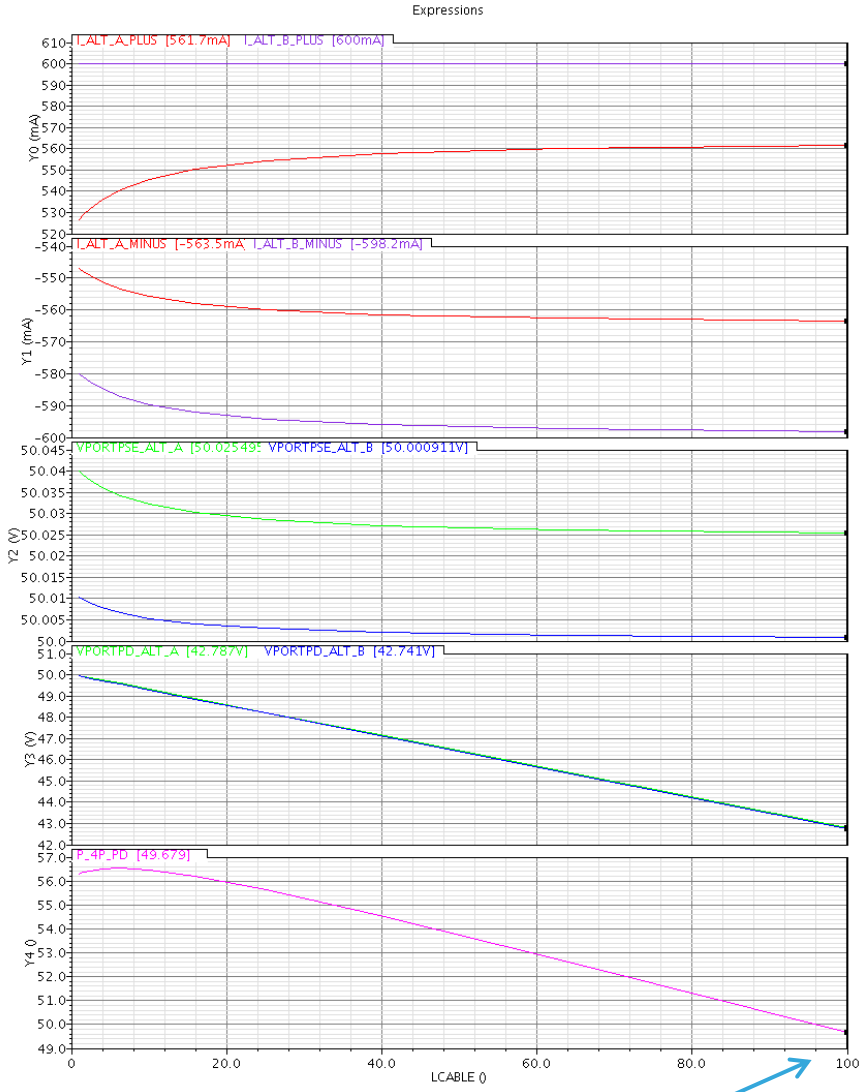
	Max PSE resistance		Max PSE port unbalance	
Cable length	*1m*	*100m*	*1m*	*100m*
VportPSE AltA	50.12V	50.04V	50.14V	50.05V
VportPSE AltB	50.01V	50.00V	50.06V	50.05V
I AltA Plus	407mA	545mA	388mA	529mA
I AltA Minus	436mA	547mA	408mA	528mA
I AltB Plus	600mA	600mA	600mA	600mA
I AltB Minus	572mA	599mA	580mA	600mA
VportPD AltA	50.06V	43.03V	50.11V	46.41V
VportPD AltB	50.01V	42.76V	50.02V	46.16V
P 4P PD	**50.36W**	**49.12W**	**49.47W**	**52.24W**

Active Bridge PD model

- Another 4P PD model has been investigated to check if better current balance is acheivable
  - Pch mosfet: 150mOhm bc, 200mOhm wc
  - Nch mosfet: 75mOhm bc, 100mOhm wc
  - Other unbalance figures are the same as diode bridge PD model



Active bridge 4P PD minimum power



49.7W @ 100m Cable

- The worst case for PD power delivery is when both PSE ports have the highest Rout
- With this model the lowest power available at PD PI is with 100m cable 49.7W
- The PD power characteristic is almost linear, with no decrease for short cables.
- Since the upper and the lower conductor of each pair has different DC resistance, a current unbalance within pairs is present, and it is higher for short cables

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Conclusion

- There are two corner cases for power delivery
- The first is with 100m, 12.5Ohm Cable, maximum parasitic resistances and maximum unbalance between the two couples of pairs
- The second is with 1m cable, minimum parasitic resistances and maximum unbalance between the two couples of pairs
- In both the conditions a power delivery of more than 48W (47.9W with ideal PSE) is achievable with simple PSE and PD design, and without exceeding 0.6A on any conductor.
- I suggest to use 48W as the objective for the minimum power at the PD PI
- Higher power delivery is achievable with more complex PD design