# 802.3at: Select Issues

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# PD Power Draw Specification

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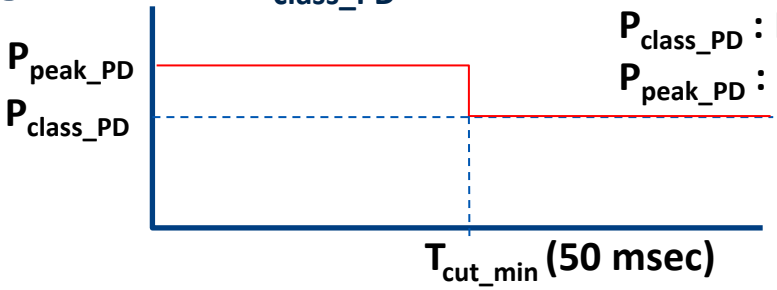
## Table 33-18: $P_{class\_PD}$

- Maximum wattage by PD Class (e.g. 25.5 for class 4)

## Figure 33-18: $P_{class\_PD}$




$P_{class\_PD}$ : Maximum power $P_{class\_PD}$ max (Tbl. 33-18)
$P_{peak\_PD}$ : Peak operating power $P_{peak\_PD}$ max (Tbl. 33-18)

## Section 33.3.7.4

Iportmax = ($P_{class\_PD}$ / $V_{port\_PD}$), $P_{class\_PD}$ is the maximum power $P_{class\_PD}$ max (33-18)

…

$P_{peak\_PD}$ = (1.11 X $P_{class\_PD}$), $P_{class\_PD}$ is the input average power

## Section 33.3.7.2

The maximum average power, $P_{class\_PD}$ in Table 33-18…is calculated over a 1 second interval.
… Average power is calculated using any sliding window with a width of 1 sec.

## ISSUE: What if LLDP defines $P_{class\_PD}$ max (power grant)?

$P_{peak\_PD}$ and $P_{class\_PD}$ in Figure 33-18 cannot be $P_{class\_PD}$ **max**, $P_{peak\_PD}$ **max** from Table 33-18

# AC Ripple/Noise Specification

## Table 33-11:

- **4 Frequency Bands**
  - < 500Hz (.5Vpp)
  - 500Hz to 150KHz (.2Vpp)
  - 150KHz -500KHz (.15Vpp)
  - 500Hz-1MHz (.1Vpp)
- **Para 33.2.7.3**
  - Common mode or Pair-to-Pair
  - 10mA – $P_{type}$ min power levels
  - Preserve Data Integrity

## ISSUE: What are practical test conditions ?

- **802.3af included test circuit with 0.1μF load**
  - Note: Minimum (worst case) detection capacitance = 0.05μF (table 33-14)
- **PD $C_{port}$ min(powered state) = 5μF**
  - Note: This is at the PD interface, not the PSE interface
- **Assuming typical high frequency source impedance, capacitive loading will make ALL THE DIFFERENCE in measurement outcomes, especially above 500Hz**

# LLDP Timing

## When Does a PSE First Produce PoE LLDP Message to a PD ?

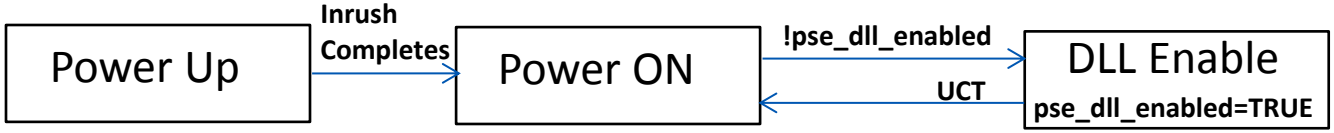
## Paragraph 33.6.2:

A Type 2 PSE shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in this PSE as indicated by the variable **pse_dll_enabled** (33.2.4.4, 33.6.3.3)

## Paragraph 33.2.4.4

**pse_dll_enabled** A variable indicating whether the Data Link Layer classification mechanism is enabled

## PSE State Diagram 33.2.4.7




## So what's the requirement?

- **10 seconds after inrush complete?**
- **UCT: If UCT is forever, what's the point of 10 seconds ?**

# LLDP TLV's

## Clause 79.3.2 PoE LLDP Message

| LLDP Headers | Power Via MDI<br>*3 octets Para 79.3.2.1 - .3* | Power Via MDI Extended<br>*5 octets Para 79.3.2.4 - .6* |
|---|---|---|

## Clause 79.3.2.1 - .3 Power Via MDI

- **MDI Power Support: Port Class (PSE / PD), PSE MDI Power Support, State, Pair Control**
- **PSE Power Pair: IETF RFC 3621 designator**
- **Power Class: IETF RFC 3621 designator (1 to 5)**

## ISSUE: Relevance and Content of Power Via MDI TLV's

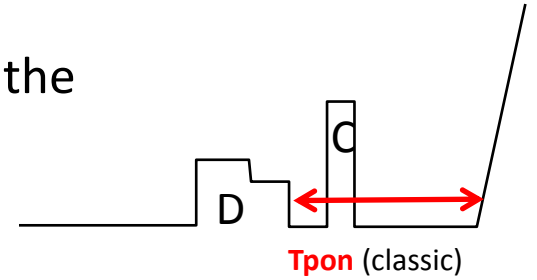
- **Information extraneous to 802.3at LLDP power negotiation – that only needs the "Extended" content**
- **Many LLDP PSE's don't appear to populate these correctly today**

  **(e.g. PSE MDI Power Support = NONE)**

# Ambiguous Tpon

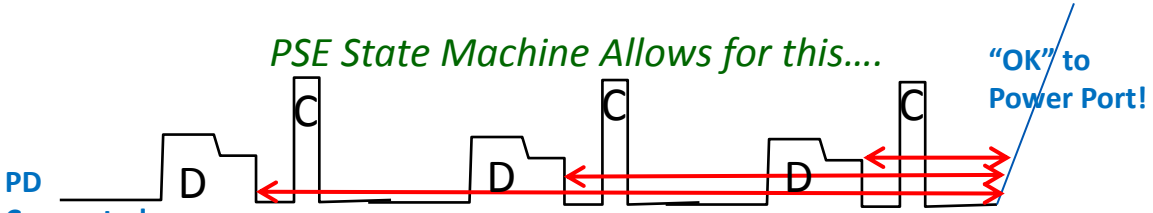
## Tpon Objective:

- Prevent powering non-PD's by minimizing the time from a successful detection until the power-up



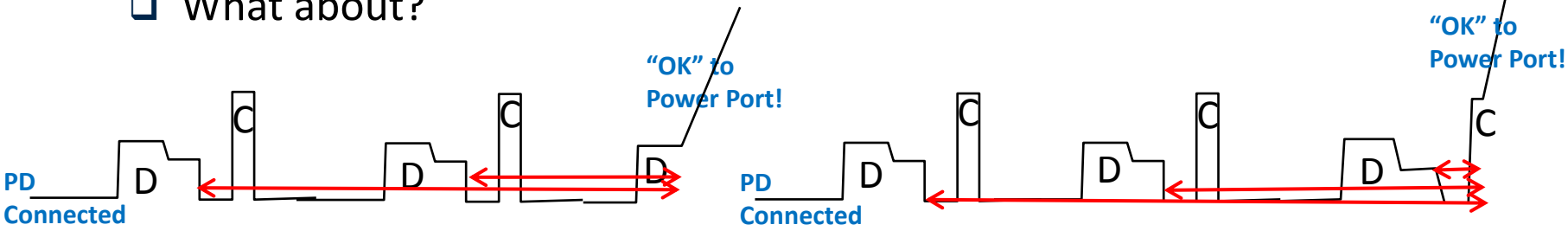

## Software Managed PSE State Machines

- The "necessary evil" given complex PSE power management situations




*But what is Tpon? How do we know which detection measurement determined the eventual power-up?*

- What about?



# Combined 2-Event & LLDP

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## Para. 33.3.2.6 and Table 33-8

- Possible award candidate for "**Hardest Table to Comprehend**" !
- Table 33-8 allows for combination of LLDP and 2-Event power grants
- Text allows: …2-Event Physical Layer classificatinn and Data Link Layer classification….

## Issue:

## Those who think "MORE IS BETTER" implement BOTH 2-Event and LLDP Classification (power-grants).

- In a PSE that must allocate a limited power budget, it is *generally illogical* to precede LLDP negotiation with a 2-Event grant for the full 25.5 watts.

## Recommendation:

- We cannot reverse this, but we could add some text pointing out that this is not a recommended configuration in systems that must allocated limited power resources.

# Combined AC MPS / DC MPS

## Para. 33.2.9.1

- The PSE shall monitor either the DC MPS component, the AC MPS component, or both.

## Issue:

## Those who think "MORE IS BETTER" implement BOTH AC MPS and DC MPS.

- In practice, DC MPS will always prevail as a 5 mA (or even a 1 mA) DC load will look like lower impedance than 25KΩ meaning AC MPS is really doing nothing.

## Recommendation:

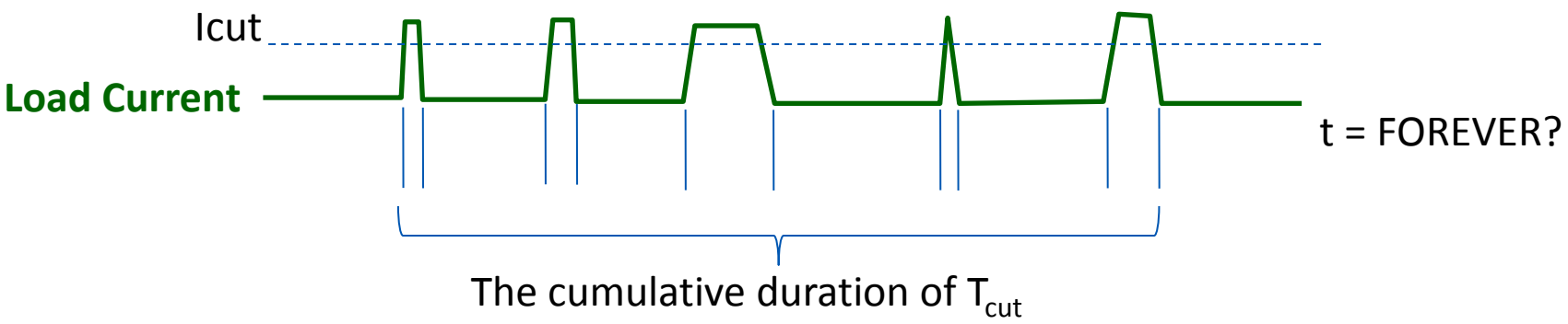
- We cannot reverse this, but we could add some text pointing out that this is not a recommended configuration to have both methods.

# Icut / Tcut Specification

## Para. 33.2.7.6 Overload Current

- Concept of required overload processing removed from 802.3at
- If $\mathbf{I_{port}}$, the current supplied by the PSE to the PI, exceeds $\mathbf{I_{cut}}$ for longer than $\mathbf{T_{cut}}$, the PSE may remove power from the PI. The cumulative duration of $\mathbf{T_{cut}}$ is measured with a sliding window of at least 1 second width.
- Table 33-1: $\mathbf{I_{cut}} = \mathbf{P_{class}} / \mathbf{V_{port\_PSE}}$, $\mathbf{T_{cut}}$= 50 to 75 msec

## ISSUE: What is a Violation of Icut/Tcut?



# DC Unbalance

## Table 33-11 Current Unbalance

- Max 3% of $I_{cable}$ ($I_{cable}$ = 350mA for Type-1, 600mA for Type-2)
  - 10.5 mA for Type-1, 18 mA for Type-2 PSE
- Para 33.2.7.11
  - … Type-2 Endpoint PSE's shall meet the requirements of 25.4.4a in the presence of ($\mathbf{I_{unb}}$/2) [These are droop specifications, $I_{unb}$ / 2 = $I_{bias}$]

## ISSUE: What Really Is the Requirement?

- **Is 3% of $I_{cable}$ the PSE <u>CONTRIBUTION</u> to DC Unbalance ?**
  - Most of Table 33-11 is describing PSE behaviors…
- **Is 3% of $I_{cable}$ the amount of DC Unbalance the PSE should <u>TOLERATE</u> and meet 25.4.4a ?**
  - DC Unbalance can (and will) be introduced by link elements such as Cabling, Connectors, PD's…
  - DC Unbalance TOLERANCE assessment is really a PHY assessment