Architectural Options and Technical Feasibility of 200GbE

IEEE P802.3 Next Generation 100 Gb/s Ethernet &
200 Gb/s Ethernet Study Group

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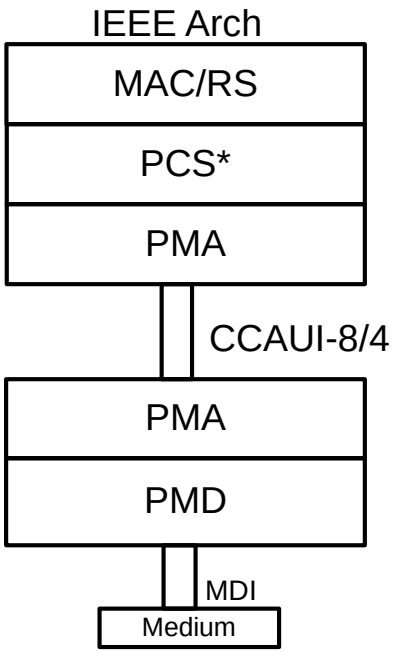
Introduction

- This looks at an architectural option and technical feasibility of 200GbE
- The following assumes reusing the 802.3bs architecture, and that FEC is always required
- Supports 8/4 lanes (25G and 50G)

PCS Architecture

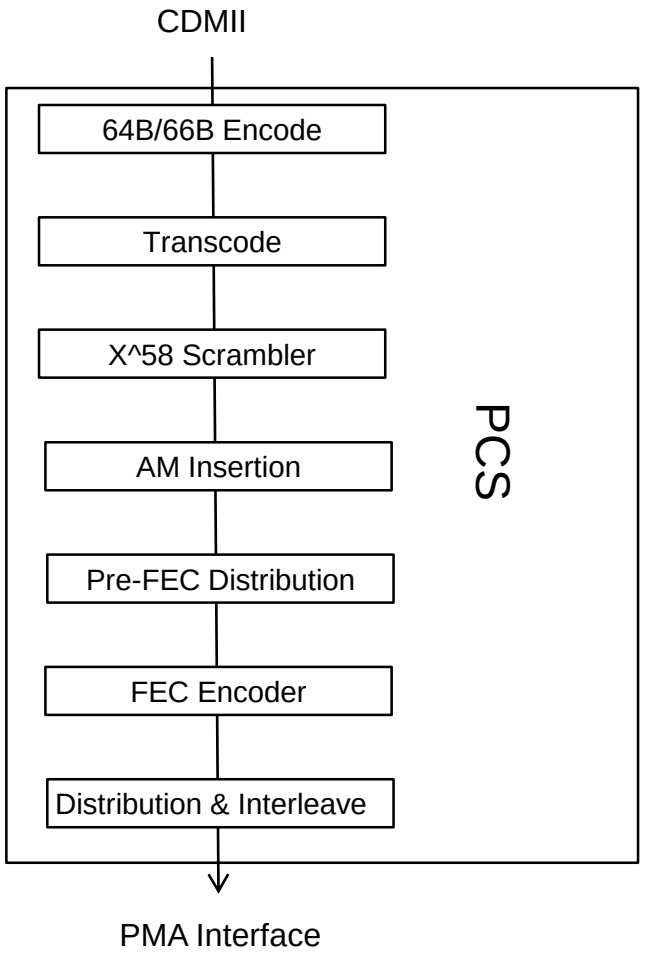
- Based on the draft 802.3bs system architecture
- A single FEC is used, across up to 5 interfaces (in the PCS sublayer)
- CCMII is an optional interface that is not shown in these figures, but is already adopted and may be present in a given implementation



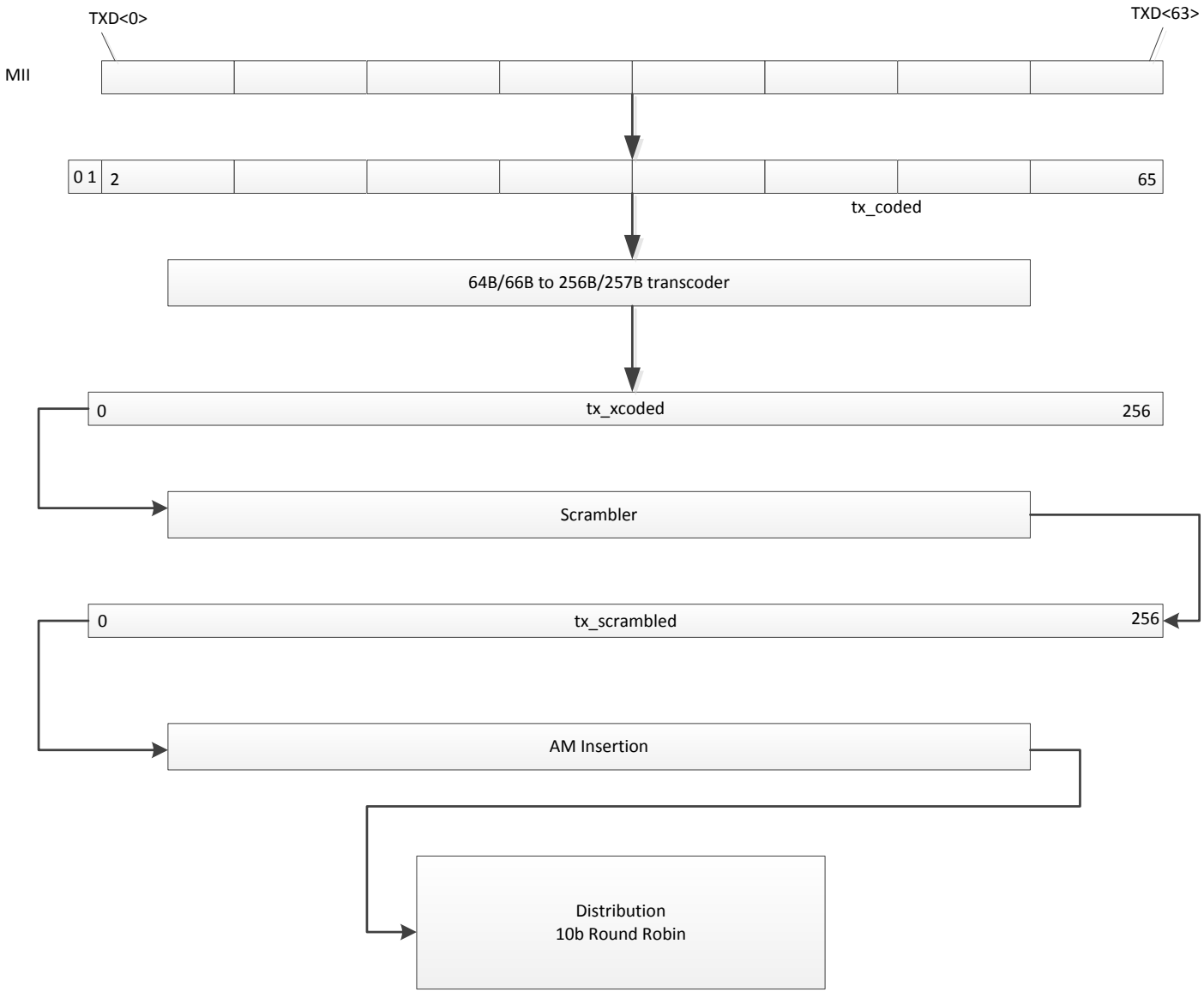
*FEC is part of the PCS sublayer

Possible TX PCS Data Flow

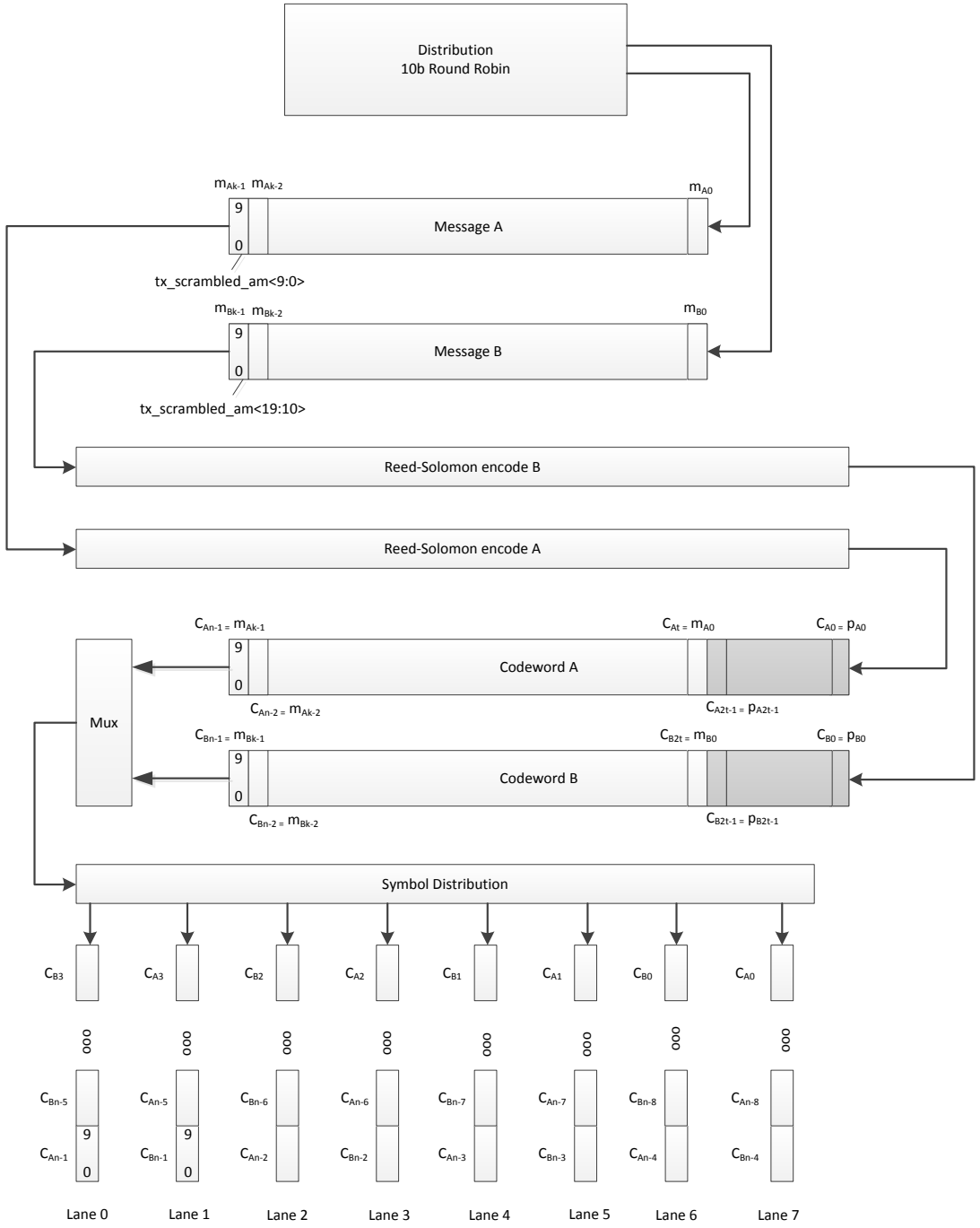
- 64B/66B encode based on clause 82/119
- Transcode to 256B/257B based on clause 91/119
- Scrambler is moved to after the Transcoding to simplify the flow, standard X^58 scrambler
- Alignment Markers are the same format as clause 119
  - Common Marker portion is the same, have new unique portion for 200GbE
  - Same AM distance
- Assuming FEC Encoder is RS(544,514,10)
  - Proposed that all FEC processing is as in clause 119, including data distribution and interleaving
- Support for any logical lane on any physical lane



200GbE Data Distribution



Distribution Cont



PMA Functions

- Identical PMA functions as clause 120
- Support for bit muxing and any logical lane to any physical lane
- With KP4 FEC the per lane signaling rate is:
  - 544/514*257/256*25G = 26.5625G
  - When running 8lanes
  - When running 4 lanes it is 53.125G per lane

Conclusion

- This presentation looks at one option for the 200GbE architecture
- This architecture is feasible, it follows 802.3bs architecture which has been shown to be technically feasible
- Achievable latency is ~110ns with similar performance/gain as 400GbE
- It does need to be shown if this architecture is sufficient or optimum for all PMD objectives that might be adopted in this study group

- Once PMDs objectives are adopted, then we need to look at the gain requirements and error propagation properties of set of PMDs, then perform an analysis to see if this architecture is optimum/sufficient for the set of PMDs chosen

Thanks!