Architectural Options and Technical Feasibility of 50GbE

IEEE P802.3 50 Gb/s Ethernet Over a Single Lane Study Group

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Introduction

- This looks at architectural options and technical feasibility of single lane 50GbE

Options

- There are several valid and technically feasible options for single lane 50GbE, all based on reuse from existing (or soon to be existing) Ethernet standards. Here are several options that come to mind:

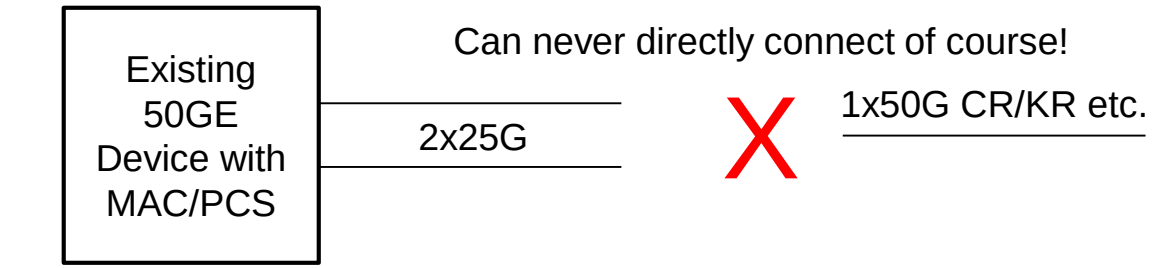
1. Re-use existing 40/50G PCS/MACs architecture
   - 4 PCS lanes
   - RSFEC sublayer (use either RS544 or RS528)
   - No FEC interleaving
2. Single lane PCS with existing RSFEC
   - 1 lane only use either FEC sync or a single CWM
   - RSFEC sublayer (use either RS544 or RS528)
   - No FEC interleaving
3. Single lane PCS with RSFEC Interleaving
   - FEC sync (or CWM)
   - Interleave nx RSFECs (use RS544)

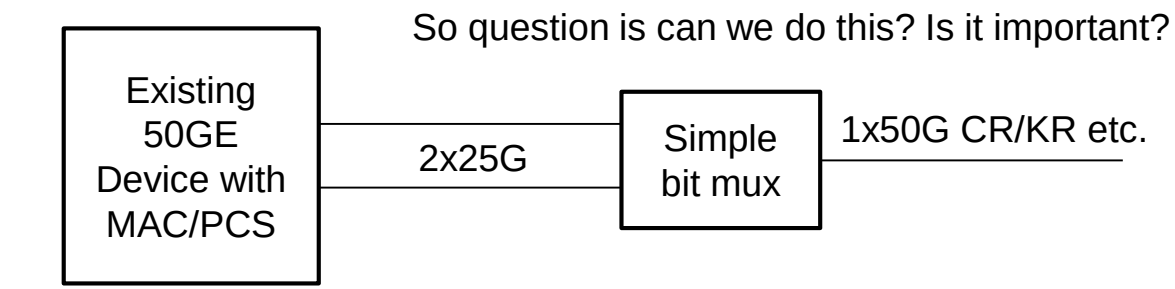
Questions to Answer

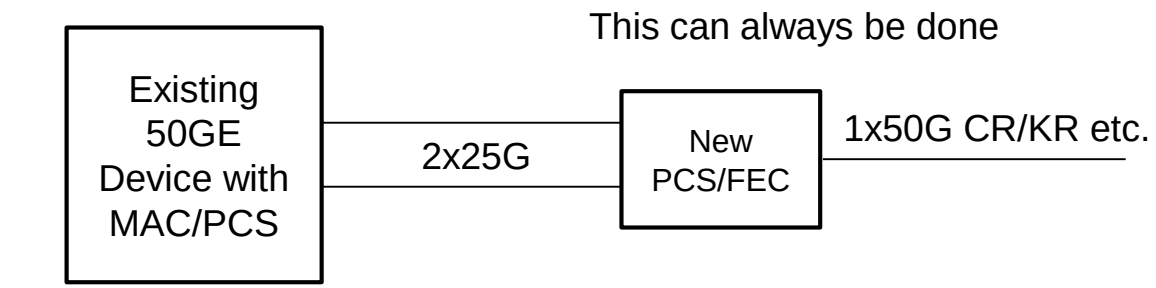
- Decide on the PMD set for the project
- Once PMDs objectives are adopted, then we need to look at the gain requirements and error propagation properties of the set of PMDs, then perform an analysis to see what FEC architecture is optimum/sufficient for the set of PMDs chosen
  - 50G per lane backplane, copper cable and MMF PMDs in particular have not yet been well studied for their error models and gain needs
- Is backwards compatibility/commonality important?
  - To current industry standard for 50/40GE?

Backwards Compatibility

- What does this mean when we go from 2 lanes to 1 lane?







Conclusion

- 50GbE is technically feasible from the logic and architectural point of view
- There is a lot of previous work that can be leveraged
- We need to better understand the PMD error models and gain requirements
- And decide on how much compatibility with previous standards is desirable

Thanks!