

THE CASE FOR 100G OVER 2 LANES

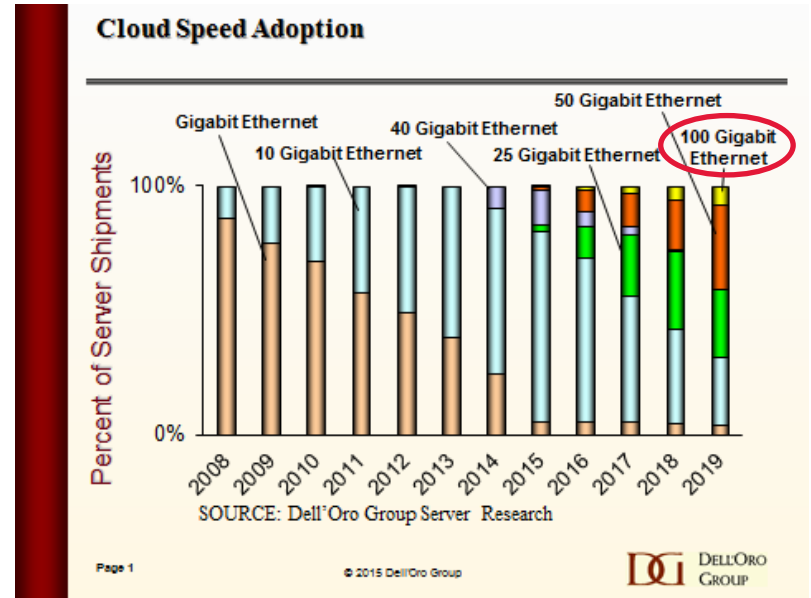
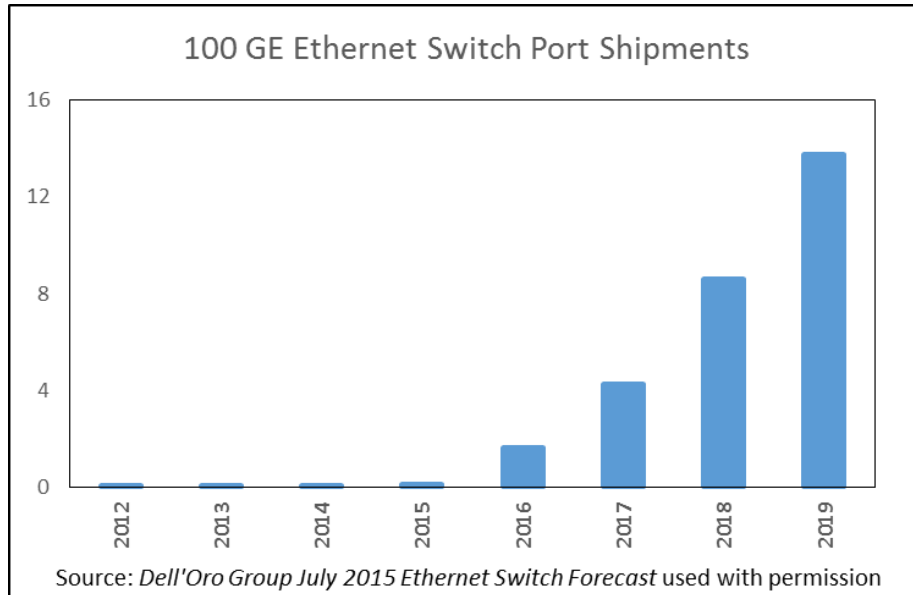


Rob Stone

IEEE Study Group - 50G / NGOATH, Atlanta January 2016

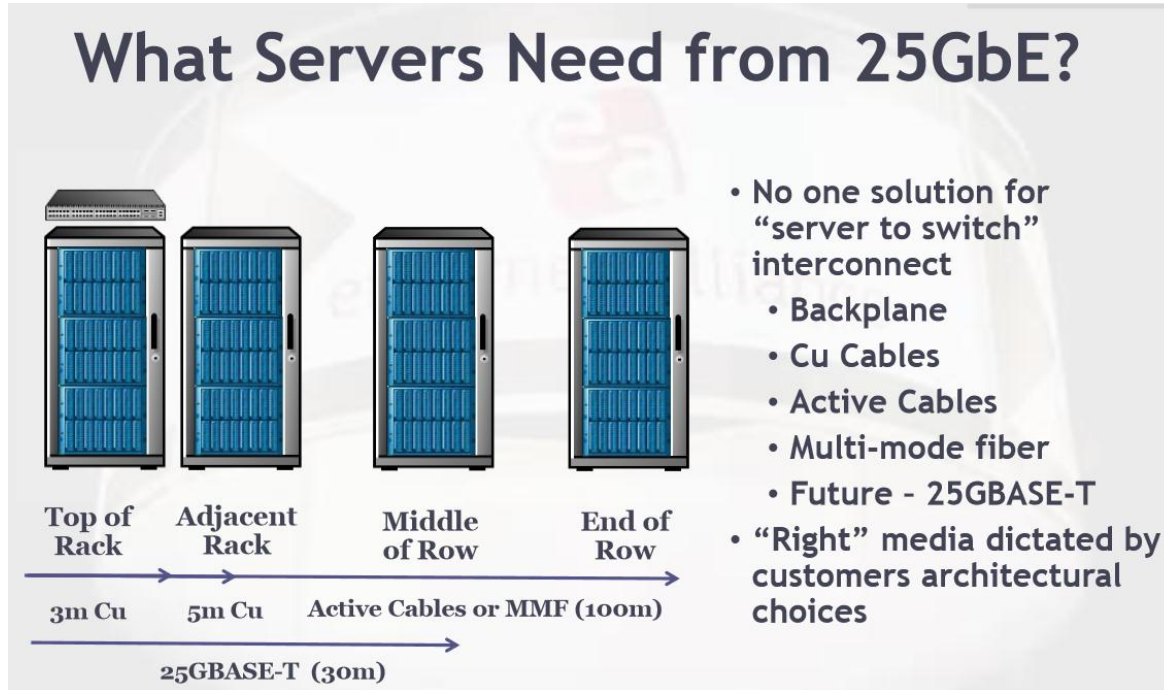
- **Vasu Parthasarthy, Broadcom**
- **Scott Kipp, Brocade**
- **Tom Palkert, Molex**
- **Scott Somers, Molex**
- **Eric Baden, Broadcom**
- **Mark Gustlin, Xilinx**
- **Greg McSorley, Amphenol**
- **Chris Cole, Finisar**
- **Brad Booth, Microsoft**
- **Kent Lusted, Intel**

- **100G currently is and will remain an important port speed**
 - Network Spine - forecast > 13M ports in 2019
 - Server Attach (Migration from 1G → 10G → 25G → 50G → 100G)



Source: Dell'Oro Controller and Adapter Forecast July 2015 - Used with permission

- **Server attach is evolving – not just DAC / Backplane**
 - (Argument from 25GbE, but holds for higher server attach speeds)



Source: http://www.ethernetalliance.org/wp-content/uploads/2014/12/Introduction-to-25GbE-Webinar_D2p1.pdf

OBSERVATIONS – MULTI-LANE PORT CONFIGURATIONS

25G Serdes
4 Lane Port

Port Speed (Gb/s)	Lane Rate (Gb/s)	# Ports Possible in 4 lanes
100	25	1
50	25	2
25	25	4
40	10	1
10	10	4

- Typically multi-lane ports can be configured to support different rates
- Optimal efficiency in terms of ASIC IO when operating at max serdes speed
 - Least # lanes (lowest cost PMDs)
 - For switches – highest BW & Radix
 - → Lowest cost network

50G Serdes
8 Lane Port

Port Speed (Gb/s)	Lane Rate (Gb/s)	# Ports Possible in 8 lanes
400	50	1
200	50	2
100	50	4
50	50	8
100	25	2
50	25	4
25	25	8

← 2 x more lanes needed in “downspeed” mode

- **100GE is forecast to remain an high volume, important rate through at least 2019**
 - The industry will take advantage of opportunities to improve 100GE efficiency
 - Maximize ASIC bandwidth (run lanes at max serdes speed) – 2 x better
 - Minimize PMD width (lower cost) ~ 2 x lower cost (PMD dependent)
 - IEEE is the right venue to do this work!
- **100G over 2 lanes is a viable technology, bookended by 802.3bs and OIF-CEI-56G work**
 - In contrast 100G / lane electrical technology is still very early stage (too early for standardization)
- **It is highly probable that vendors developing multi-lane ports will implement the whole set of port speeds**
 - (For 50G serdes, this means 50, 100, 200 and 400GE)
 - If we undertake 50 and 200GE logic standardization, incremental effort to do 100G is small
- **Including 100G over 2 lanes in the 50 / NGOATH projects will enable beneficial architectural and logic consistency with other IEEE port speeds**

Thanks!