Multi Lane PCS Proposal for 50GbE & NGOATH

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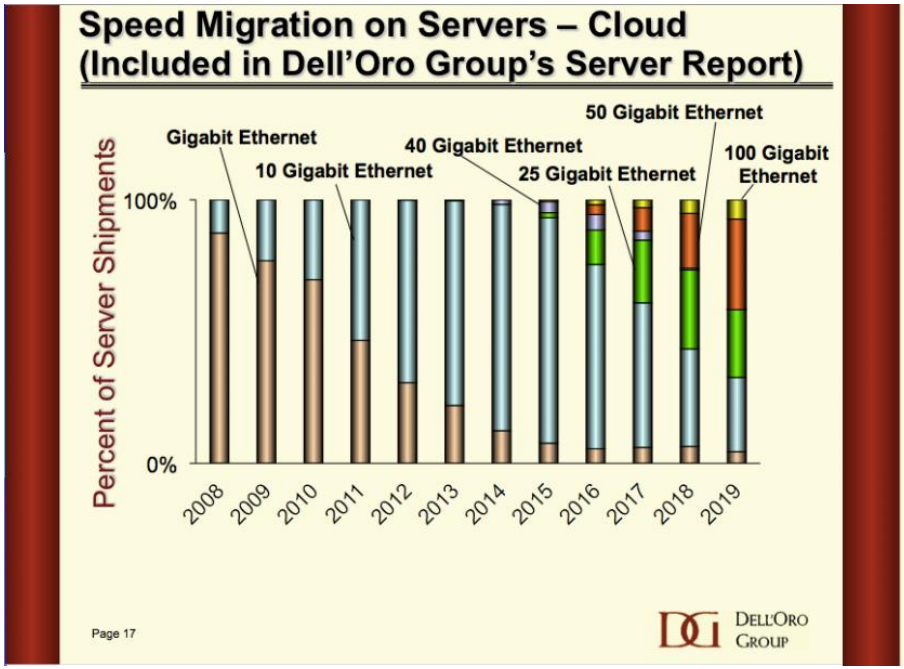
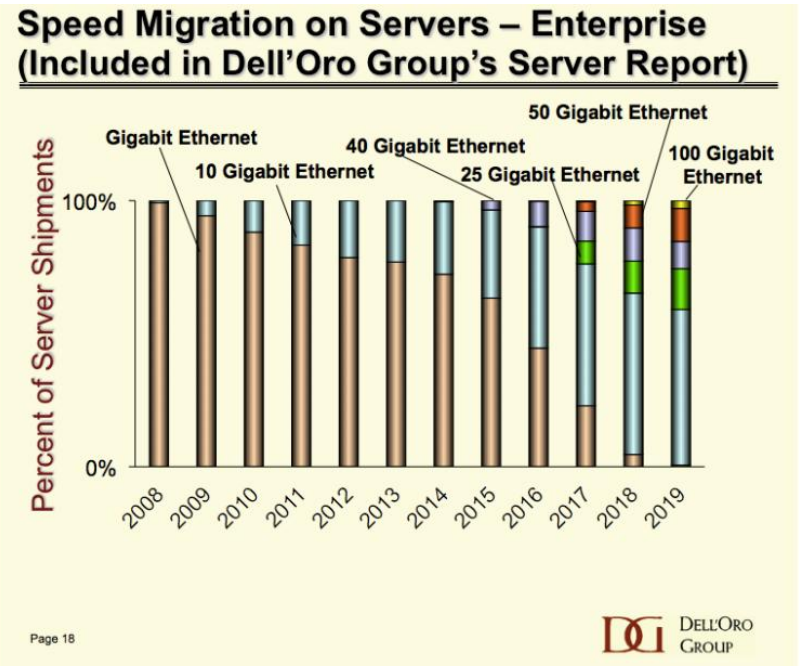
Forecast 50GbE Application in Server

- 50GbE rate migration is expected from 2016 or 2017
- Will single lane PCS supporting only 50G IO in C2C/C2M interface impede early deployment of 50GbE&NGOATH?

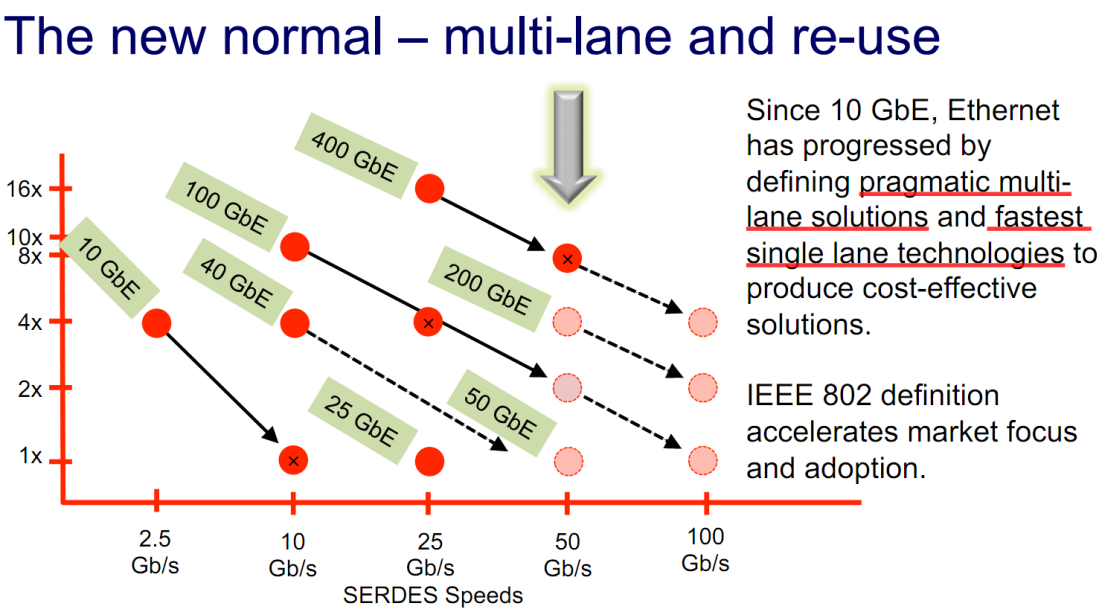




Refer to CFI_01_1115

Electrical Interface History in 10/100/400GbE

- At least two generations of chip-to-module interface defined in IEEE 10/100/400GbE standards to enable diverse pluggable module solutions



CFI_01_1115

- According to 50G_NGOATH_PAR_0116,
  - "**Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 03/2018**"
- Can we assume 50GbE host ASIC with only 50G IO is the best solution from cost, power and performance perspective at that time?

Reuse Existing 25Gbps Class SerDes Standard in IEEE

- Refer to Annex 83D/E: CAUI-4
  - Works well with multiple legacy PMDs, with No FEC or KR4 FEC PMDs because they have same bit rate @25.78125Gbps
  - Bit error rate is limited to less than 1E-15
  - Backward compatibility
- Refer to Annex 120B/C: CDAUI-16
  - Running @26.5625G, with 3% Overclocking for KP4 FEC comparing to CAUI-4
  - Bit error rate is limited to <= 1E-6, with much lower actual BER expected in final product
  - Forward looking to 50G IO capability

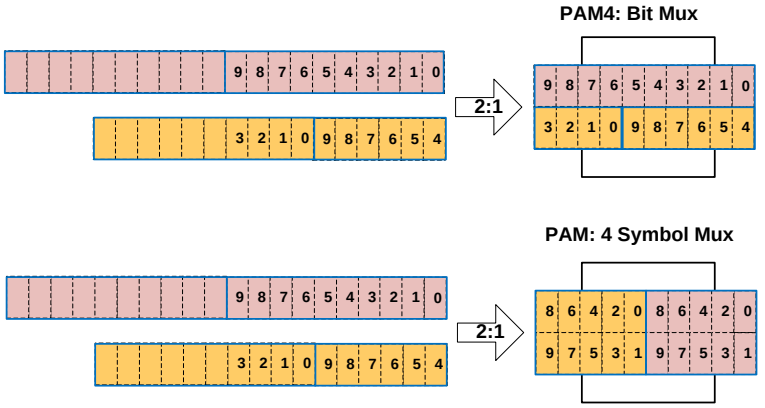
Options of SerDes Interface of 50GbE

- Option 1: 50GAUI
  - Running at 53.125Gbps (2x26.5625Gbps)
  - Capable of 3% Overclocking for KP4 FEC
- Option 2: 50GAUI-2
  - Running at 26.5625Gbps
  - Capable of 3% Overclocking for KP4 FEC, Interoperate capability with 50GAUI in option 1 with 50GAUI
  - Support No FEC in bypass mode, with stuffing bits
- Option 3: 50GAUI-2
  - Running at 25.78125Gbps
  - Capable of KR4 FEC or No FEC

Cost of Supporting 25Gbps SerDes Interface

- Multi lane PCS:
  - Requires distribution on TX side, de-skew and reorder on RX
  - Not significant extra logic cost

- PCS/PMA in pluggable Module
  - PMA w/ Bit-Mux, protocol agnostic
  - PMA w/ Symbol-Mux, protocol aware
  - FEC conversion needed if KR4/KP4 FEC coexist



- FEC capability penalty
  - PMA schemes will introduce different FEC coding gain loss

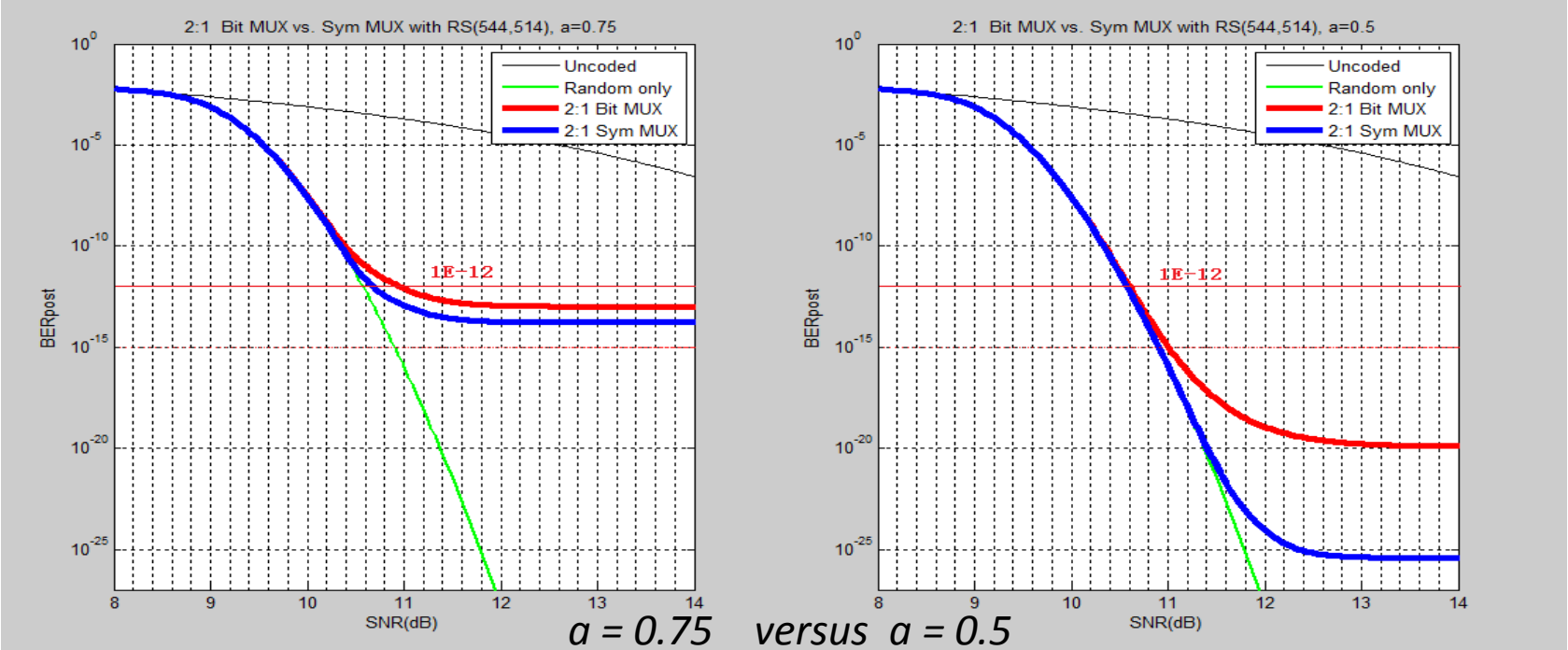
50GbE FEC Coding Gain Analysis

- 50GAUI-2 is safe w/ bit Mux or symbol Mux, if covered by KP4 FEC
  - Because of low BER rate (~1E-15) on 25.78125G/26.5625G SerDes
- 50GAUI has risk in FEC capability, w/ bit Mux or symbol Mux, if covered by KP4 FEC
  - Either bit Mux or symbol Mux with KP4 FEC has risk to cover PCS to PCS connection , assuming 1E-6 BER on 50G Serdes IO as OIF-56G-VSR-PAM4 /OIF-56G-MR-PAM4
  - Bit Mux loss 0.3dB than symbol Mux

Aim for 1E-12	Electrical DER, a=0.75		Optical DER	
Bit Mux	Burst	5E-7	Random	2.4E-4
Symbol Mux	Burst	2E-6	Random	2.4E-4

**Calculated on two part link model as in slides#3 of "wang_x_3bs_01_0915"*

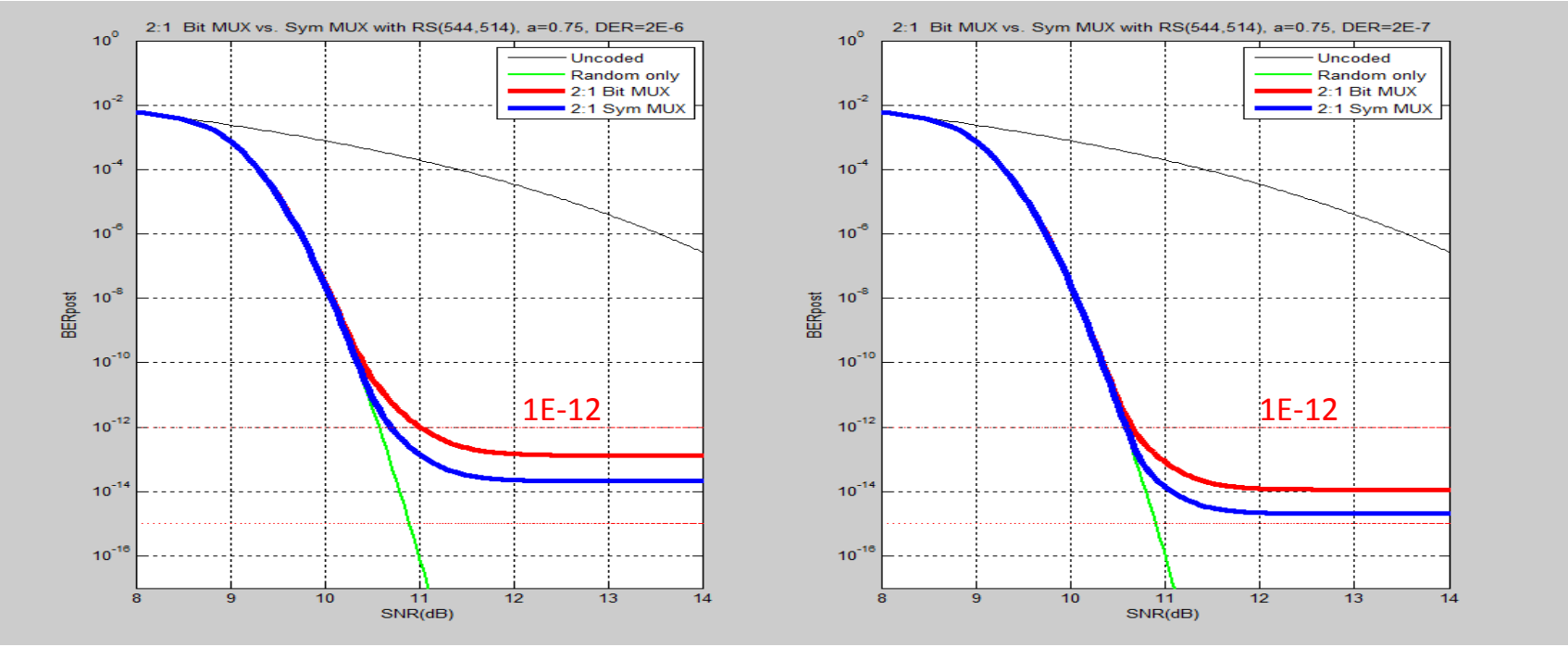
Coding Gain on 50GbE Affected by Error Propagation



a = 0.75 versus a = 0.5

Aim for 1E-12	Electrical DER			Optical DER	
Bit Mux	*a* =0.75	Burst	5E-7	Random	2.4E-4
Symbol Mux		Burst	2E-6	Random	2.4E-4
Bit Mux	*a* =0.5	Burst	4E-6	Random	3E-4
Symbol Mux		Burst	4E-6	Random	3E-4

Coding Gain on 50GbE Affected BER Limitation



- Limiting DER upper bound to meet 1E-12 objective, is less effective than limiting error propagation
- Need to investigate measures to improve BER on C2C/C2M links

Proposal

- Enable 25G class SerDes interface for broader market potential and leave more detailed technical work on specification in task force
- Seeking information on approaches to reduce burst errors and enable 50G IO w/ KP4 FEC
  - Limiting DFE tap coefficient; (not reliable?)
  - Limiting BER upper bound
  - Tradeoff between latency and interleaving
- Further analysis on KR4 FEC to investigate technical feasibility

Thank you