Low-latency Schemes for 50GE

Phil Sun, Credo

Introduction

- In January interim meeting, the importance and possible solutions of 50GE low-latency link have been discussed in multiple presentations:
 - [1] 50G, 100G & 200G SERVER CONNECTIVITY
 - [2] <u>Breakout applications and impacts on objectives for 50/200G Ethernet</u>
 - [3] <u>No-FEC Link for 50GE</u>

- The presentation is to clarify/demonstrate two possible schemes:
 - No-FEC C2M and C2C
 - Lower-latency FEC

No-FEC C2M and C2C

- What does this mean?
 - BER is lower than 1e-12, so no FEC is needed for the whole link.
- What does it look like?
 - With active cables:





• Short-reach chip to chip:



Chip

No-FEC C2M and C2C

- What to be defined?
 - BER target: 1e-12 without FEC.
 - Insertion loss: 6dB to10dB @ 12.89 GHz. The reach needs to meet application needs while easy enough to enable low BER.

• Considerations:

- Very low latency as no FEC is involved!
- FEC Power can be saved.
- Flexibility to add external customized FEC without having KP4 FEC latency penalty.
- Repeaters or active cables are required for copper cable link.
- Impact on current PMD needs to be analyzed.

Lower-latency FEC

- KR4 and KP4 FEC frame latency is more than 100ns. A typical decoder may require another 70ns to100ns decoding latency.
- If FEC latency needs to be less than 100ns [1], a lower-latency FEC is needed.
- RS(272,257,t=7,m=10) may be a good candidate:
 - Same primitive field and generator polynomials as KP4/KR4 FEC.
 - Same clock rate as KP4 FEC.
 - Compatible with transcoding and AM schemes used for KP4 FEC.
 - Most of the logic can be shared with KP4/KR4 FEC.
 - 1 more FEC modes, but manageable.
 - Another candidate that can be easily added is RS(264,257,t=3,m=10). But RS(272,257) performance is much better.

FEC Performance on Electrical Link

- This analysis assumes precoding is used, or error propagation rate can be limited to 0.5 for low-latency channels.
- Latency is a trade off of complexity.

FEC	DER for 1e-12 BER "a"=0.5	DER for 1e-12 BER with precoding	Latency
RS(544,514), KP4	3.1e-4	2.0e-4	198ns
RS(528,514), KR4	1.1e-5	9.0e-6	169ns
RS(272,257), KS4?	2.4e-5	1.8e-5	99ns
RS(264,257)	2.3e-9	5.6e-8	86ns

• In this case, RS(272,257) can tolerate higher than 1e-5 DER (about the same DER target as 802.3bs C2C and 802.3bj KP4) while achieves less than 100ns latency.

FEC Performance on Electrical Link



RS(544, 514), KP4



10⁻⁶

 $\overset{\text{Detector Error Ratio (DER)}}{\text{RS}(264,257)}$

10⁻⁴

10⁻⁸

Credo Semiconductor

02/2016

Conclusions

- Conclusions:
 - There are promising approaches for Low-latency link.
 - No-FEC C2M and C2C
 - Lower latency.
 - Lower-latency FEC
 - Easy to be added.

Thanks!