

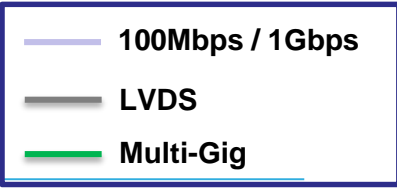
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# Technical Feasibility - EEE for Asymmetry

IEEE 802.3 Greater than 10 Gbps Automotive Electrical  
Ethernet Study Group

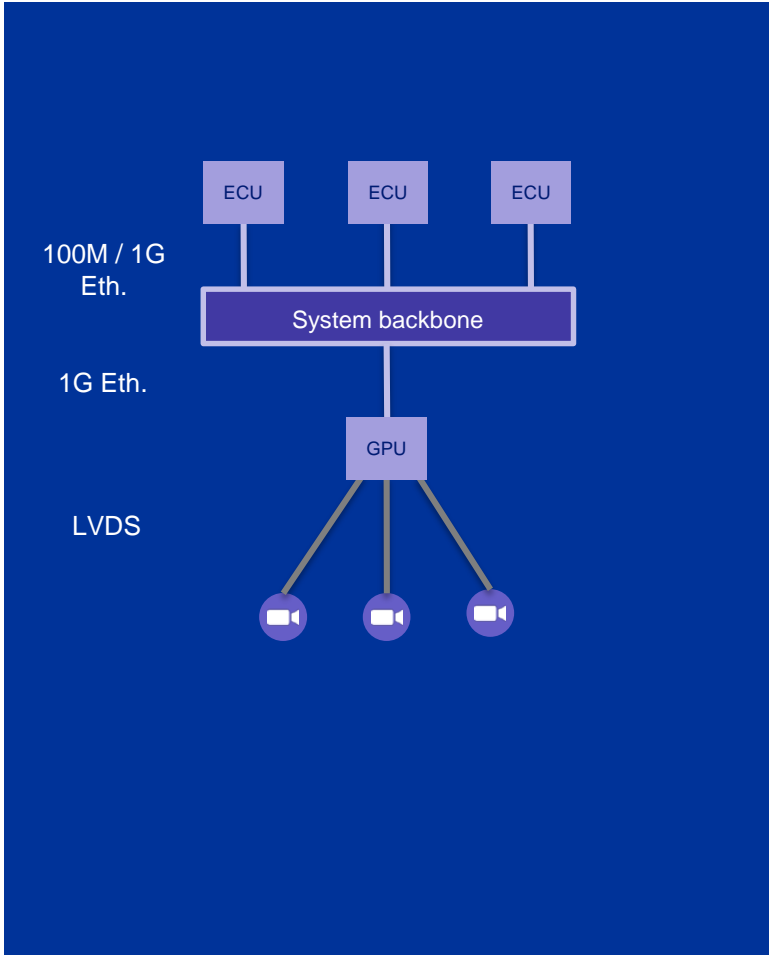
George Zimmerman, CME Consulting, Inc / Marvell

# Automotive Ports Transition to Multi-Gig Ethernet

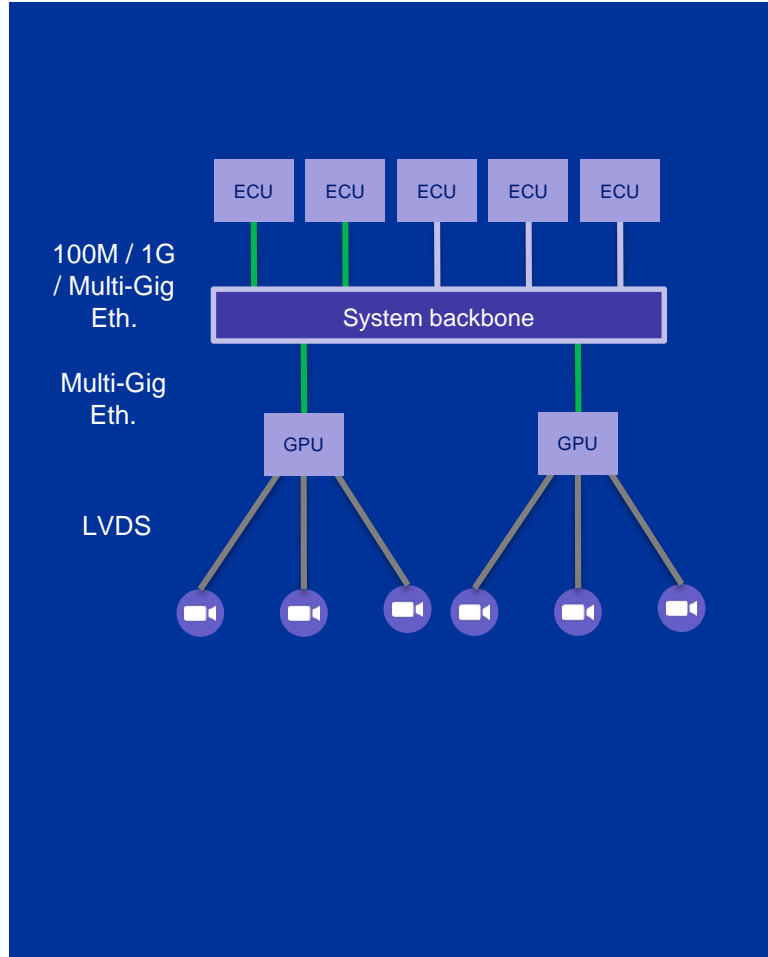


Symmetric Bandwidth

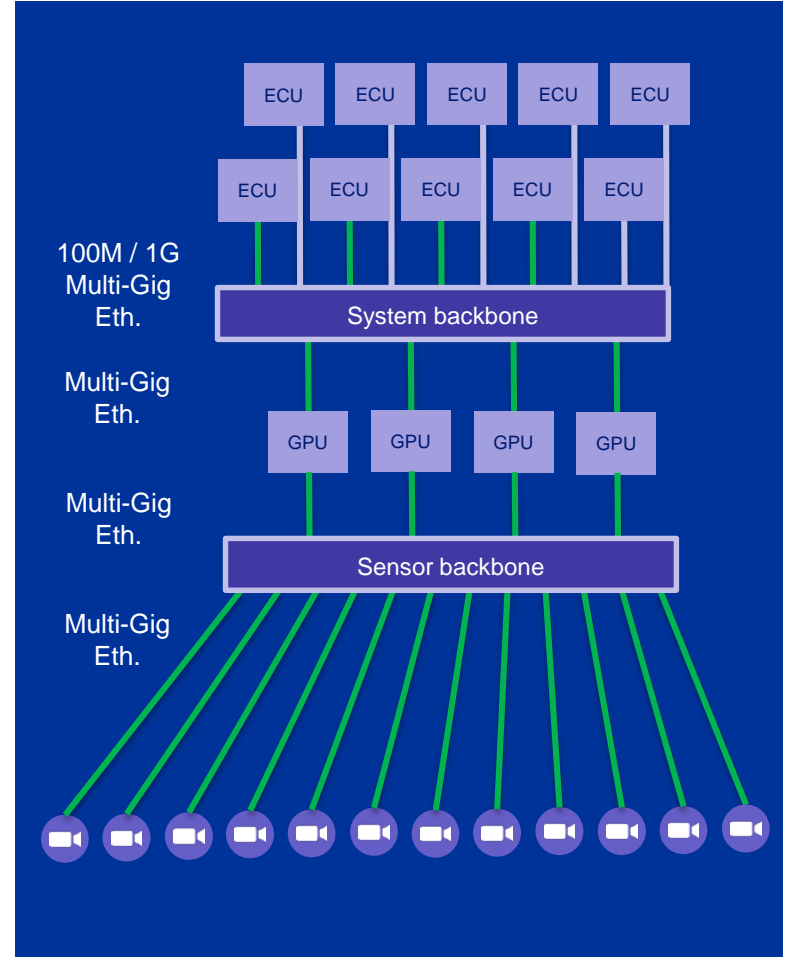
Asymmetric?



2010 - 2018



2019 - 2023



2024 - 2028

# IEEE 802.3 Energy Efficient Ethernet

## Where IEEE 802.3az EEE came from

- Energy Efficient Ethernet (EEE) was introduced in BASE-T PHYs to help computers meet Energy Star power consumption targets
  - Basic idea is to turn the link off as much as possible when there is no traffic, and turn it on as quickly as possible when there is traffic (50 us)
    - State is referred to as Low-power Idle (LPI)
- EEE allows:
  - Up to 90% power savings on a link in LPI state
  - Full flexibility in BW versus power consumption
  - The ability to use a standard MAC/PHY interface, as EEE is also standardized on these interfaces

# How 802.3az EEE Works

- EEE is controlled by the Low Power Idle (LPI) client
  - Allows the MAC & higher layers to go to sleep
  - Physical layer only knows it is in LPI state and is quiet most of the time
- LPI client signals and controls the transition in/out of Low Power Idle state
- Asymmetric Operation: each direction only wakes and sends data as needed

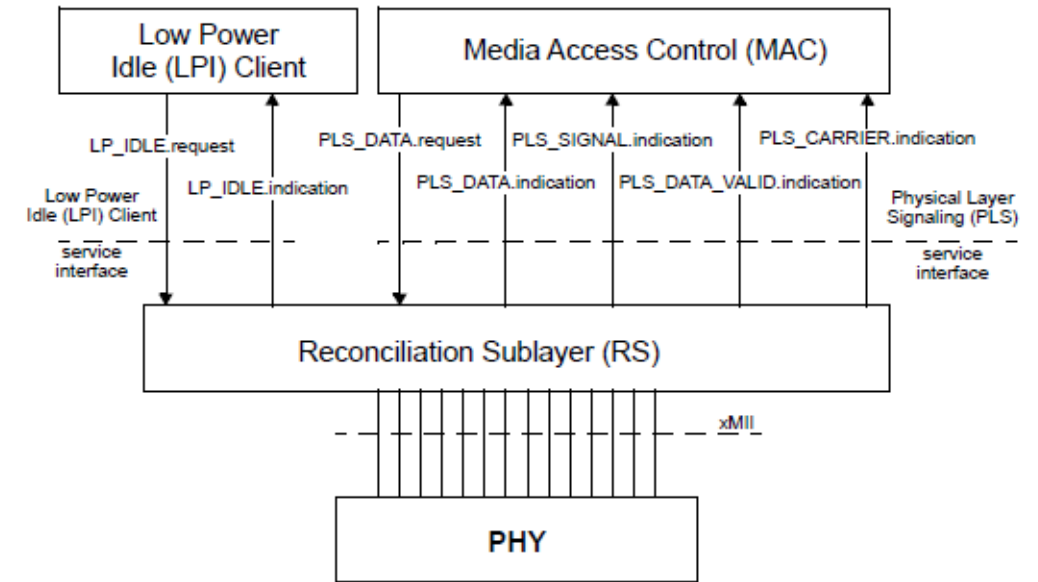
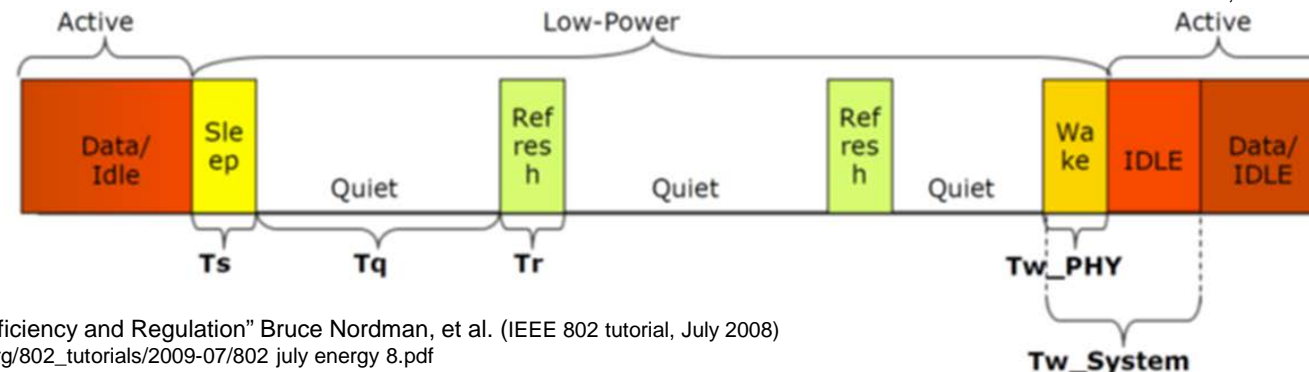


Figure 78-1—LPI Client and RS interlayer service interfaces

Source: IEEE Std. 802.3-2018, IEEE Standard for Ethernet, Clause 78, Energy Efficient Ethernet



Source: "Energy Efficiency and Regulation" Bruce Nordman, et al. (IEEE 802 tutorial, July 2008)  
[http://www.ieee802.org/802\\_tutorials/2009-07/802\\_july\\_energy\\_8.pdf](http://www.ieee802.org/802_tutorials/2009-07/802_july_energy_8.pdf)

# IEEE 802.3az Designed for bursty data – with rapid wake up

- Designed for bursty data and requiring minimal buffering
- Fast, application-transparent recovery
  - “The link status shall not change as a result of the transition”

## Desktop links have low utilization

- Snapshot of a typical **100 Mb** Ethernet link
  - Shows time versus utilization (trace from Portland State Univ.)

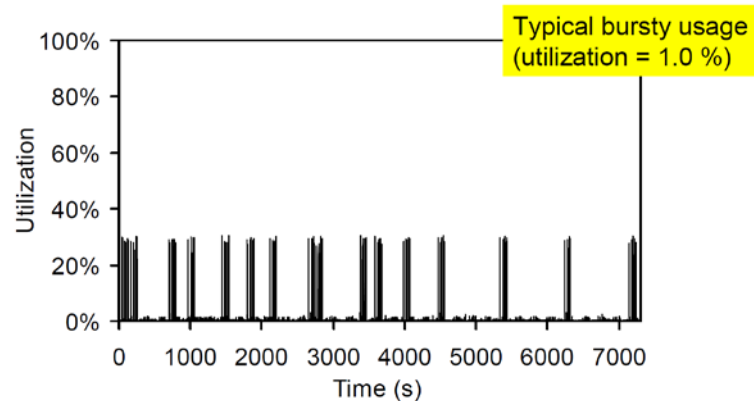


Fig1.xls

July 16, 2007

9

## Transition Time Conclusions

- Applications require sub 10 ms transition time
- Recommend that the EEE TF retain the goal of achieving a transition time of less than or equal to 1 ms

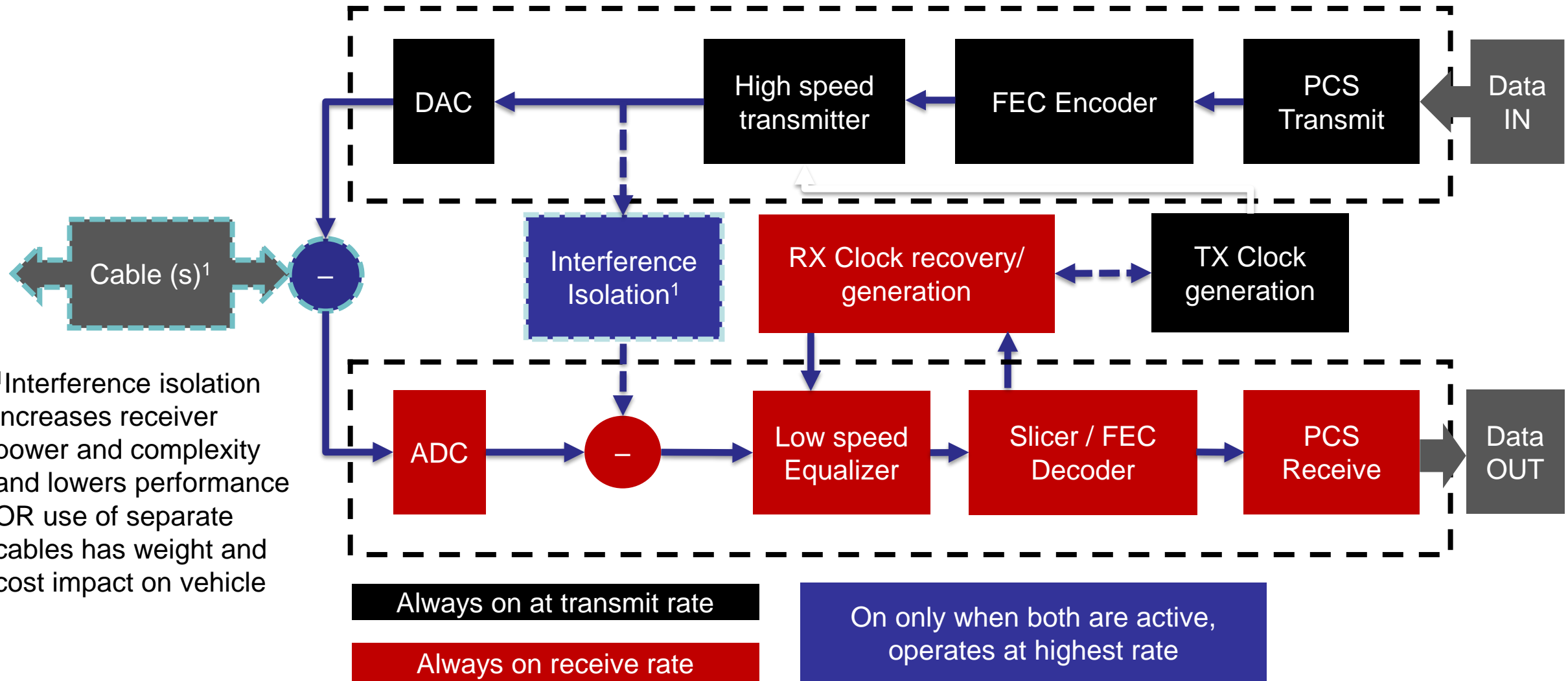
July 16, 2007

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Source: “IEEE 802 Tutorial – Energy Efficient Ethernet”, Hugh Barrass, et al. (IEEE 802 tutorial, July 2007)  
[http://www.ieee802.org/802\\_tutorials/07-July/IEEE-tutorial-energy-efficient-ethernet.pdf](http://www.ieee802.org/802_tutorials/07-July/IEEE-tutorial-energy-efficient-ethernet.pdf)

# Impact of Asymmetry on PHY circuitry

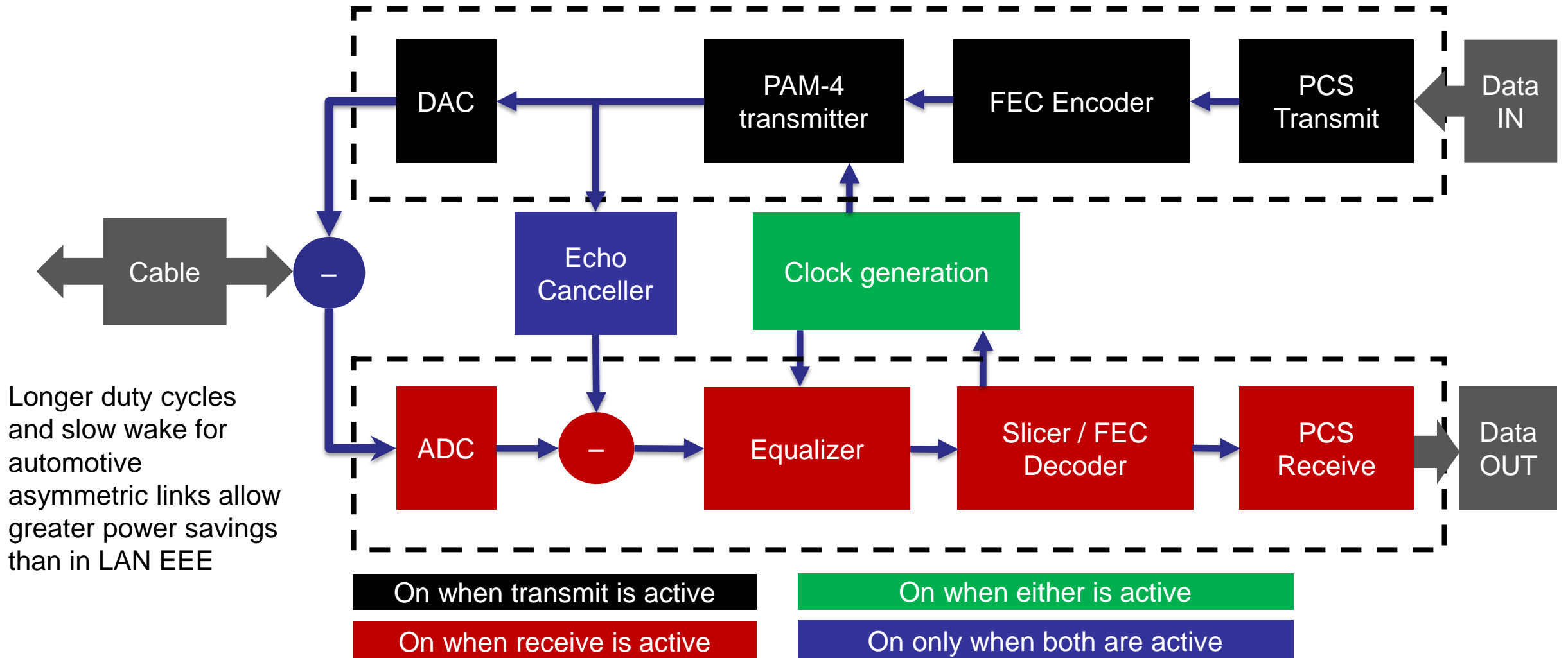
Block Diagram of "Tx" PHY (High speed video transmission PHY)



<sup>1</sup>Interference isolation increases receiver power and complexity and lowers performance OR use of separate cables has weight and cost impact on vehicle

# Asymmetric EEE Operation

Implementation and allowable transition time drives power savings



Longer duty cycles and slow wake for automotive asymmetric links allow greater power savings than in LAN EEE

# Asymmetric Use Model – Are our use cases different?

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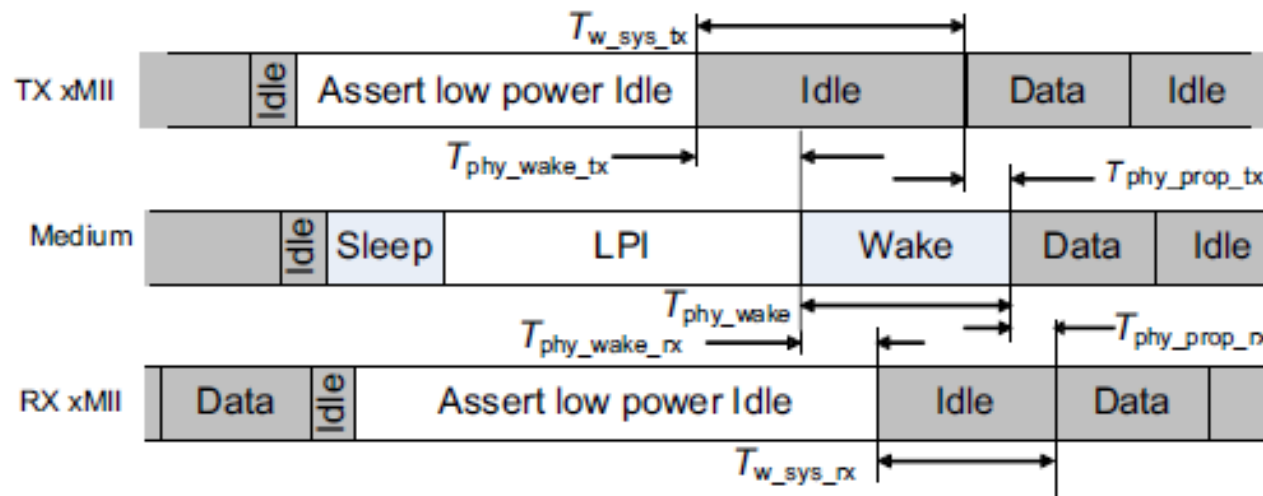
- Startup / maintenance operation
  - May require significant data in the opposite direction
  - Can be scheduled
- Normal operation –
  - High speed – can be unidirectional, can be continuous, requires low (msec) latency
  - Occasional status / control information in the other direction, much less time sensitive
  - Can tolerate slower wake up
- Potentially longer sleep times



# Adjusting EEE parameters for Asymmetric Links

- PHY gets to specify system wake up timing parameters
- While  $T_{w\_phy}$  is a minimum,  $T_{w\_sys\_tx}$  can be set longer, to accommodate longer PHY wake up.

Figure 78-5 illustrates the relationship between the LPI mode timing parameters and the minimum system wake time.



Source: IEEE Std. 802.3-2018, IEEE Standard for Ethernet, Clause 78, Energy Efficient Ethernet

# IEEE Energy Efficient Ethernet: 802.3ch Modifications

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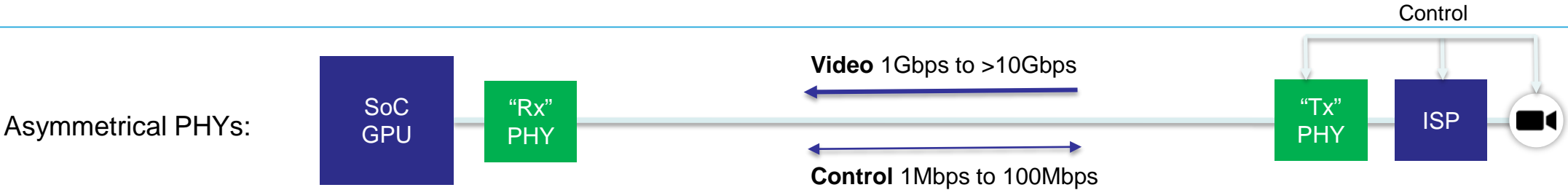
- 802.3ch copied the EEE mechanism from 2.5G – 10GBASE-T PHYs
  - Allows either direction to go in LPI independent of the other direction
- Since 802.3ch implements a hybrid system (which means Tx and Rx are on the same physical copper pairs), it is a strict requirement to keep both ends of the link phase-locked to make the signal processing work
  - This means a link in the LPI state must periodically transmit a burst of data to keep the far-end receiver phase-locked, and the filters converged
- With EEE, a single 802.3ch PHY can be deployed in various system scenarios, effectively supporting all traffic scenarios and scaling the power usage accordingly
  - Versus fixed, non-standard transmission schemes for each scenario

# Potential Extensions for EEE in Automotive

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- A natural extension to the 802.3ch EEE scheme is to introduce a mode to totally shut off transmission when not in use
  - Referred to as “Link Suspension Mode” (useful for slave PHY)
- I2C has been used for control of cameras, where the downstream is continuously transmitting, and the upstream only occasionally (on the order of seconds) transmits a low-speed command
- This extension uses the same “Alert signal”, transmitted at specific known times, and a new Idle character to signal total shut-off of the link
  - It means the camera has to provide the link timing (master) and the far end is phase-locked to it (slave)
    - The result is that when the GPU wants to send an I2C command, it sends an alert, and then the camera’s PHY just has to reconverge the filters and potentially timing phase, allowing a relatively quick wake-up
- Allows close to 100% total power savings in this mode

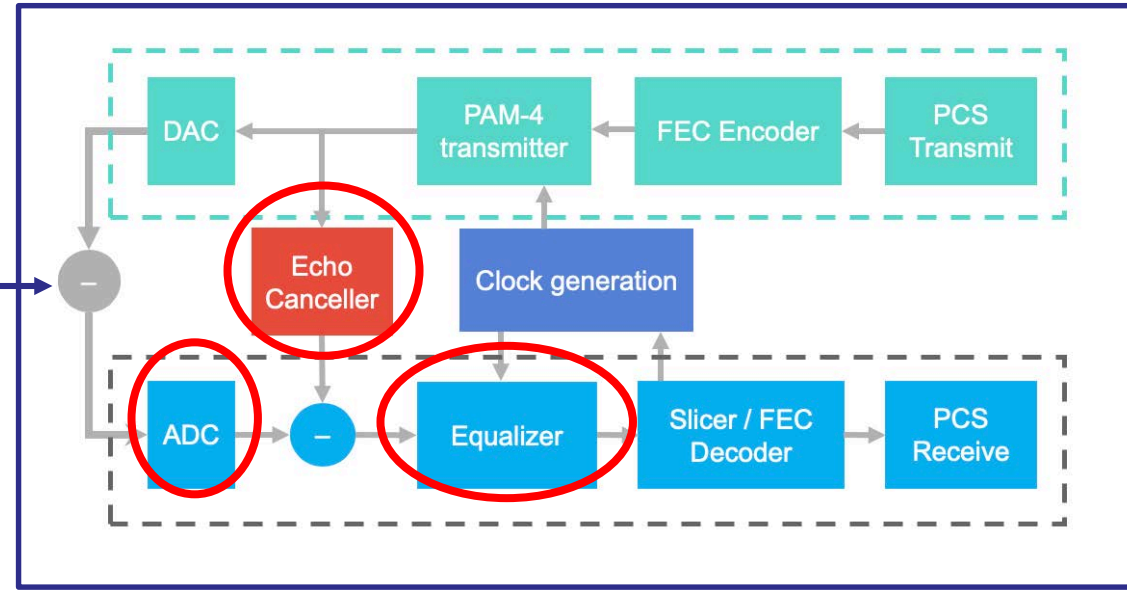
# Impact of Asymmetrical vs Symmetrical PHY Design



For asymmetrical PHY, the circuits and blocks that are not required:

“Tx” PHY (transmits at high speed):  
Echo Canceller, ADC (simplified), Equalizer/Decoder (simplified)

“Rx” PHY (receives at high speed):  
Echo Canceller, DAC/Encoder (simplified)



Save in size :  
“Tx” PHY – about 35%  
“Rx” PHY – about 20%

Typical size of 10Gbps symmetrical PHY is ~2 mm<sup>2</sup>

MINIMAL CHANGES IN DIE AREA:  
“Tx” PHY – about 0.7 mm<sup>2</sup>  
“Rx” PHY – about 0.4 mm<sup>2</sup>

# Summary

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- EEE as envisioned by 802.3az defined ‘instant-on’ recovery
  - Historical BASE-T EEE power savings driven by keep-alive functions and avoidance of long (seconds) of BASE-T training
- EEE for automotive breaks this mold – fast startup, slow wakes allowed
  - Automotive applications could schedule even longer, e.g., link-suspension
- Allowing asymmetry does not substantially impact silicon area or power in modern designs
- Support objective like:
  - Support Energy Efficient Ethernet optimized for automotive applications

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# THANK YOU!

Consensus  
WE BUILD IT.

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