Architectural considerations in support of 100G and 400G 80km DWDM PHYs

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Introduction

- This presentation addresses some architectural considerations in support of the 100G and 400G 80km DWDM PHY objectives

Adopted b10k DWDM PHY Objectives

Adopted Objectives

* - Adopted by SG Jan 2018 Interim. Not approved by IEEE 802.3 WG.
** - Adopted by SG Mar 2018 Plenary. Not approved by IEEE 802.3 WG.
*** - Adopted by SG May 2018 Interim. Not approved by IEEE 802.3WG.
Approved by IEEE 802.3 WG - July 2018 Plenary

- Support full-duplex operation only*
- Preserve the Ethernet frame format utilizing the Ethernet MAC*
- Preserve minimum and maximum FrameSize of current Ethernet standard*
- Provide appropriate support for OTN*

50 Gb/s Ethernet

- Support a MAC data rate of 50 Gb/s*
- Support a BER of better than or equal to 10^-12 at the MAC/PLS service interface (or the frame loss ratio equivalent) for 50 Gb/s*
- Provide a physical layer specification which supports 50 Gb/s operation over at least 40 km of SMF*

100 Gb/s Ethernet

- Support a MAC data rate of 100 Gb/s **
- Support a BER of better than or equal to 10^-12 at the MAC/PLS service interface (or the frame loss ratio equivalent) for 100 Gb/s **
- Provide a physical layer specification supporting 100 Gb/s operation on a single wavelength capable of at least 80 km over a DWDM system. **

200 Gb/s Ethernet

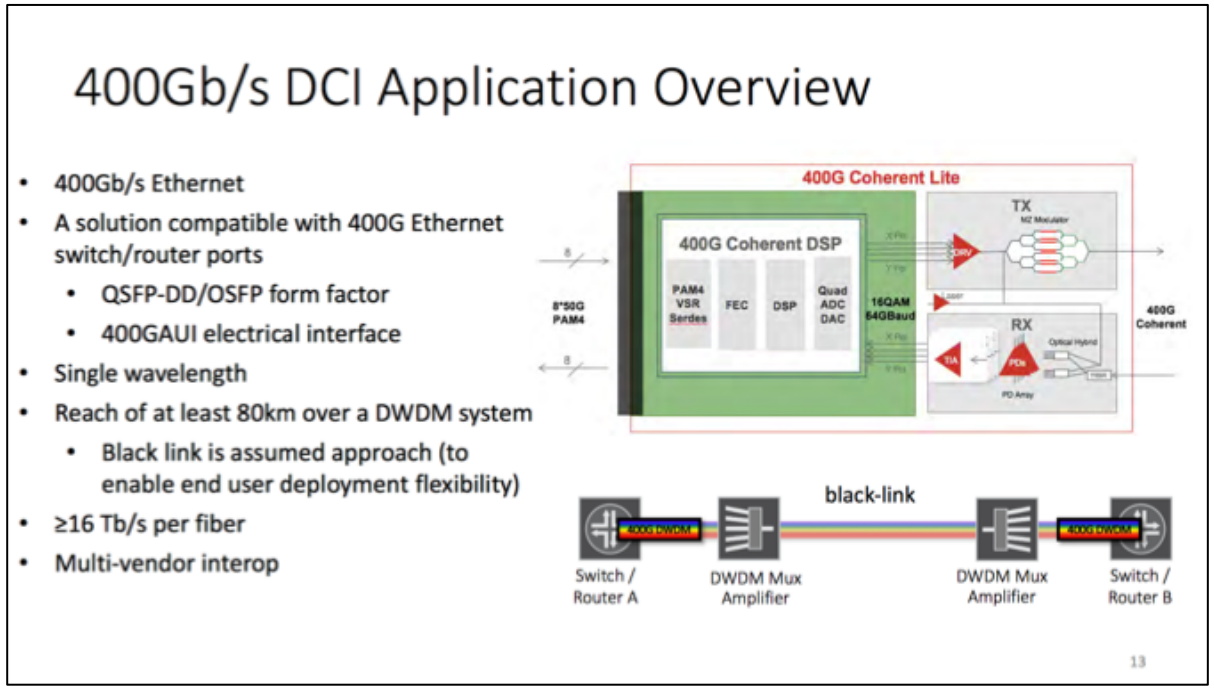
- Support a MAC data rate of 200 Gb/s **
- Support a BER of better than or equal to 10^-13 at the MAC/PLS service interface (or the frame loss ratio equivalent) for 200 Gb/s **
- Provide a physical layer specification supporting 200 Gb/s operation over four wavelengths capable of at least 40 km of SMF**

400 Gb/s Ethernet

- Support a MAC data rate of 400 Gb/s ***
- Support a BER of better than or equal to 10^-13 at the MAC/PLS service interface (or the frame loss ratio equivalent) for 400 Gb/s ***
- Provide a physical layer specification supporting 400 Gb/s operation over eight wavelengths capable of at least 40 km of SMF***
- Provide a physical layer specification supporting 400 Gb/s operation on a single wavelength capable of at least 80 km over a DWDM system.***

www.ieee802.org/3/B10K/project_docs/Objectives_180712

User Case Recap



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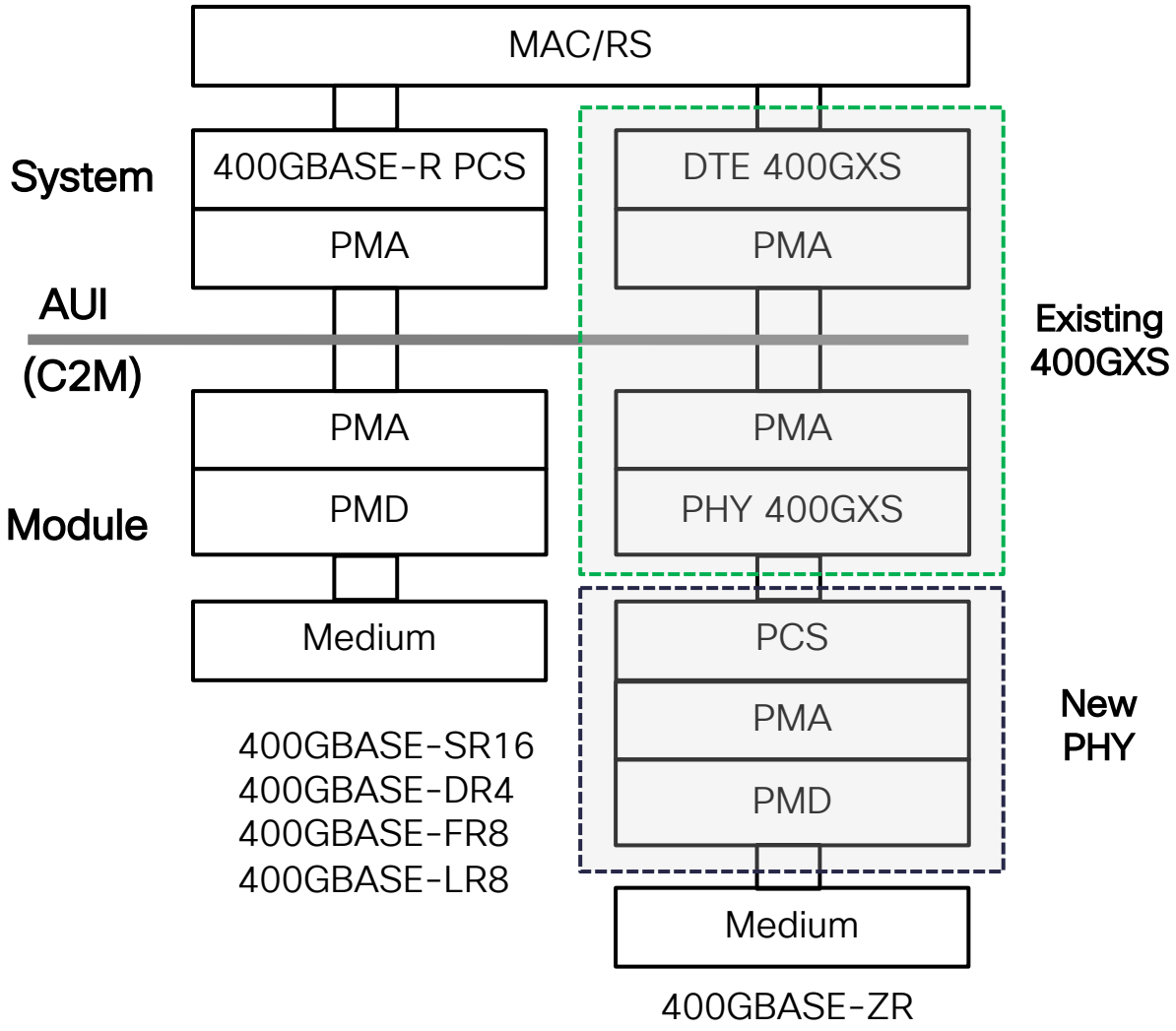
A key requirement is that the solutions are compatible with existing 100G and 400G Ethernet switch/router ports:

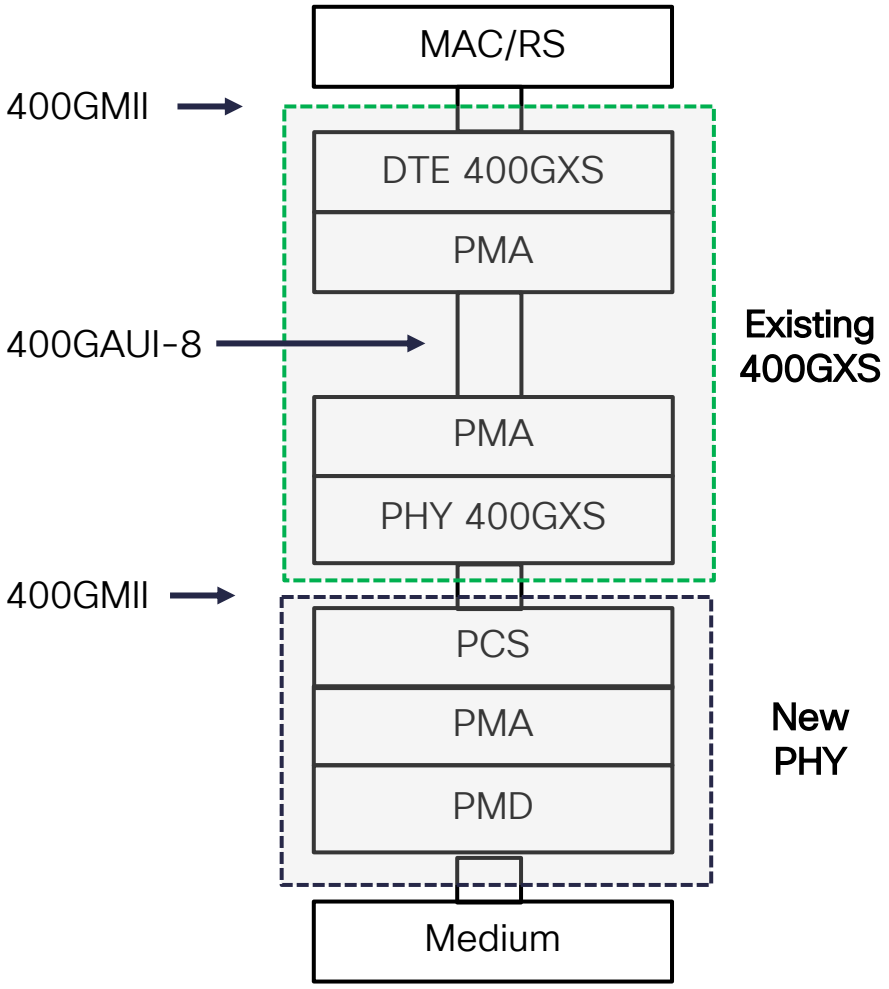
- Interface with existing 100G and 400G C2M AUIs (no new electrical interface development).
- Coexist with current 100G and 400G Ethernet architecture stacks

400G Architecture



- The existing 400GMII Extender (Clause 118) allows the new 400GBASE-ZR PHY to easily interface with current 400G switch ports (and their associated C2M AUI electrical interfaces)
- The 400GBASE-ZR PHY can be defined as any other PHY, in that it contains PCS, PMA and PMD sublayers and interfaces directly to the 400GMII.

400GBASE-ZR PHY Considerations



400GBASE-ZR

- For 400GBASE-ZR the PCS, PMA and PMD sublayers are all specific to a single media interface, and not intended to be (or easily) separable over a physically instantiated electrical interface
  - see Ilya_b10k_01_0918 for more details
- In this respect 400GBASE-ZR is a lot closer to a BASE-T PHY than it is to the existing 400BASE-R PHYs
- In a BASE-T PHY the PCS, PMA and PMD sublayers are typically defined within a single clause (e.g. Clause 55 for 10GBASE-T). Perhaps we should adopt the same approach for 400GBASE-ZR ?

10GBASE-T PHY (Clause 55)

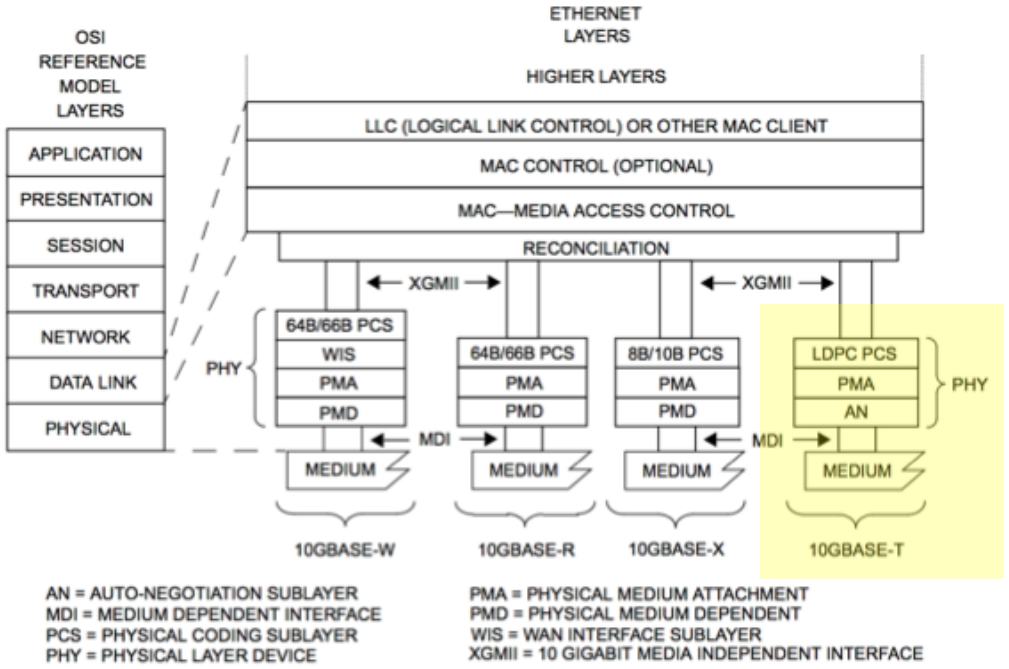


Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause										
	48	49	50	51	52			53	54	55	68
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	Twisted-pair PCS & PMA	1310 nm Serial MMF PMD
10GBASE-SR		M[a]		M	M						
10GBASE-SW		M	M	M	M						
10GBASE-LX4	M							M			
10GBASE-CX4	M								M		
10GBASE-LR		M		M		M					
10GBASE-LW		M	M	M		M					
10GBASE-ER		M		M			M				
10GBASE-EW		M	M	M			M				
10GBASE-T										M	
10GBASE-LRM		M		M							M

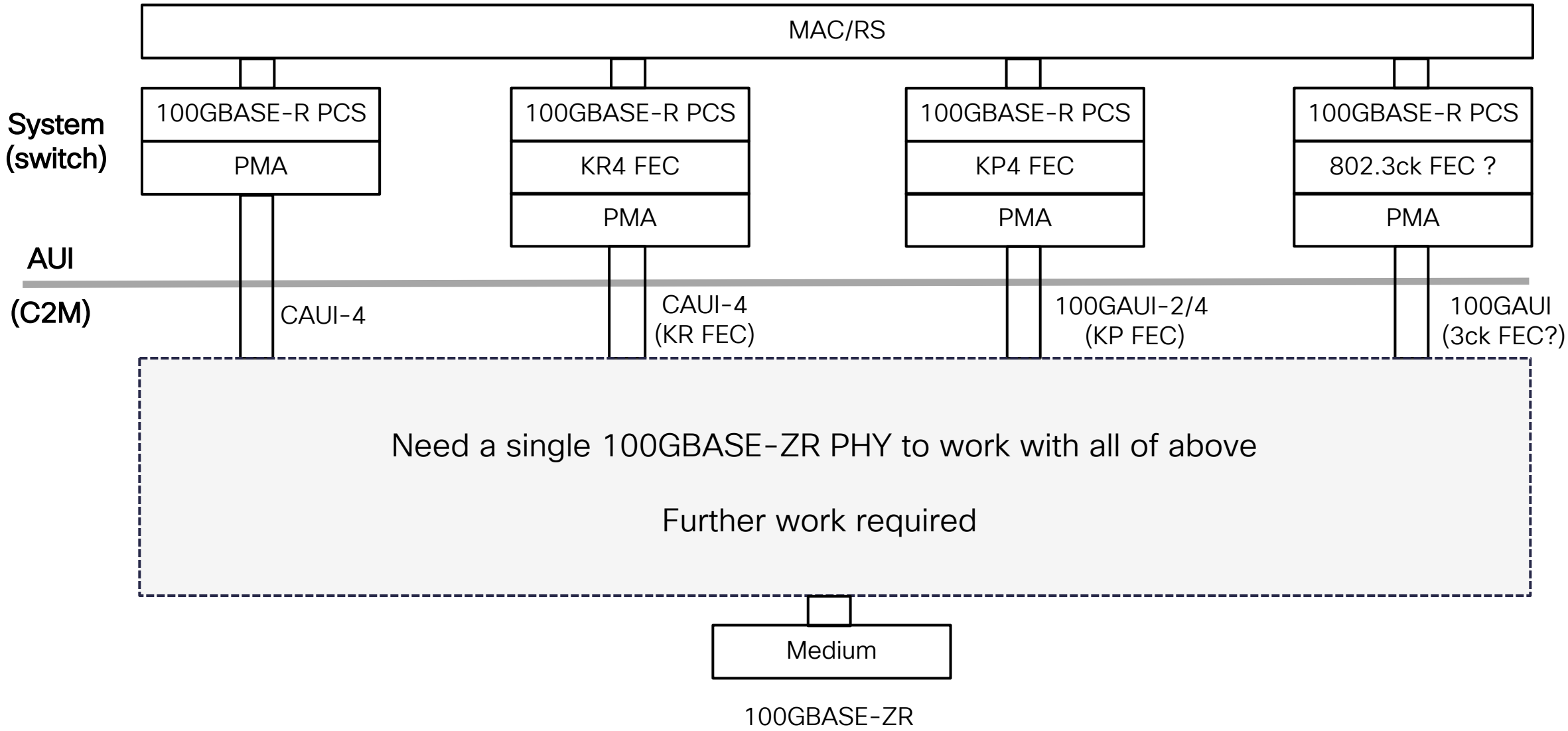
[a]M = Mandatory

10GBASE-T: Only a single entry in Clause table

100G Architecture

- The situation at 100G is somewhat more complicated than it is for 400G
- There is no existing 100GMII Extender to leverage
- The PCS and FEC are implemented as separate sub-layers
- There are at least three different C2M AUIs to interface to:
  - CAUI-4 (no FEC)
  - CAUI-4 (KR4 FEC)
  - 100GAUI-2 (KP4 FEC)

100G Architecture



Summary

- Need to interface with common use 100G and 400G C2M AUIs
- For 400G, the solution is fairly straightforward
  - Leverage the existing 400GMII Extender (Clause 118) and define a new 400GBASE-ZR PHY (PCS+PMA+PMD)
  - The main question is whether the new PCS, PMA and PMD sublayers should be defined as separate clauses or within a single clause (like BASE-T)
- For 100G, more work is required