1000BASE-RH Packet Jitter Analysis

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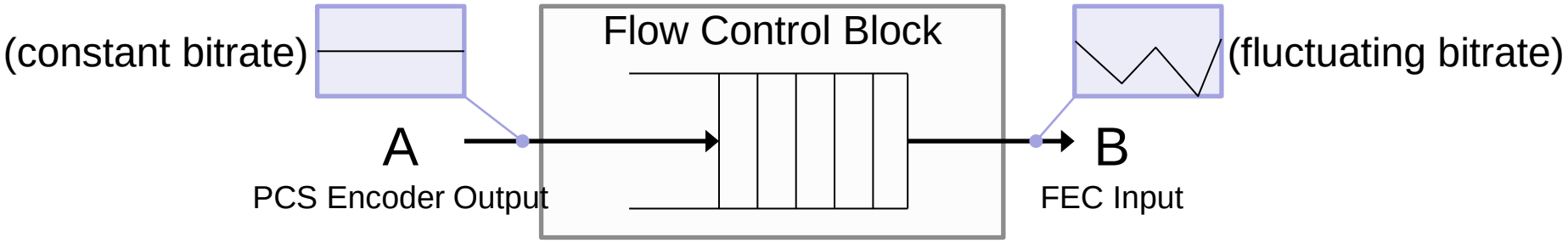
Background and Objectives

- In 802.3bv TF Interim meeting of January 2015 and Plenary meeting of March 2015 several parts of the baseline were adopted:
  - PCS encoding proposed in [1].
  - FEC and modulation schemes proposed in [2].
  - Transmission scheme defined in [3].
- In [1] it is analyzed the packet jitter introduced by the PCS encoding. In that presentation the jitter analysis assumes that there is a flow control block that guarantees a constant bit rate at the output of the PCS encoder. Therefore there is no packet jitter.
- In this presentation the jitter is analyzed in more detail, and the flow control mechanism is compared for three different systems:
  - Modulation scheme adopted in 1000BASE-RH TF.
  - 10GBase-T.
  - Modulation scheme adopted in 1000BASE-T1 TF.

Flow Control Block

- In 1000BASE-RH transmitter, the average bit rate at the input interface of the MLCC encoder exactly matches the average bit rate at the output of the PCS encoder.
- If not compensated by flow control, the MLCC encoder does not work with a constant bit-rate due to the presence of a BCH encoder, and also by the insertion of the S1/S2/PHS ([2] and [3]).
  - In this situation, the non-constant bit rate would be transformed directly in packet-to-packet jitter.
- However the transformation of a non-constant bitrate into a constant bit-rate is easily solved inserting a flow control block, with an internal buffer to implement the compensation. As the input and output rates on the block are identical there is no risk of buffer under or overflow.
  - The flow control mechanism was already proposed and adopted for 1000BASE-RH in [1] and [2].
- The flow control block completely hides the rate fluctuations to the PCS Encoder, and as a result eliminates the source of jitter. Although not part of this presentation, the same concepts apply to the receiver.
- The flow control block is depicted in the following figure.



Flow Control Block II

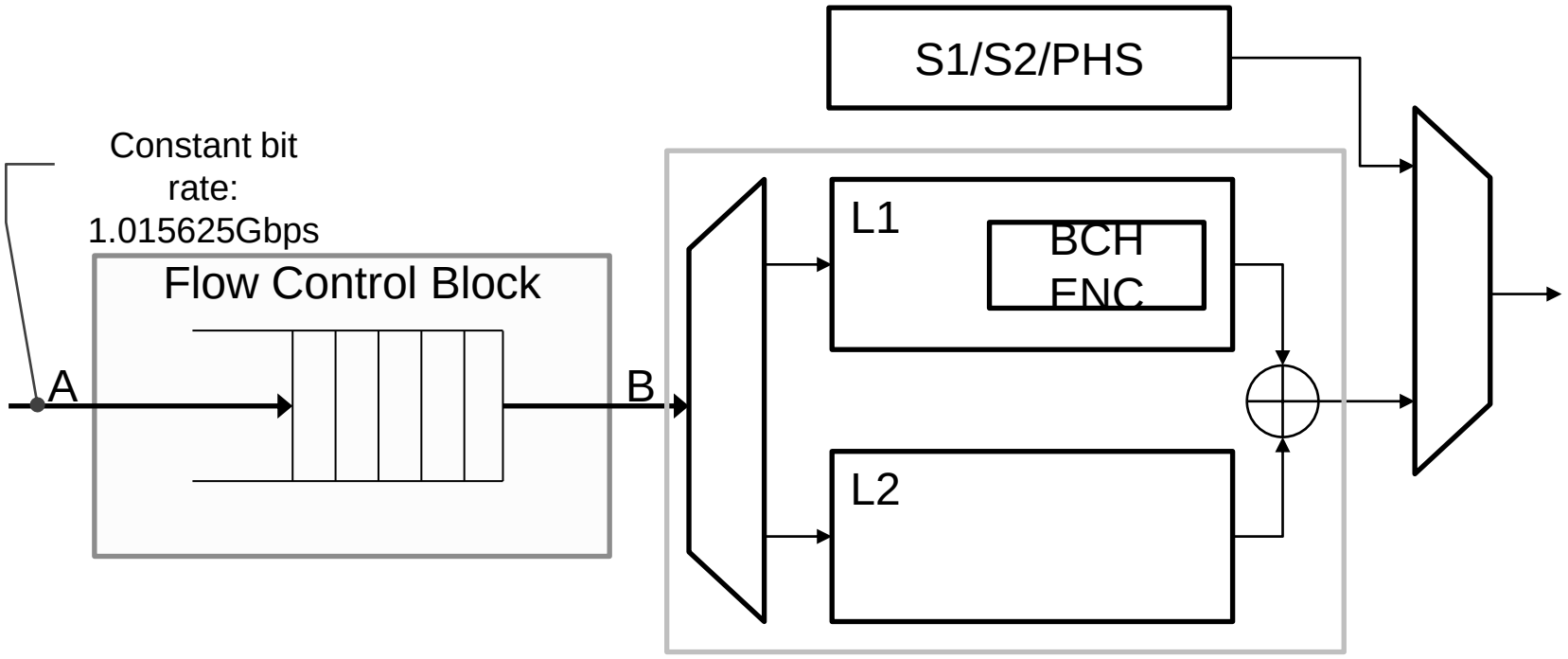
- As presented in [1], in 1000BASE-RH the PCS Encoder encodes the GMII information in blocks of 8 bytes, and encodes all the information present at the GMII interface (so data from the Ethernet packets and data present during IPG). It adds an extra type bit as part of the PCS Encoding process. As a result the same flow control analysis might be applied on this block. This analysis is not performed because the PCS encoder needs to buffer a whole block of 8 GMII bytes to be able to perform the encoding, which renders unnecessary any extra flow control mechanism.
- In 1000Base-RH there is no alignment between the PCS Encoding boundaries and the FEC code words. However this has no impact on the jitter analysis:
  - The flow control block guarantees a constant bit rate.
  - The constant bit rate between the PCS Encoder and FEC isolates the structure of the FEC code words from the structure of the PCS Encoding blocks.
- Due to the constant bitrate at the output of the PCS Encoder, there is no jitter introduced in the system except in the interfacing between GMII interface and the transmitter/receiver, and this happens only when they are not synchronous due to the need to perform clock domain crossing and IPG stretching. However the jitter introduced due to this is minimal (about 2-4 GMII clock cycles). This source of jitter is not specific to 1000Base-RH and also exists in the other systems analyzed in this presentation.

System Analysis

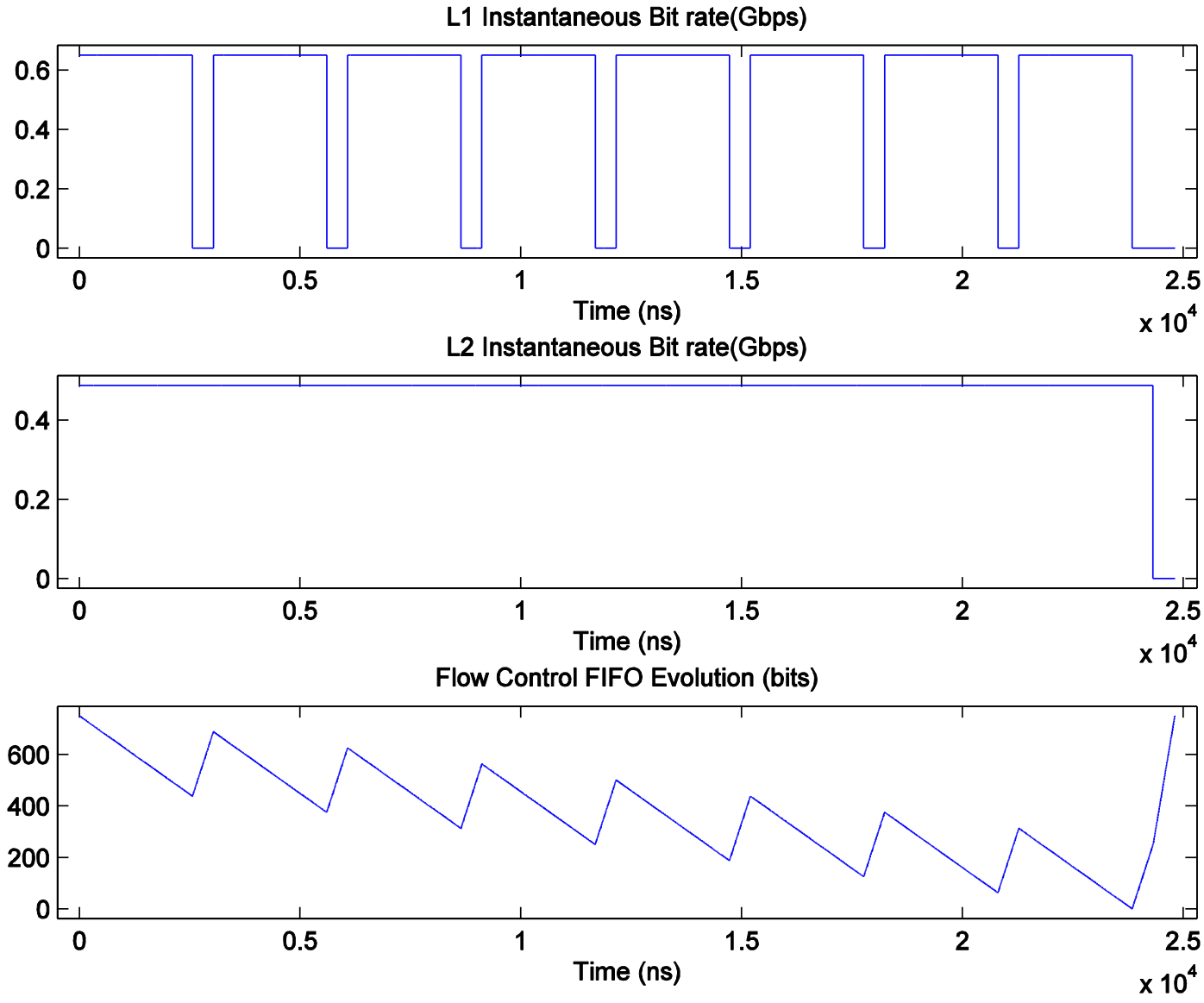
- To keep the presentation as simple as possible this presentation only focus in the transmitter structure. At the same time, only the blocks relevant to the jitter topic will be shown.
- For each system a single flow control block has been inserted at the boundaries of mayor blocks for simplicity. It does not imply that the flow control block physically exists or is described in the relevant documents at the same location.
  - For example, in [2] the flow control is shown as two independent FIFO's for L1 and L2.
- For each system in the comparison an analysis of the instantaneous bit rates at the output of the flow control block have been performed. For all of them the instantaneous bit rate at the output of the flow control block is periodic, so the analysis has been performed for a complete period.
- It will also be shown the evolution of the number of buffered bits in the FIFO along time. This evolution is also periodic, so the analysis is also performed for a single period.
- Each of the systems analyzed has a different symbol rate, and, at the FEC level, each of them works at a different bitrate:
  - 1.015625 Gbps in the case of 1000-BASE-RH
  - 1.0125 Gbps in the case of 1000-BASE-T1
  - 10.15625 Gbps in the case of 10GBASE-T
- To show the results in a uniform manner the instantaneous bit rate, and the evolution of the buffering inside the flow control block are shown versus time, measured in ns.

1000BASE-RH

- The figure in this slide show the simplified transmitter structure used in the analysis.
- In the next slide the instantaneous bit rate at L1 input, the instantaneous bit rate at L2 input and the evolution of the number of bits in the flow control block buffer are shown.

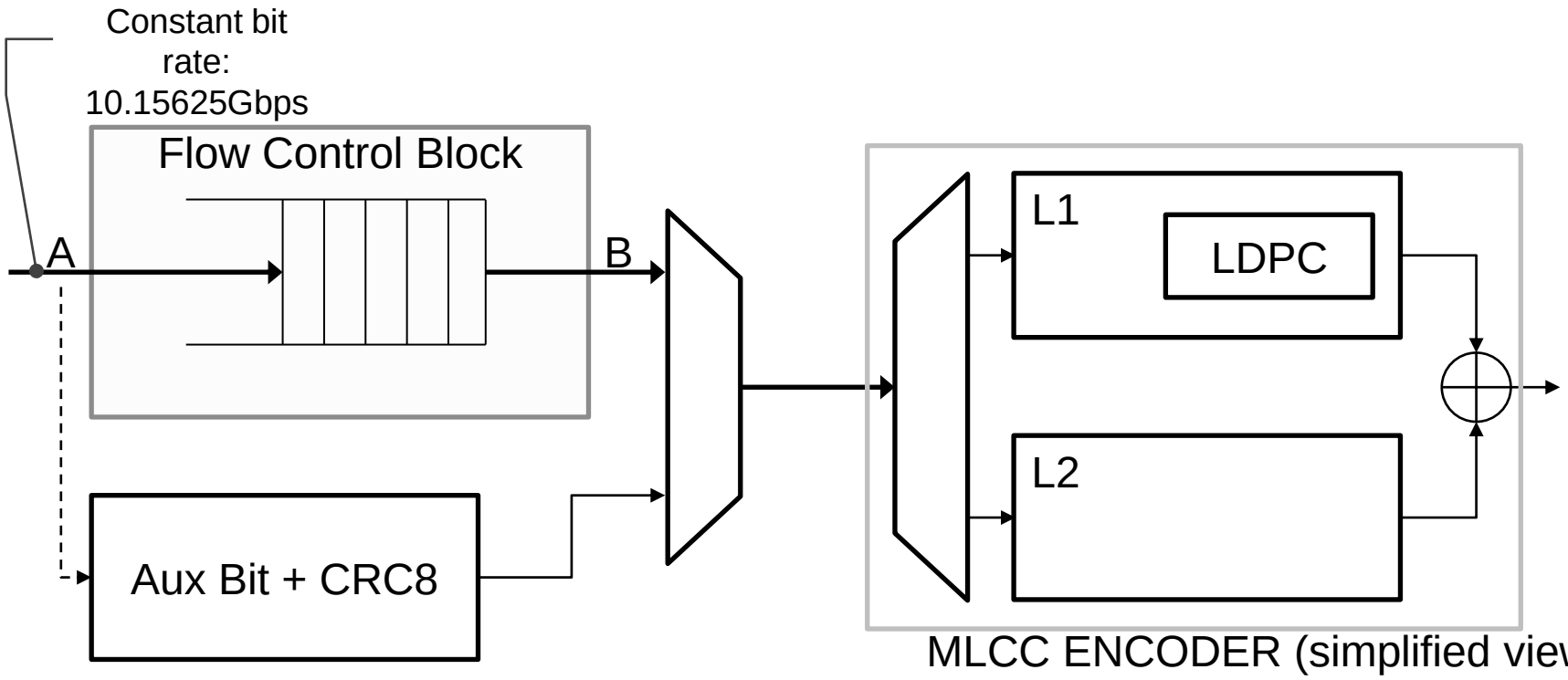


1000BASE-RH II

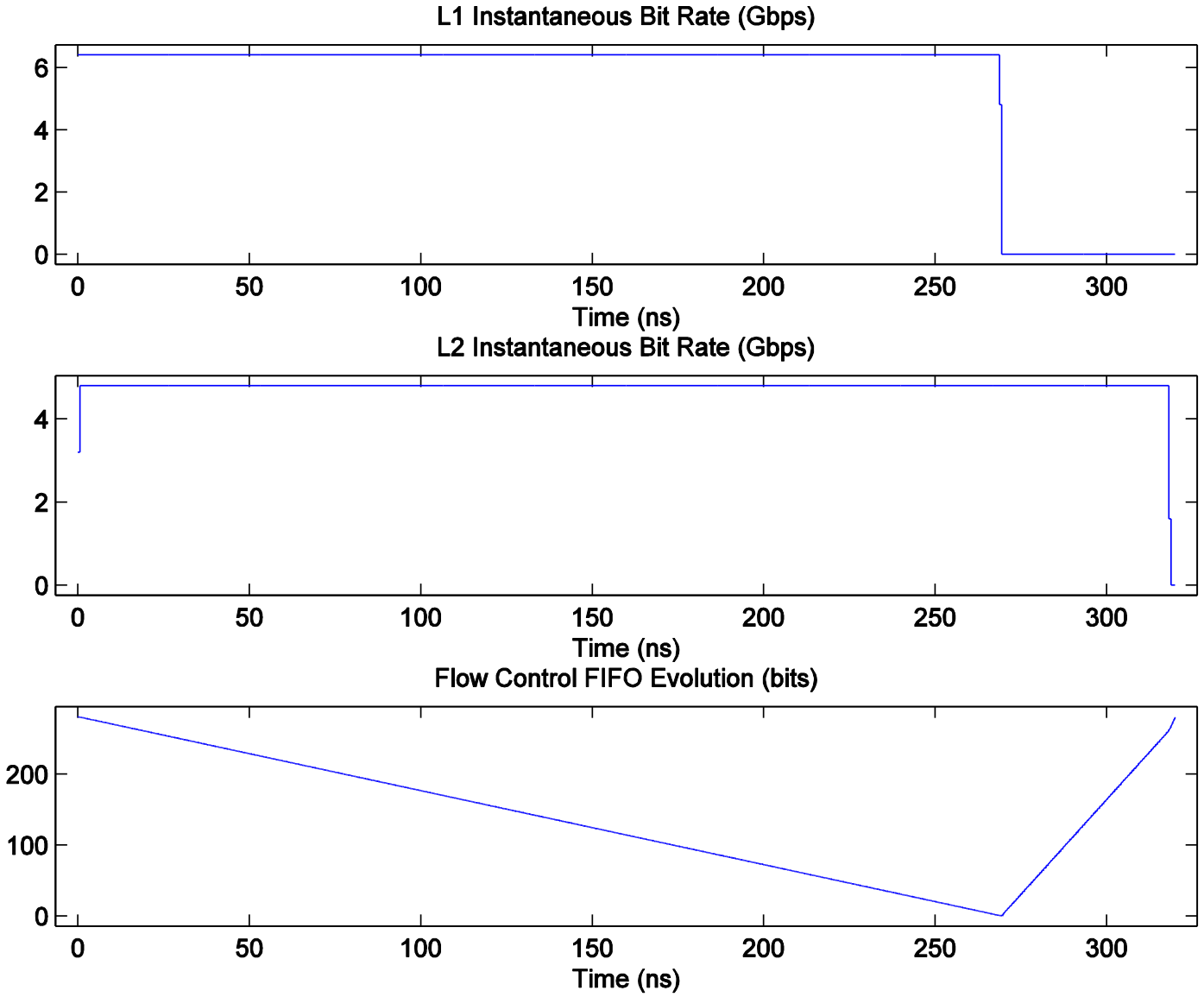


10GBASE-T

- The figure in this slide show the simplified transmitter structure used in the analysis.
- In the next slide the instantaneous bit rate at L1 input, the instantaneous bit rate at L2 input and the evolution of the number of bits in the flow control block buffer are shown.

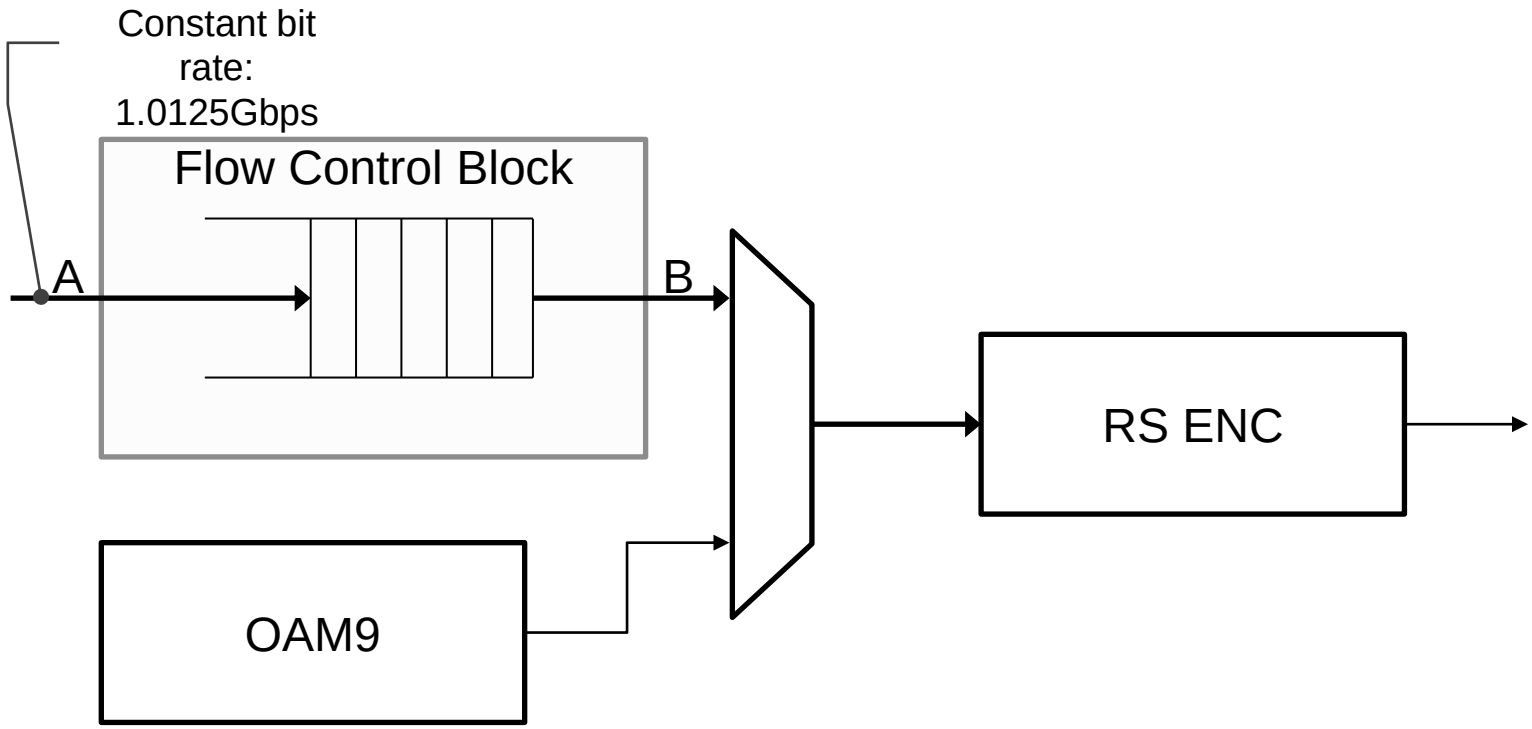


10GBASE-T II

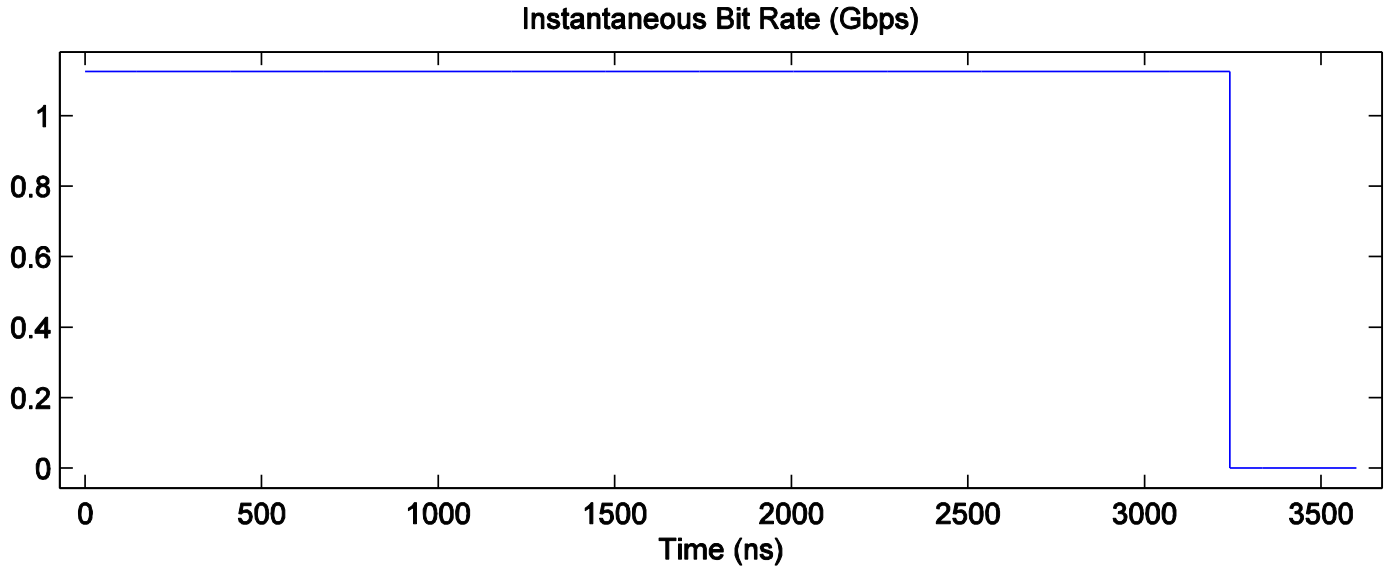

L1 Instantaneous Bit Rate (Gbps)
6
4
2
0
0
50
100
150
200
250
300
Time (ns)
L2 Instantaneous Bit Rate (Gbps)
4
2
0
0
50
100
150
200
250
300
Time (ns)
Flow Control FIFO Evolution (bits)
200
100
0
0
50
100
150
200
250
300
Time (ns)

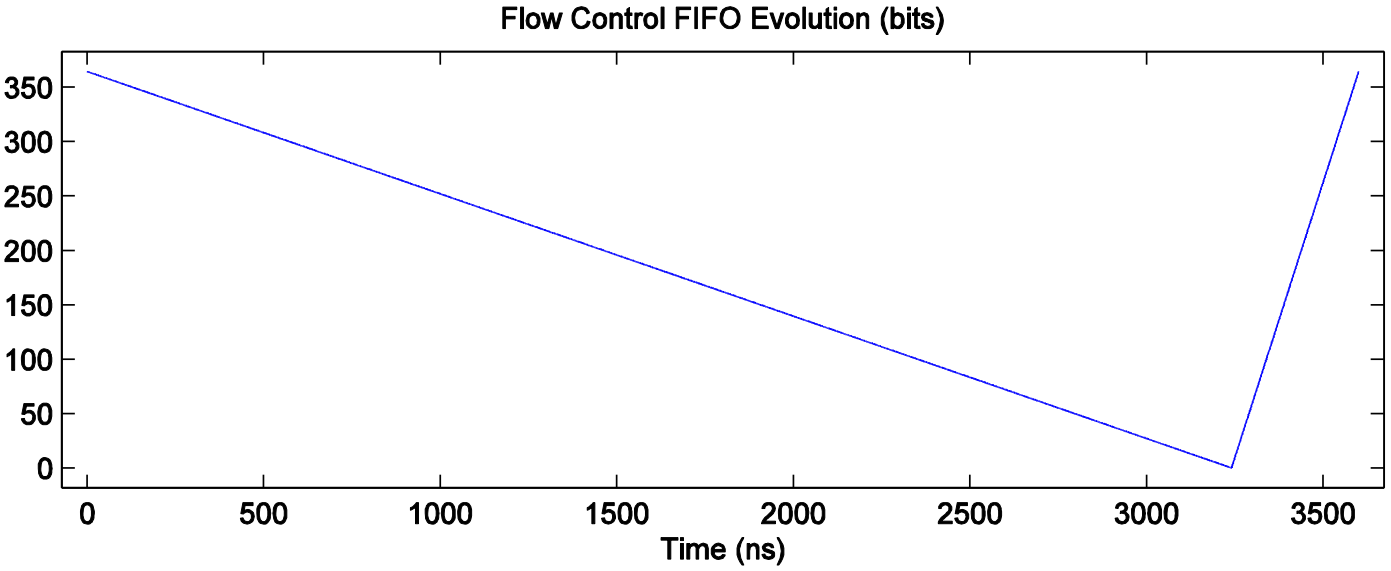
1000BASE-T1

- The figure in this slide show the simplified transmitter structure used in the analysis.
- In the next slide the instantaneous bit rate at B, and the evolution of the number of bits in the flow control block buffer are shown.



1000BASE-T1 II





Conclusions

- This presentation demonstrates that the baseline adopted for 1000BASE-RH does not present packet jitter.
- The jitter that might be generated due to the FEC block coding is easily solved by the inclusion of a flow control block at the boundary between the PCS Encoder and the FEC.
  - The presence of the flow control block was already proposed and adopted in [1] and [2].
- The problem is not specific to 1000BASE-RH, and happens in all the systems that implement block codes, for example in 1000BASE-T1 and 10GBASE-T.
- In 1000BASE-RH there is no alignment between PCS blocks and FEC code words, but as it has been demonstrated this causes no problems.
- The only jitter source in 1000BASE-RH happens when the Transmitter/Receiver are not synchronous to the GMII interface and it is necessary to perform clock-domain crossing and IPG stretching.
  - This is not specific to 1000BASE-RH, and also happens in 10GBASE-T and 1000BASE-T1.

References

- [1] *David Ortiz, et al., "64B/65B PCS encoding for GEPOF", IEEE 802.3bv TF, Plenary Meeting, March 2015.*
- [2] *Rubén Pérez-Aranda, et al., "High spectrally efficient coded 16-PAM scheme for GEPOF based on MLCC and BCH", IEEE 802.3bv TF, Interim Meeting, January 2014*
- [3] *Rubén Pérez-Aranda, "Transmission scheme for GEPOF", IEEE 802.3bv TF, Interim Meeting, January 2014*