Symbol Rate Selection for 40GBASE-T

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January 22, 2013

Supporters

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Introduction

- In `http://www.ieee802.org/3/NGBASET/public/sep12/bliss_01a_0912.pdf` a power reach analysis was done for 40GBASE-T.
- The goal here is to extend this analysis towards the goal of finding the optimum symbol rate and modulation format.
- In this presentation we will focus on symbol rate optimization for the analog front ends. The equally important digital power impacts will be addressed in a future presentation.

Cable

- The measurements results of the Cat 8 cable presented in `http://www.ieee802.org/3/NGBASET/public/nov12/larsen_01a_1112_ngbt.pdf` are used in this analysis.
- Our results are based on the insertion loss of the pair (45).
- Scaling responses by cable length is achieved by this transformation: $f_1 L_1 \rightarrow f_2 L_2$.

Insertion Loss of the Cable

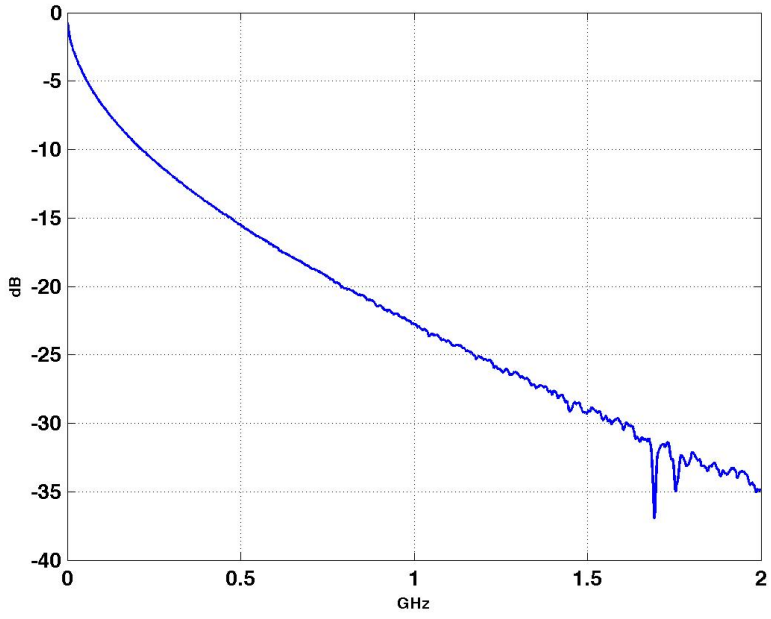

Figure: Insertion Loss of the 40m Cat 8 Cable

- The 40m cable is showing only 35 dB loss at 2 GHz.
- Even at $f_s = 4$GBd symbol rate, the $f_s/2$-loss is significantly less than the corresponding $f_s/2$-loss for a Cat 6A 100m cable at $f_s = 0.8$GBd.

Gap to Capacity and Link Margin

- The gap to capacity of a PAMn constellation is almost independent of the constellation size.
- Using a proper coded modulation scheme, the gap to capacity is predominately a function of the binary performance of the code.
- In this analysis we assume a fixed gap to capacity independent of the symbol rate and dictated by the choice of the FEC.
- In additional to the gap to capacity, we assume a certain operational margin for reliable performance.

Table: Margin Assumptions

Gap to Capacity (dB)	4
Operating Margin(dB)	3

Operating SNR and Symbol Rate

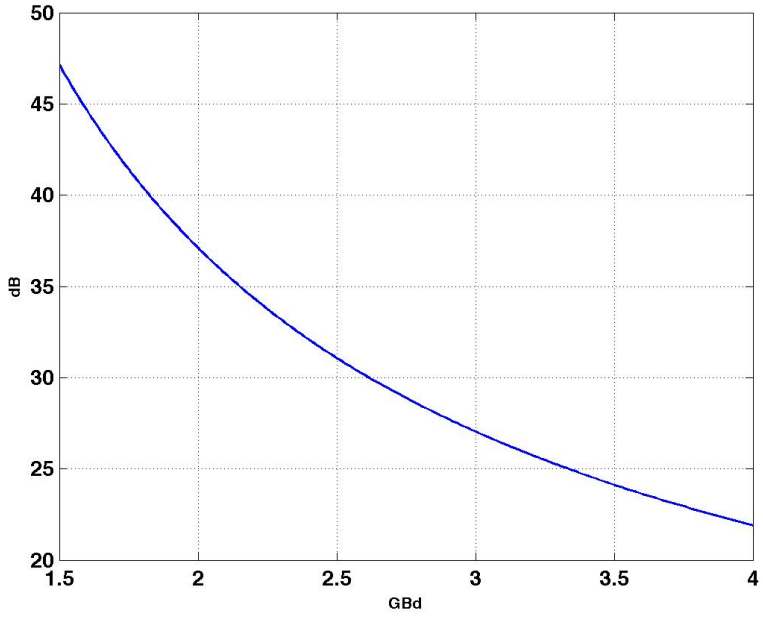

Figure: The Required SNR vs Symbol Rate for the 40m Cable

Combining the gap to capacity and the link margin in one variable, g, the required SNR is computed as:

$$\mathrm{SNR}\,(f_s) = g\,(2^{\frac{2R}{f_s}} - 1) \gtrapprox\ g\,2^{\frac{2R}{f_s}}$$

Analog Gain

In order to estimate the required front end performance we need to calculate the amount of the gain that we can apply at the receiver front end.

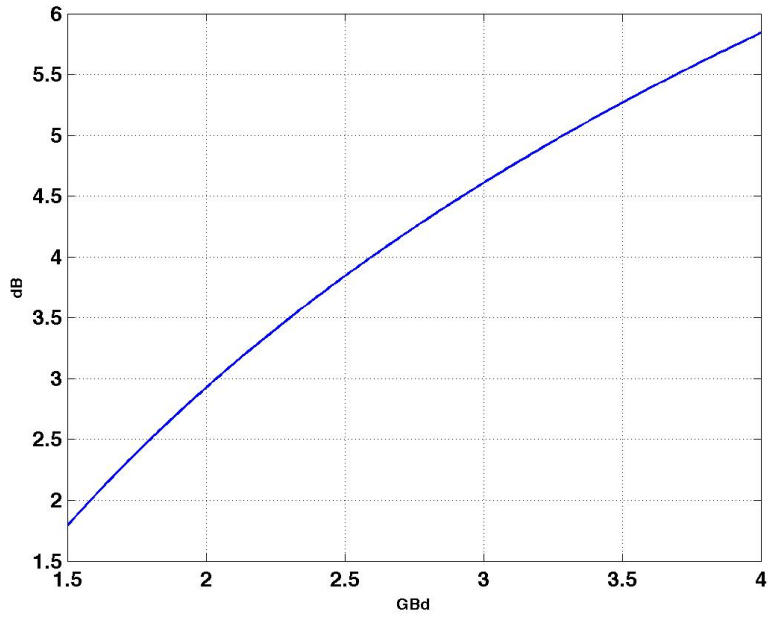

Figure: The Analog Gain vs Symbol Rate for the 40m Cat 8 Cable and 13 dB ADC Back Off.

Digital Noise Enhancement

In order to link the AFE performance with the link margin at the slicer input we need to calculate the required gain of the digital equalizer:

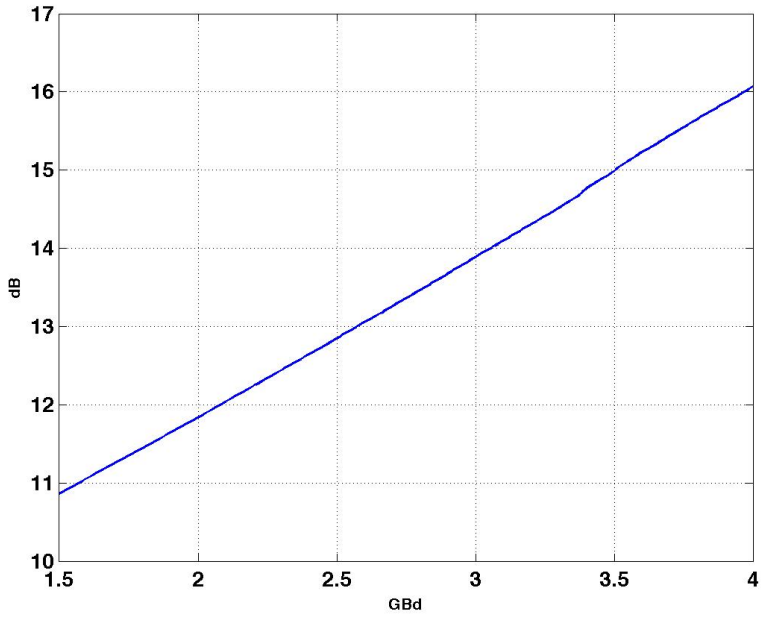

Figure: The Digital Gain vs Symbol Rate for the 40m Cat 8 Cable and 13 dB ADC Back Off.

Residue Nonlinear Echo

- In a full duplex system only the linear component (with respect to the transmit signal) of the echo is cancelled by the DSP.
- The nonlinear component of the transmit signal is not cancelled by the linear echo canceler.
- In CMOS, improvements in technology and design techniques play more important roles than the allocated power in reducing the nonlinear echo.
- The scaling rule for the power of the nonlinear echo $\gamma(f_s)$ measured in dB's with respect to the transmit level is:

$$\gamma(f_s) = \begin{cases} \gamma_0 & \text{if } f_s < f_0 \\ \gamma_0 - 20\log_{10}(\frac{f_s}{f_0}) & \text{if } f_s \geq f_0 \end{cases}$$

Residue Nonlinear Echo vs Symbol Rate

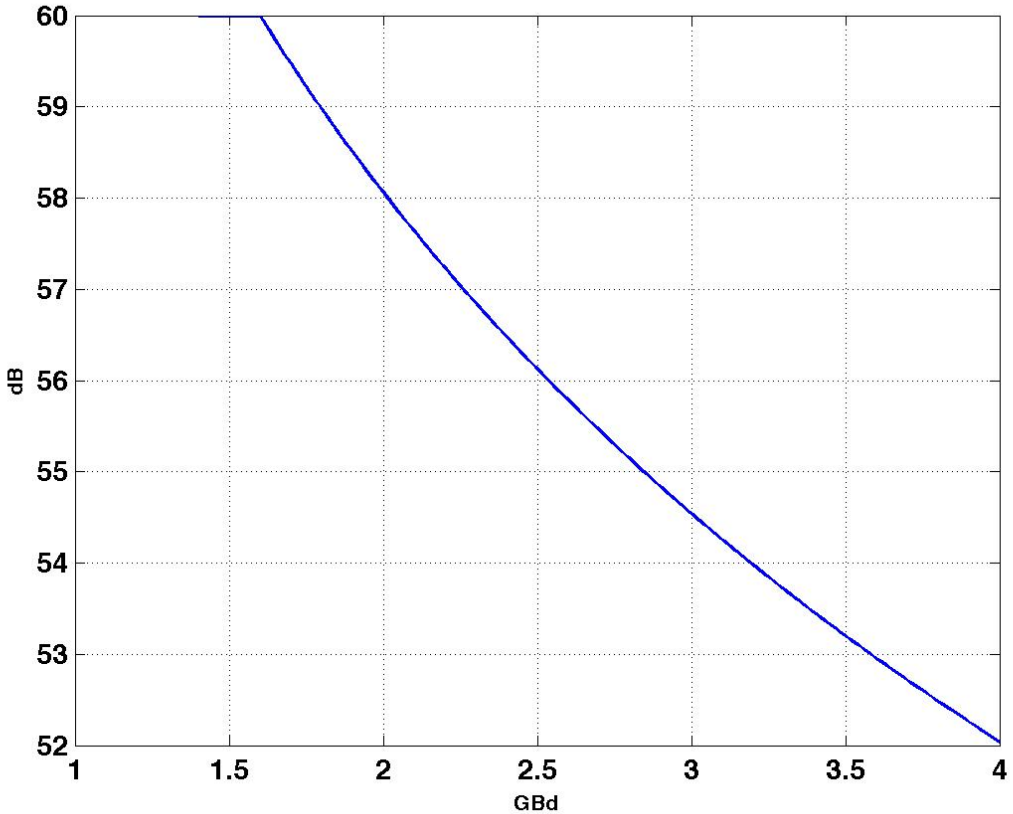

Figure: The Scaling Rule for the Residue Nonlinear Echo vs Symbol Rate

Nonlinear Echo SNR Floor

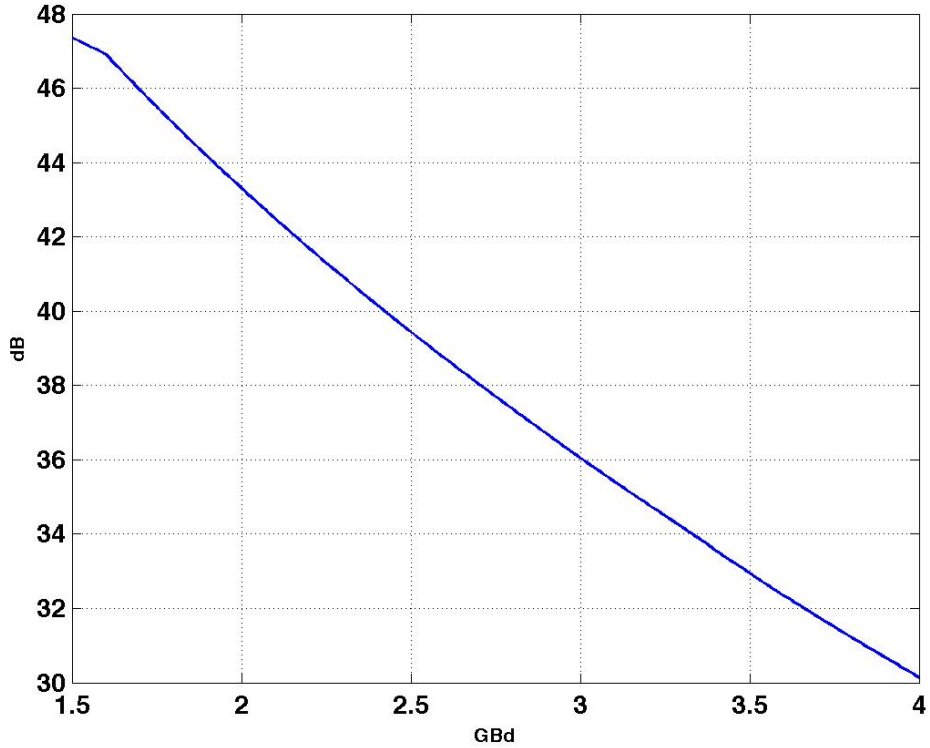

Figure: The SNR Floor due to the Nonlinear Echo vs Symbol Rate for the 40m Cable

Nonlinear Echo SNR Loss

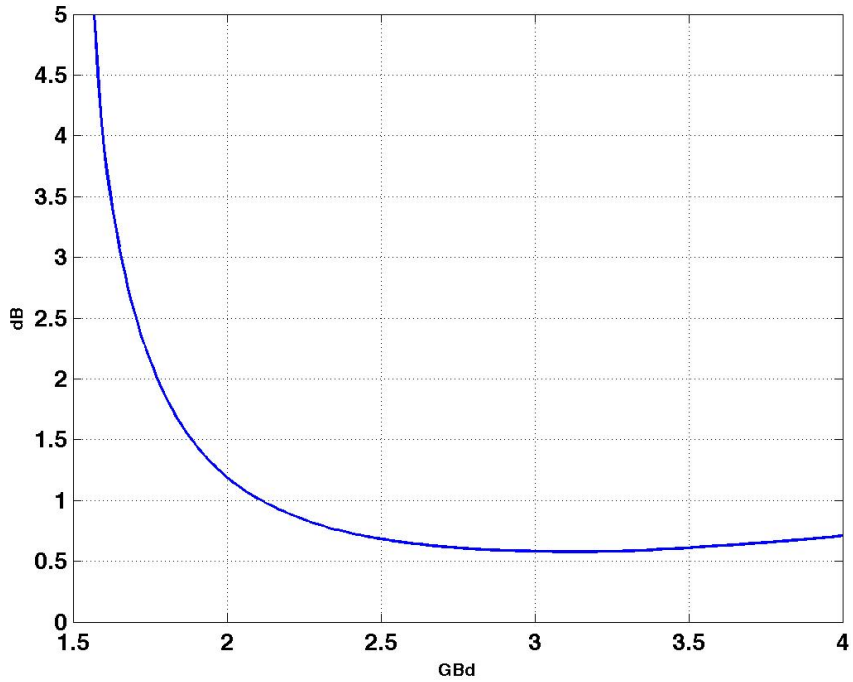

Figure: The SNR Loss due to the Nonlinear Echo vs Symbol Rate for the 40m Cable

- The loss in link margin due to the nonlinear echo is less than 1.25 dB for $f_s > 2\,\text{GBd}$.

Nonlinear Echo SNR Loss for 30m

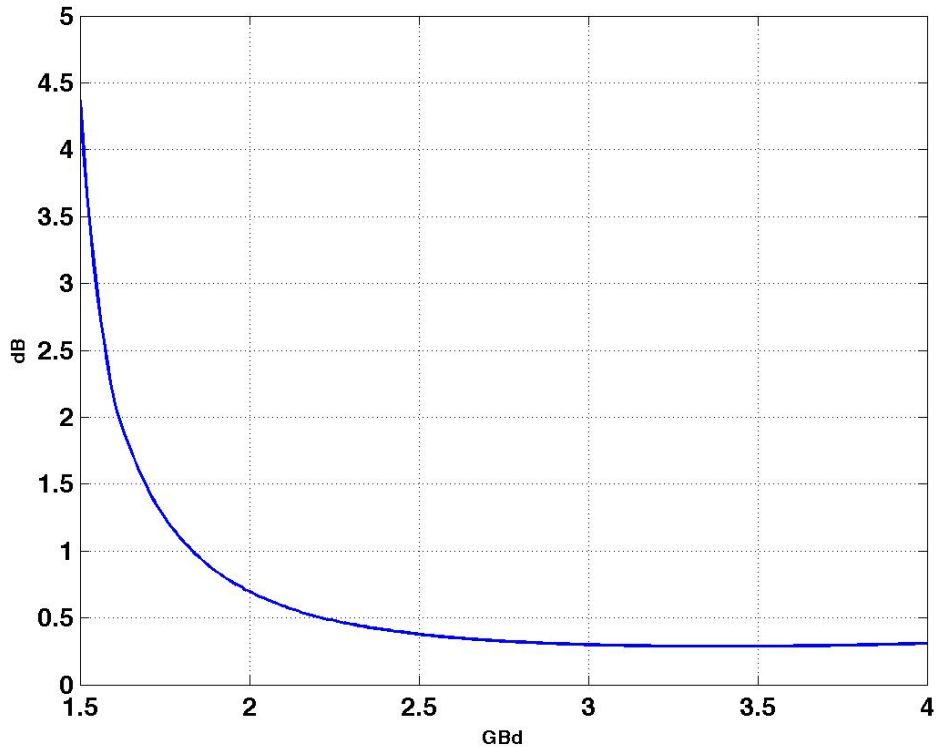

Figure: The SNR Loss due to the Nonlinear Echo vs Symbol Rate for a Scaled 30m

SNDR Requirement for ADC

- We allocate 3 dB loss in the link budget analysis for the ADC.
- Knowing the slicer SNR requirement and the digital noise enhancement, we calculate the required SNDR for the ADC:

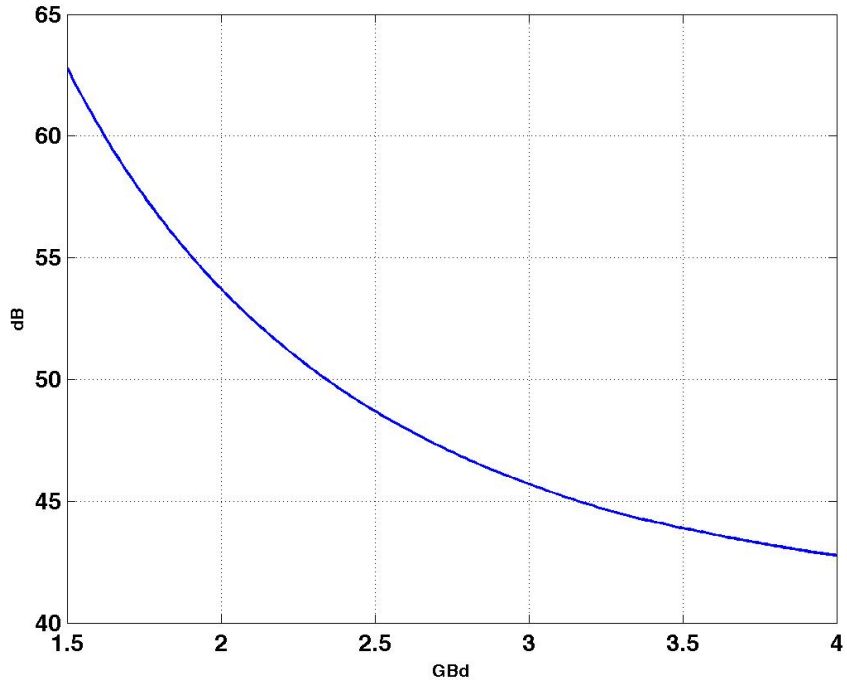

Figure: The SNDR Requirement for the ADC vs Symbol (Sampling) Rate for the 40m Cable

ENOB Requirements for ADC

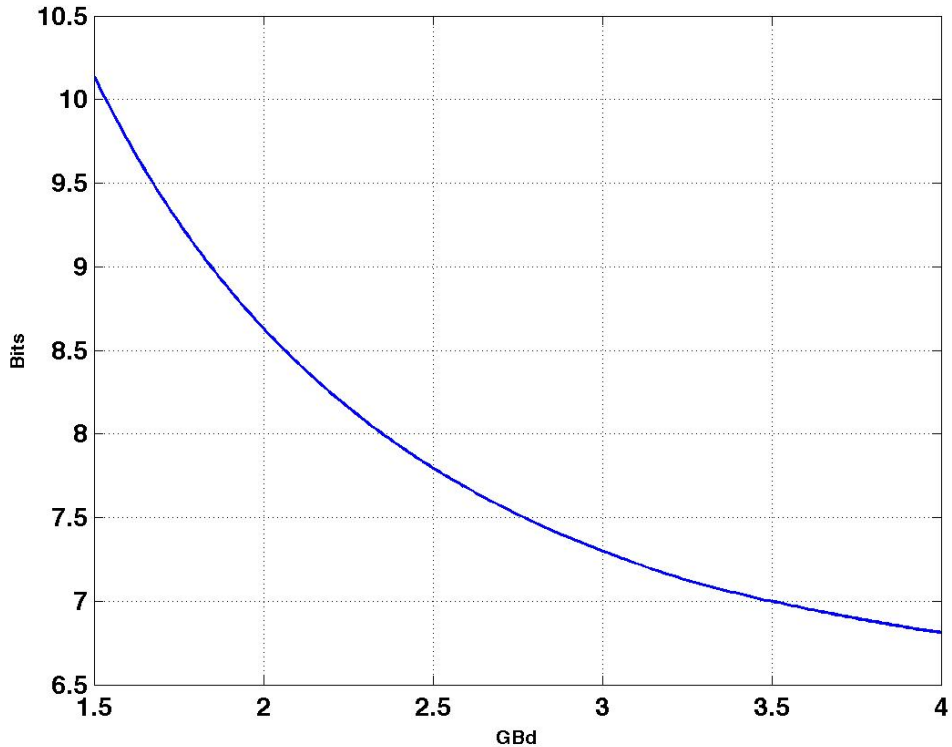

Figure: The ENOB Requirements for the ADC vs Symbol (Sampling) Rate for the 40m Cable

ADC SNDR Requirements for 30m

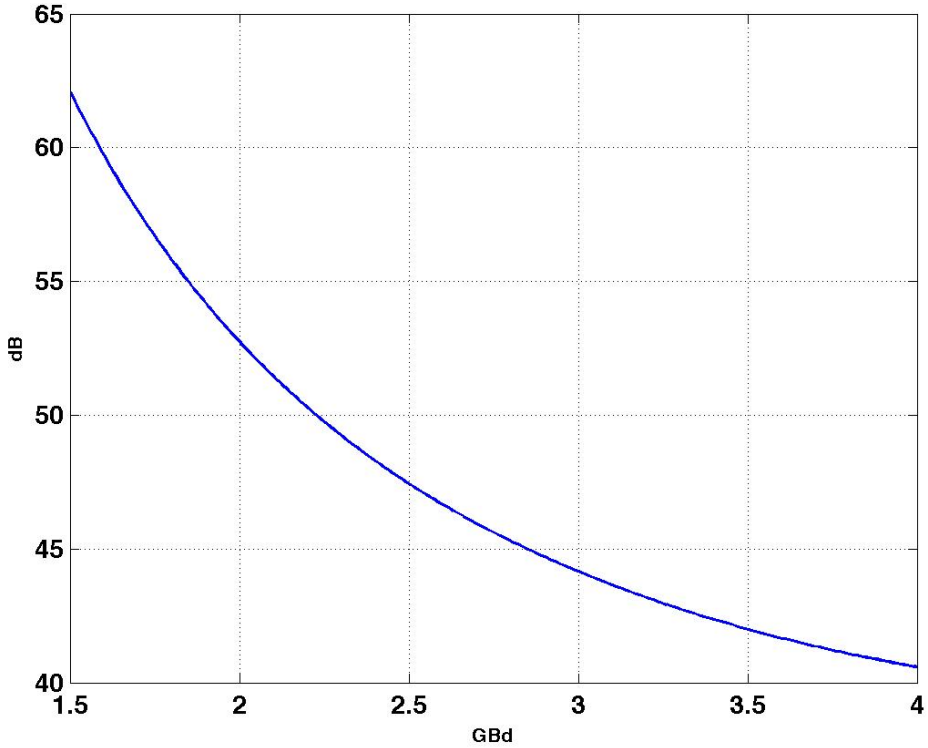

Figure: The SNDR Requirement for the ADC vs Symbol (Sampling) Rate for the 30m Cable

ADC ENOB Requirements for 30m

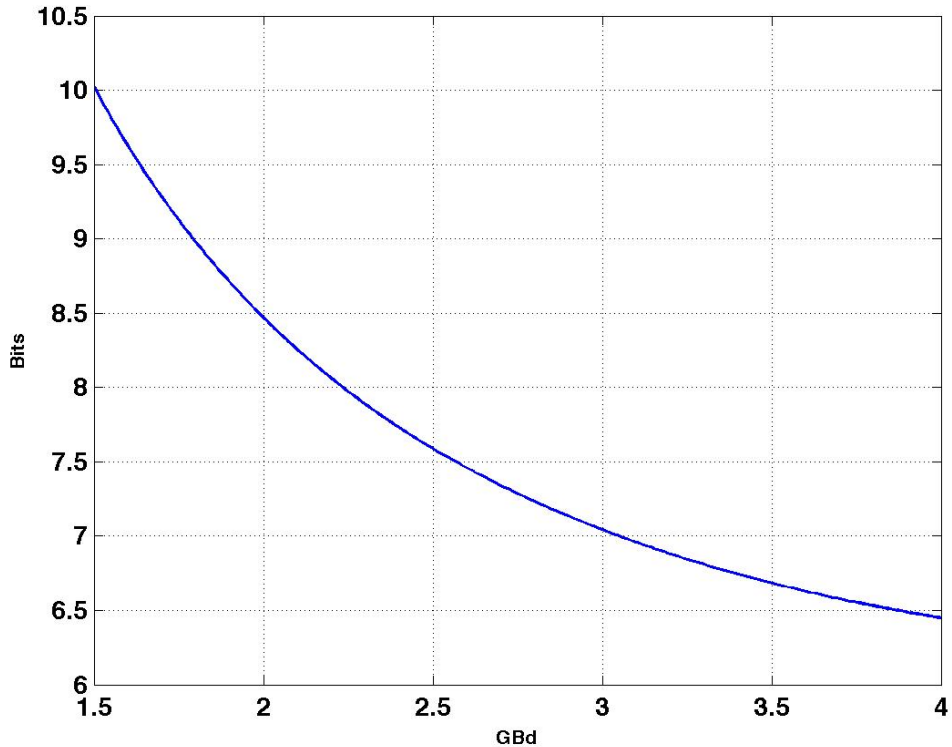

Figure: The ENOB Requirements for the ADC vs Symbol (Sampling) Rate for a Scaled 30m Cable

ADC Figures of Merit

- The Walden Figure of Merit (FOM_W) is used to scale the ADC performance vs the sampling rate and the power consumption:

$$\text{FOM}_W = \frac{P}{f_s 2^{\text{ENOB}}} \tag{1}$$

- In a scaling rule based on FOM_W, doubling the accuracy for a given sampling rate leads to doubling the power.
- Alternatively, the Schreier Figure of Merit results in a scaling where doubling the power only leads to 3 dB improvement in noise:

$$\text{FOM}_S = 10 \log 10\left(\frac{f_s}{2P}\right) + \text{SNDR} \tag{2}$$

- For a comprehensive survey of ADC's and the relevance of FOM_W vs FOM_S see: B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: `http://www.stanford.edu/~murmann/adcsurvey.html`.

ADC Power vs Symbol Rate

- The SNDR plot for the ADC shows that for $f_s > 2\,\text{GBd}$, FOM_W is more applicable than FOM_S. Therefore we use FOM_W to estimate the ADC power consumption as a function of the symbol rate:

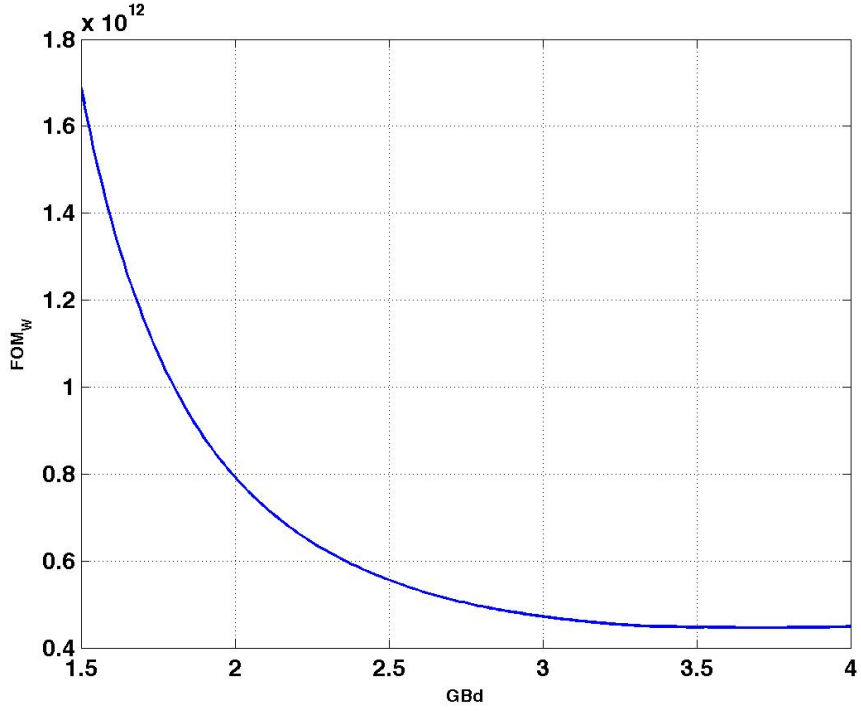

Figure: The Estimated ADC Power vs Symbol Rate for the 40m Cable

ADC Power vs Symbol Rate for 30m

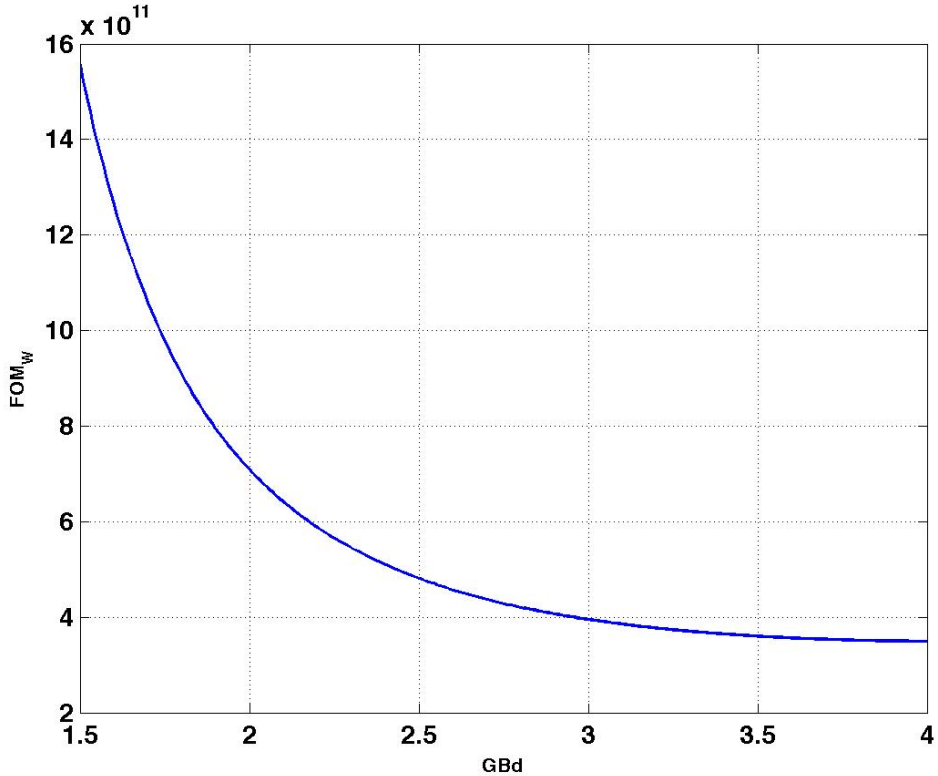

Figure: The Estimated ADC Power vs Symbol Rate for the Scaled 30m Cable

Discussions

- We analyzed two of the most important sources of impairments and power consumption for 40GBASE-T analog front ends.
- Our analysis shows that with a reasonable echo cancelation nonlinearity floor scaling rule, the associated loss will be less than 1.25 dB for $f_s > 2\,\text{GBd}$.
- The ADC power analysis shows that there is a significant power advantage in increasing the symbol rate to $f_s \approx 3\,\text{GBd}$.
- However, we expect that increasing the symbol rate will have a negative effect on the digital power consumption.
- We did not see a significant advantage in ADC power consumption in reducing the length from 40m to 30m.