

# Relative Power Estimates for 40GBASE-T over 25m and 30m on Category 8

Contribution to IEEE 802.3: NG-BASE-T Study Group Interim Meeting  
January 2013  
Phoenix, AZ USA

George Zimmerman, Ph.D.  
CME Consulting / Commscope

# Supporters

---

- Will Bliss, Broadcom
- David Chalupsky, Intel
- Michael Grimwood, Broadcom
- Paul Kish, Belden
- Wayne Larsen, Commscope
- William Lo, Marvell
- Gavin Parnaby, Marvell
- Sterling Vaden, OCC
- Peter Wu, Marvell

# Overview

---

- Methodologies
- Power and Reach #1 – Insertion Loss Comparisons
- Power and Reach #2 – 10GBASE-T PHY power scaling
- Power and Reach #3 – Detailed PHY analysis
- Reconciliation with Bliss
- Conclusions

# Methodologies

---

- In signal processing-heavy PHYs, power and complexity are difficult to estimate without detailed design
  - ***But - detailed design waits for Task Force!***
    - Estimates on 10GBASE-T ranged from 44X 1000BASE-T power to 6X 1000BASE-T power
    - First-generation was ~ 12X 1000BASE-T power at the time, today's is ~5-10X
- Study Group predictions inherently leave out three things
  - Overhead effects (leakage, interfaces)
  - Innovation driven by challenges
  - Problems uncovered during task force

# Methodologies (2)

---

- Proposed Method – surround the problem
  - Consider channel differences –
    - Provides a sanity check as to how much results should differ
  - Consider existing PHYs
    - Includes overhead effects and possibly relevant architectures
    - Understate optimization, because its based on one solution to an existing problem
  - Consider complexity/power models based on modulation/impairment studies
    - E.g., cancellation, receiver noise, bandwidth requirements
    - Provides relative estimation
    - Leaves out overhead and architecture change effects
- Consider all 3 to bound the space

# Importance of Insertion Loss

---

- All PHY assumptions assume cancellation of internal noise
- All PHY assumptions are driven by external or circuit noise limitations
- Insertion loss determines TX power, RX noise floor, Cancellation and Equalization requirements
- Existing PHYs can be examined for IL
  - IL at the middle of the used band ( $1/2$  Nyquist) is a good single metric, sometimes Nyquist is used too.

***IL sensitivity is common to all estimations***

# Comparative Technologies & IL

Technology	Bits / Sec / Hz /pair	Mid-Band Freq. (1/2 Nyquist)	Insertion Loss at Mid Band	Band-edge Freq. (Nyquist)	Insertion Loss at Band-edge	Primary Impairments
100BASE-TX (dual-simplex)	2	31.25 MHz	12.6 dB	62.5 MHz	18.5 dB	Near-End Crosstalk & Intersymbol Interference
1000BASE-T (echo-cancelled)	4.1	31.25 MHz	12.6 dB (100m) >18 dB (typical)	62.5 MHz	18.5 dB	Far-End & (residual) Near-End Crosstalk
10GBASE-T (echo-cancelled)	6.35	200 MHz	31.7 dB	400 MHz	46.9 dB	Alien Crosstalk & Receiver Noise/Residual Echo
40GBASE-CR4 (simplex)	2	2.571825 GHz	12.7 dB*	5.15625 GHz	20.9 dB	Timing Jitter, Near & Far-End Crosstalk

\* Loss is for cable assembly – Including PCB channel loss, mid band IL is up to 16.5dB

# 802.3an vs. Cat 8 25-30m Insertion Loss

## 802.3an Channel Insertion Loss (IL)

200 MHz = 31.7dB (100m)  
 400 MHz = 46.9 dB (100m)

$$\text{Insertion loss}(f) \leq 1.05 \left( 1.82 \times \sqrt{f} + 0.0169 \times f + \frac{0.25}{\sqrt{f}} \right) + 4 \times 0.02 \times \sqrt{f} \quad (\text{dB}) \quad (55-11)$$

## 40GBASE-T: TIA PN-568-C.2-1 draft 0.4 channel IL (30m cable)

$$\text{Insertion loss}(f) \leq 0.32 \left( 1.80\sqrt{f} + 0.005f + \frac{0.25}{\sqrt{f}} \right) + 2 \cdot B + 0.0324\sqrt{f} \text{ dB},$$

Where B=connecting hardware insertion loss (dB):

Frequency	B, Connecting HW IL (dB)
$1 \leq f \leq 500\text{MHz}$	$0.02\sqrt{f}$
$500 \leq f \leq 2000\text{MHz}$	$(0.008\sqrt{f} + 0.00029 \cdot f + 0.5 \cdot 10^{-6} f^2)$

Frequency	25m	30m
500MHz	13.2 dB	15.3 dB
1000MHz	19.8 dB	22.9 dB
800MHz	17.3 dB	20.0 dB
1600MHz	27.0 dB	31.0 dB

**10GBASE-T IL is substantially more (46.9 vs. 31 dB) than 30m target**



# Power and Reach #1 – Insertion Loss Comparison

---

- Insertion loss varies less than 16% from 25 to 30m (20% variation in length)
  - Unlikely to drive major architecture or bandwidth variation
- Insertion loss varies 2 to 4 dB between 25 & 30m
  - About 2X Connector + ILD budgets
  - Within cabling margin
  - Less than differences in PHY design points

***At either point, insertion loss looks more like 1000BASE-T than 10GBASE-T***

# Power and Reach #2 – 10GBASE-T PHY Power Scaling

---

- Existing 10GBASE-T PHYs optimize power consumed on a link
  - TX DAC power, DSP resolution, taps & cancellation, Analog front-end resolution & noise, coding gain are all tuned for reach
  - See WuParnaby\_01\_0113\_NGBT.pdf for more detail
- Methodology:
  - Determine equivalent reaches mapping NGBASE-T to 10GBASE-T
  - Measure reach-scaled 10GBASE-T power consumption as a % of total power to estimate savings
- Advantage: Includes overhead functions (e.g., PCS) and all blocks in estimate, not just the obvious ones
  - Experience shows this was a substantial oversight in 10GBASE-T estimates
- Disadvantage: Works on a fixed architecture, bandwidth & architecture not optimized for each reach
  - ***BUT: Bandwidth and architecture shouldn't vary much over 15-20% in IL / reach requirements***
  - ***AND: 10GBASE-T PHYs have been optimized for power vs. reach***

# 10GBASE-T PHY Power Scaling

- Exact results depend on bandwidth scheme used
  - Assume used bandwidths from 1GHz to 2GHz, using mid-band frequency
- Use “no link” measurement to estimate overhead

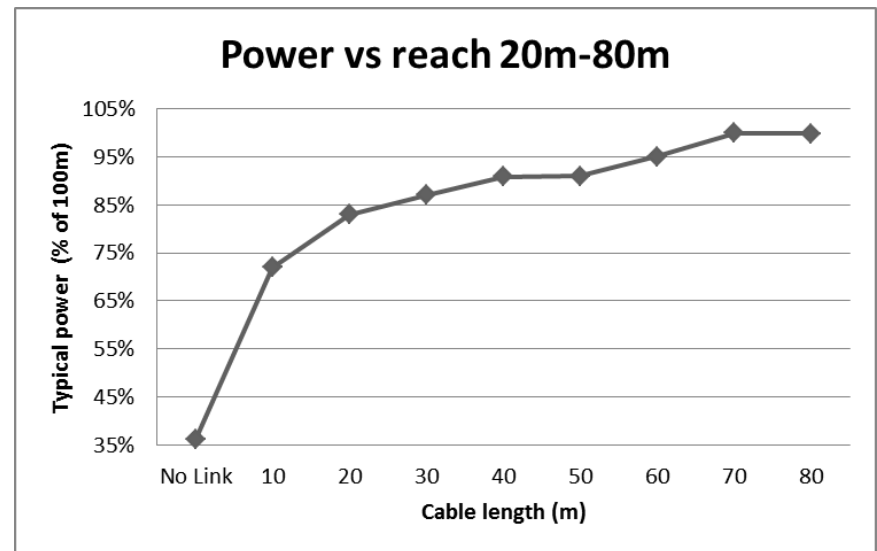
**Power varies 10-15% over range**

*Largely driven by big Transmit power back-off step*

**“Overhead” Power is 25-30%**

**Estimate is a little low, but shows effect of overhead in dewatering differences**

Mid-band Freq	25m equiv length	30m equiv length
500MHz	41.6 meters	48.3 meters
800MHz	54.6 meters	63.1 meters
1 GHz	62.4 meters	72.2 meters
Min/Max	41.6 (min)	72.2 (max)



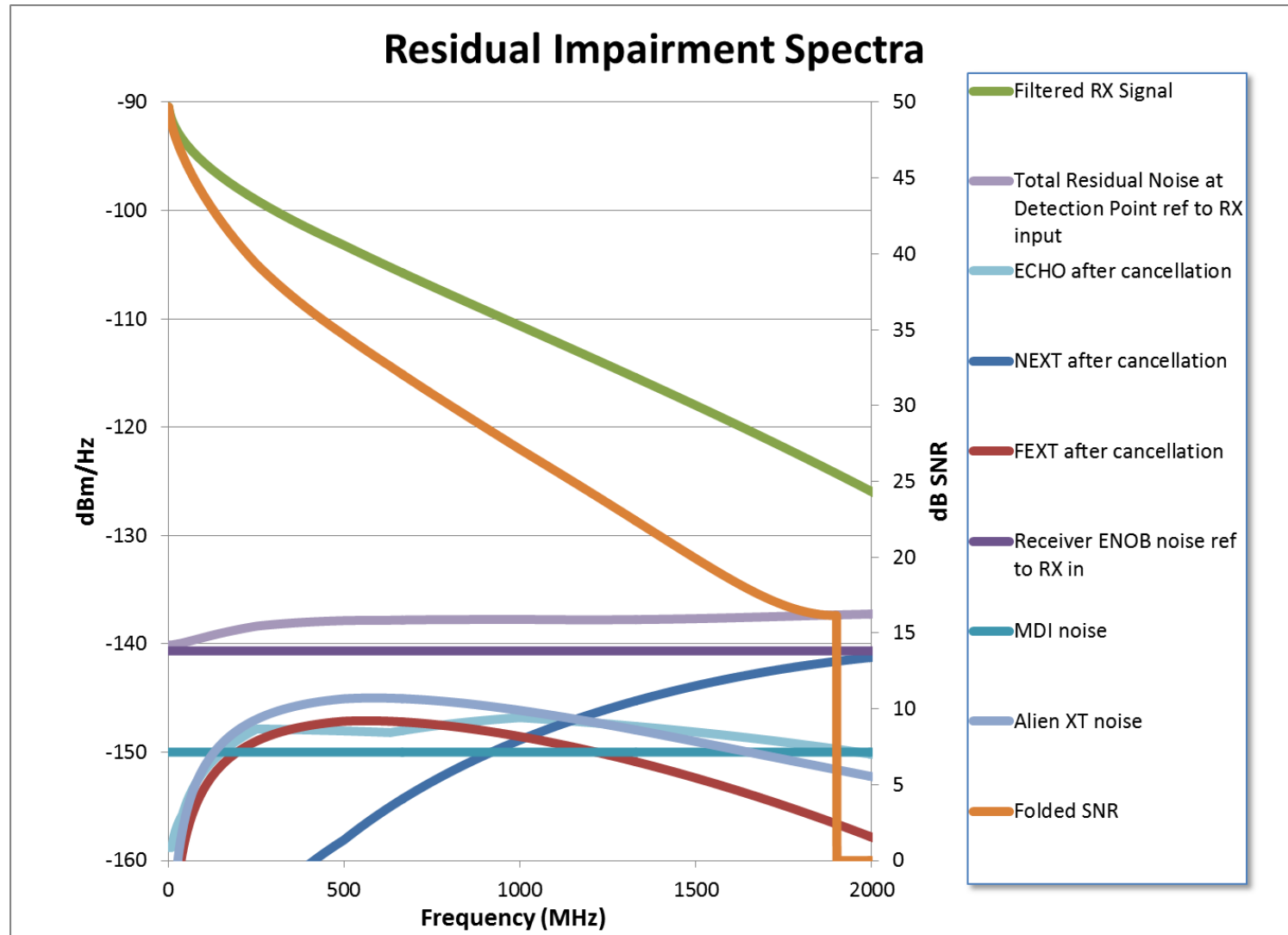
Source: WuParnaby\_01\_113.\_NGBTpdf

# Power & Reach 3:

## Detailed PHY Margin Analysis

- Detailed frequency-domain of cancellation & receiver noise requirements to achieve a given implementation margin over Optimum DFE (Salz) SNR
  - Varies bandwidth used, allows optimization of margin, complexity and/or power
  - Assumes code + format performance of 10GBASE-T rel. to capacity
  - Successfully used for tradeoffs in generations of DSL & 10GBASE-T
- Examines 6, 8 or 10dB implementation margin design points
- Channel based on TIA draft 0.5 Category 8 spec, and includes alien crosstalk at specified levels
  - Does not assume shielded cabling has negligible alien near-end or far-end crosstalk (ANEXT and AFEXT)
  - Slightly better than Cat 7a alien far-end crosstalk (AFEXT) levels

# Example – 8dB design point



# A Power Metric (1)

---

- PHY front-end power ( $\sim 1/3$  to  $1/2$  total power) is related to front-end bandwidth and SNR requirements, through a technology “figure of merit”

$$\text{FOM} = P / (2^{\text{ENOB}} * f_s)$$

- $f_s$  is 2 x bandwidth, ENOB is the receiver equivalent number of bits (a measure of SNR & SFDR), and P is the power consumed by the front end.
- For a given technology & skill, generally:  $P_{\text{FOM}} \sim 2^{\text{ENOB}} * f_s$
- This will tend to overestimate the differences in PHY designs:
  - Analog receiver is not the total PHY power
  - Analog receiver front ends tend to vary less with power than indicated when performance is below 55dB SNDR (8.85 bits ENOB) (see WuParnaby\_01\_0113\_NGBT.pdf, Murmann ADC Survey)

# A Power Metric (2)

---

- Power is compared by examining required cancellation and required front-end power
- Similar bandwidths & cancellations -> similar architecture & complexity
- Plenty of room for implementation margin (6 to 10dB vs. 4 to 6 dB with 10G)
- Estimates of unmodeled overhead power are 25-30% from 10G measurements

***Compare total PHY power at reaches, assuming analog receiver power is  $\frac{1}{2}$  to  $\frac{3}{4}$  of total PHY power, & other power doesn't vary with reach***

# PHY Power Comparison

- Minimum Analog Receiver power factors ( $P_{FOM}$ )\*

Channel	6 dB Design Point	8 dB Design Point	10 dB Design Point
25m	2.05	2.70	3.57
30m	2.95	3.89	5.40

- Relative total PHY Power Estimates

- Analog receiver ~ ½ PHY power (typical)

Channel	6 dB Design Point	8 dB Design Point	10 dB Design Point
25m	100%	100%	100%
30m	122%	122%	126%

- Analog receiver ~ ¾ PHY power (pessimistic)

Channel	6 dB Design Point	8 dB Design Point	10 dB Design Point
25m	100%	100%	100%
30m	133%	133%	138%

***Greater power trade in margin design point than in 5m of reach***

\* Detailed results in supporting data slides in backup



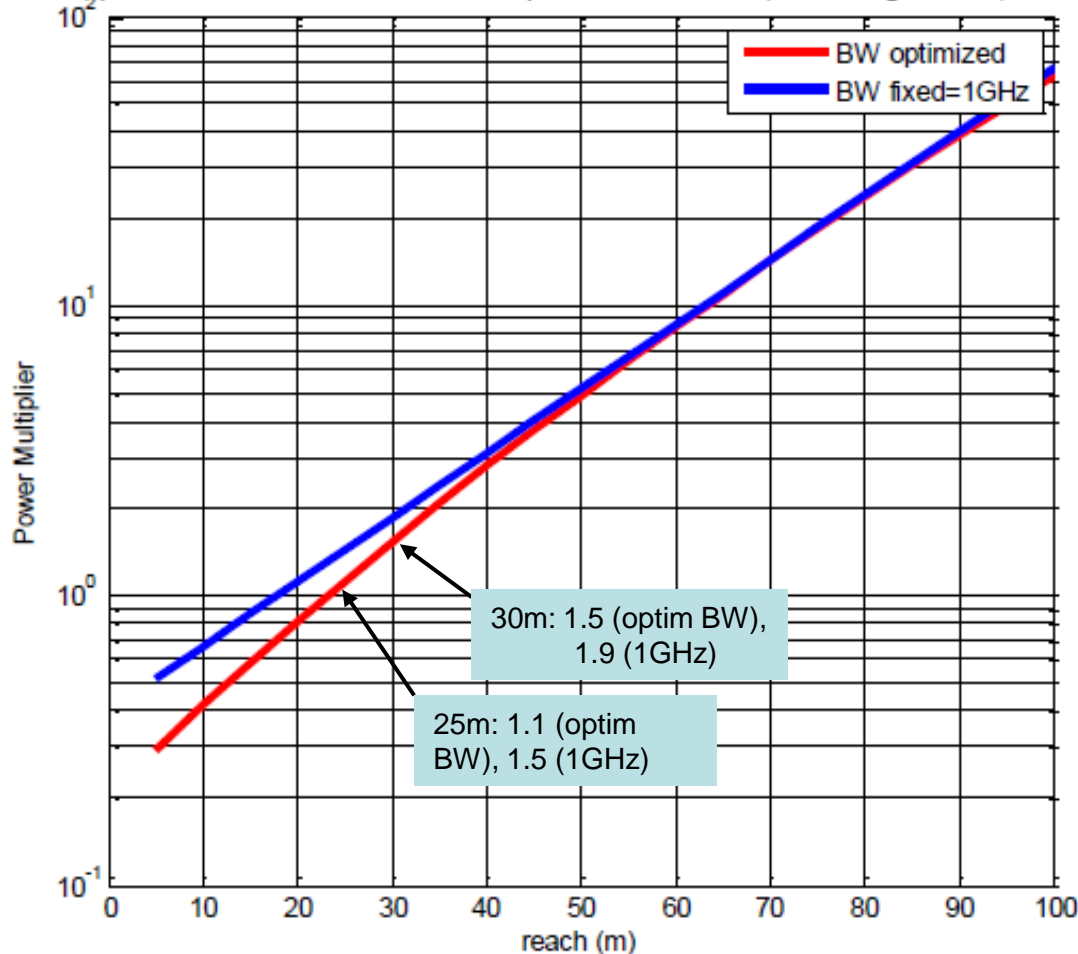
# Observations

---

- Viable bandwidths are within 25% range, minimum cancellations are roughly equivalent for 25 vs. 30m
  - Implies negligible difference in DSP power
- Receiver requirements are within 0.5 bits on 6dB margin point, and can stay below 55dB SNDR ( $>8.85\text{ENOB}$ )
  - Power dependency is probably pessimistic
  - Allows designers trades they did not have in 10GBASE-T
- Alien FEXT specification may be limiting
  - Self-noise limitation means transmit power can probably be adjusted down for power savings
- Pessimistic estimate of PHY power increase for increasing channel from 25 to 30m is 22-33% of total PHY power, including constant overhead
  - Variation caused by design choice from 6 dB implementation margin to 10dB implementation margin is much greater: 41.5-62%

# Reconciliation to Bliss\_1\_0912

Power Multiplier wrt 10GB-T vs. Reach for 40Gbps. TXlaunch=3dBm, TotalMargin=10dB, Self Noise



## Power ratios 25m/30m:

- Optimum BW=36%
- 1GHz BW=26%

## Model Differences:

- Bliss model doesn't include Alien FEXT, which limits lower BW power
- Zimmerman model has a term to include non-signal processing overhead

**YET, Results are in-line**

Source: Bliss\_01\_0912.pdf, slide 25

# Summary of Results

---

- Insertion Loss: comparison of 25m to 30m showed only 16% variation
  - Connectors and ILD dilute the length difference
- Existing PHYs: Power scaled 10GBASE-T indicates < 15% power variation for 40G between 25 & 30m reach
  - 25% overhead in PHY power due to non-reach related effects
- Detailed PHY margin analysis: Multiple design points with 6-10dB implementation margin within <33% total PHY power difference between 25m & 30m design points
  - Bliss\_01\_0912 analysis showed 26 to 36% difference

***Results suggest errors in estimates are greater than 5 meter differences in reach***

# Conclusions

---

- 25-30m design of NGBASE-T is more like 1000BASE-T (at higher frequency) than it is like 10GBASE-T in signal loss
- Power differences are likely small
  - Measured a variety of ways bound it between 15-36%
- Recommend decisions based on marketing considerations

---

# SUPPORTING DATA

# Analog Receiver Parameters

## Cat8 d0.5spec, Power factors are relative

### 10dB Margin Point

p_BAUD	25 meters					30 meters				
	Min of ADC_FOM_power	Min of p_RXENOB	Min of p_NEXT REDUX	Min of p_ECHO REDUX	Min of p_FEXT REDUX	Min of ADC_FOM_power	Min of p_RXENOB	Min of p_NEXT REDUX	Min of p_ECHO REDUX	Min of p_FEXT REDUX
3200						6.55	10	50	100	100
3400						6.06	9.8	50	100	30
3600	3.69	9	100	100	100	5.59	9.6	50	50	30
3800	3.89	9	50	100	30	5.90	9.6	45	50	25
4000	3.57	8.8	50	50	30	5.40	9.4	50	50	25

### 6 dB Margin Point

p_BAUD	25 meters					30 meters				
	Min of ADC_FOM_power	Min of p_RXENOB	Min of p_NEXT REDUX	Min of p_ECHO REDUX	Min of p_FEXT REDUX	Min of ADC_FOM_power	Min of p_RXENOB	Min of p_NEXT REDUX	Min of p_ECHO REDUX	Min of p_FEXT REDUX
2400	2.46	9	45	100	100	3.24	9.4	40	50	25
2800	2.50	8.8	40	50	25	3.29	9.2	40	45	25
3200	2.48	8.6	35	45	25	3.28	9	40	45	20
3400	2.30	8.4	35	45	20	3.03	8.8	40	45	20
3600	2.12	8.2	35	40	20	3.21	8.8	40	45	20
3800	2.23	8.2	35	40	20	2.95	8.6	40	45	20
4000	2.05	8	35	40	20	3.10	8.6	40	45	20

Min ADC Power factors: 25m = 3.57/2.05, 30m = 5.40/2.95,  
 Greater power tradeoff in picking margin design point than in 5m of reach